

**TL071, TL071A, TL071B, TL072  
TL072A, TL072B, TL074, TL074A, TL074B  
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS**

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- Low Power Consumption
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short-Circuit Protection
- Low Total Harmonic Distortion . . . 0.003% Typ
- Low Noise  
 $V_n = 18 \text{ nV}/\sqrt{\text{Hz}}$  Typ at  $f = 1 \text{ kHz}$
- High Input Impedance . . . JFET Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . .  $13 \text{ V}/\mu\text{s}$  Typ
- Common-Mode Input Voltage Range Includes  $V_{CC+}$

### description/ordering information

The JFET-input operational amplifiers in the TL07x series are similar to the TL08x series, with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07x series ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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**description/ordering information (continued)**

**ORDERING INFORMATION**

$T_A$	$V_{IOMax}$ AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	10 mV	PDIP (P)	Tube of 50	TL071CP	TL071CP
			Tube of 50	TL072CP	TL072CP
		PDIP (N)	Tube of 25	TL074CN	TL074CN
		SOIC (D)	Tube of 75	TL071CD	TL071C
			Reel of 2500	TL071CDR	
			Tube of 75	TL072CD	TL072C
			Reel of 2500	TL072CDR	
			Tube of 50	TL074CD	TL074C
			Reel of 2500	TL074CDR	
		SOP (NS)	Reel of 2000	TL074CNSR	TL074
		SOP (PS)	Reel of 2000	TL071CPSR	TL071
			Reel of 2000	TL072CPSR	T072
		TSSOP (PW)	Reel of 2000	TL072CPWR	T072
			Tube of 90	TL074CPW	T074
			Reel of 2000	TL074CPWR	
	6 mV	PDIP (P)	Tube of 50	TL071ACP	TL071ACP
			Tube of 50	TL072ACP	TL072ACP
		PDIP (N)	Tube of 25	TL074ACN	TL074ACN
		SOIC (D)	Tube of 75	TL071ACD	071AC
			Reel of 2500	TL071ACDR	
			Tube of 75	TL072ACD	072AC
			Reel of 2500	TL072ACDR	
			Tube of 50	TL074ACD	TL074AC
			Reel of 2500	TL074ACDR	
		SOP (PS)	Reel of 2000	TL072ACPSR	T072A
	SOP (NS)	Reel of 2000	TL074ACNSR	TL074A	
	3 mV	PDIP (P)	Tube of 50	TL071BCP	TL071BCP
			Tube of 50	TL072BCP	TL072BCP
		PDIP (N)	Tube of 25	TL074BCN	TL074BCN
		SOIC (D)	Tube of 75	TL071BCD	071BC
Reel of 2500			TL071BCDR		
Tube of 75			TL072BCD	072BC	
Reel of 2500			TL072BCDR		
Tube of 50			TL074BCD	TL074BC	
Reel of 2500			TL074BCDR		
SOP (NS)		Reel of 2000	TL074BCNSR	TL074B	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**description/ordering information (continued)**

**ORDERING INFORMATION**

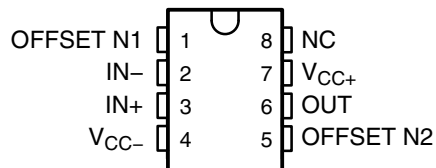
$T_A$	$V_{IOmax}$ AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	6 mV	PDIP (P)	Tube of 50	TL071IP	TL071IP
			Tube of 50	TL072IP	TL072IP
		PDIP (N)	Tube of 25	TL074IN	TL074IN
		SOIC (D)	Tube of 75	TL071ID	TL071I
			Reel of 2500	TL071IDR	
			Tube of 75	TL072ID	TL072I
			Reel of 2500	TL072IDR	
			Tube of 50	TL074ID	TL074I
			Reel of 2500	TL074IDR	
		-55°C to 125°C	6 mV	CDIP (JG)	Tube of 50
CFP (U)	Tube of 150			TL072MUB	TL072MUB
LCCC (FK)	Tube of 55			TL072MFKB	TL072MFKB
9 mV	CDIP (J)		Tube of 25	TL074MJB	TL074MJB
	CFP (W)		Tube of 25	TL074MWB	TL074MWB
	LCCC (FK)		Tube of 55	TL074MFKB	TL074MFKB

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

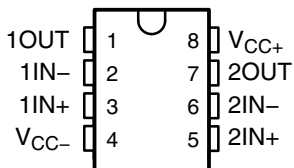
# TL071, TL071A, TL071B, TL072 TL072A, TL072B, TL074, TL074A, TL074B LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

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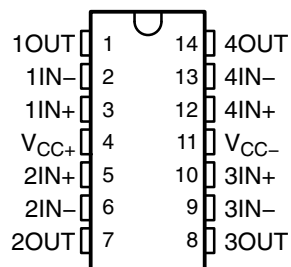
**TL071, TL071A, TL071B**  
D, P, OR PS PACKAGE  
(TOP VIEW)



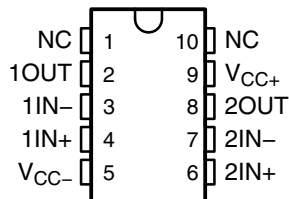
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D, JG, P, PS, OR PW PACKAGE  
(TOP VIEW)



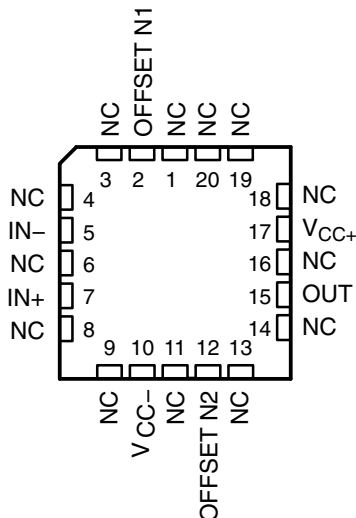
**TL074A, TL074B**  
D, J, N, NS, OR PW PACKAGE  
TL074 . . . D, J, N, NS, PW,  
OR W PACKAGE  
(TOP VIEW)



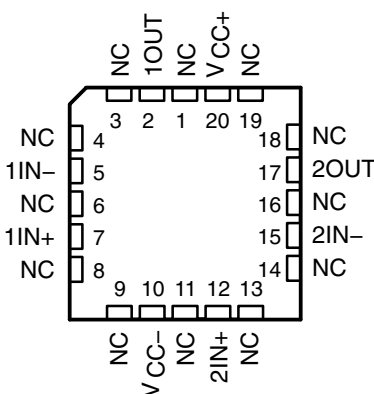
**TL072**  
U PACKAGE  
(TOP VIEW)



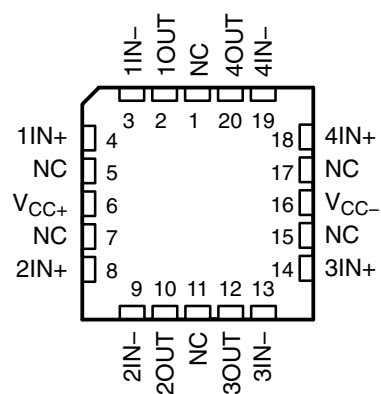
**TL071**  
FK PACKAGE  
(TOP VIEW)



**TL072**  
FK PACKAGE  
(TOP VIEW)

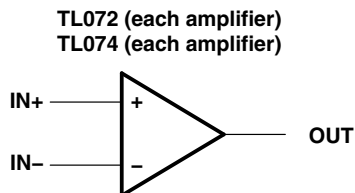
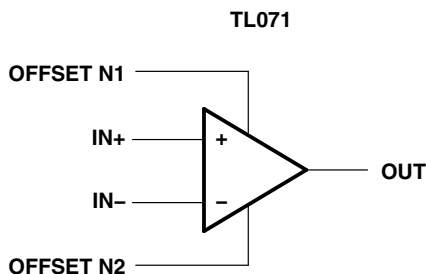


**TL074**  
FK PACKAGE  
(TOP VIEW)



NC – No internal connection

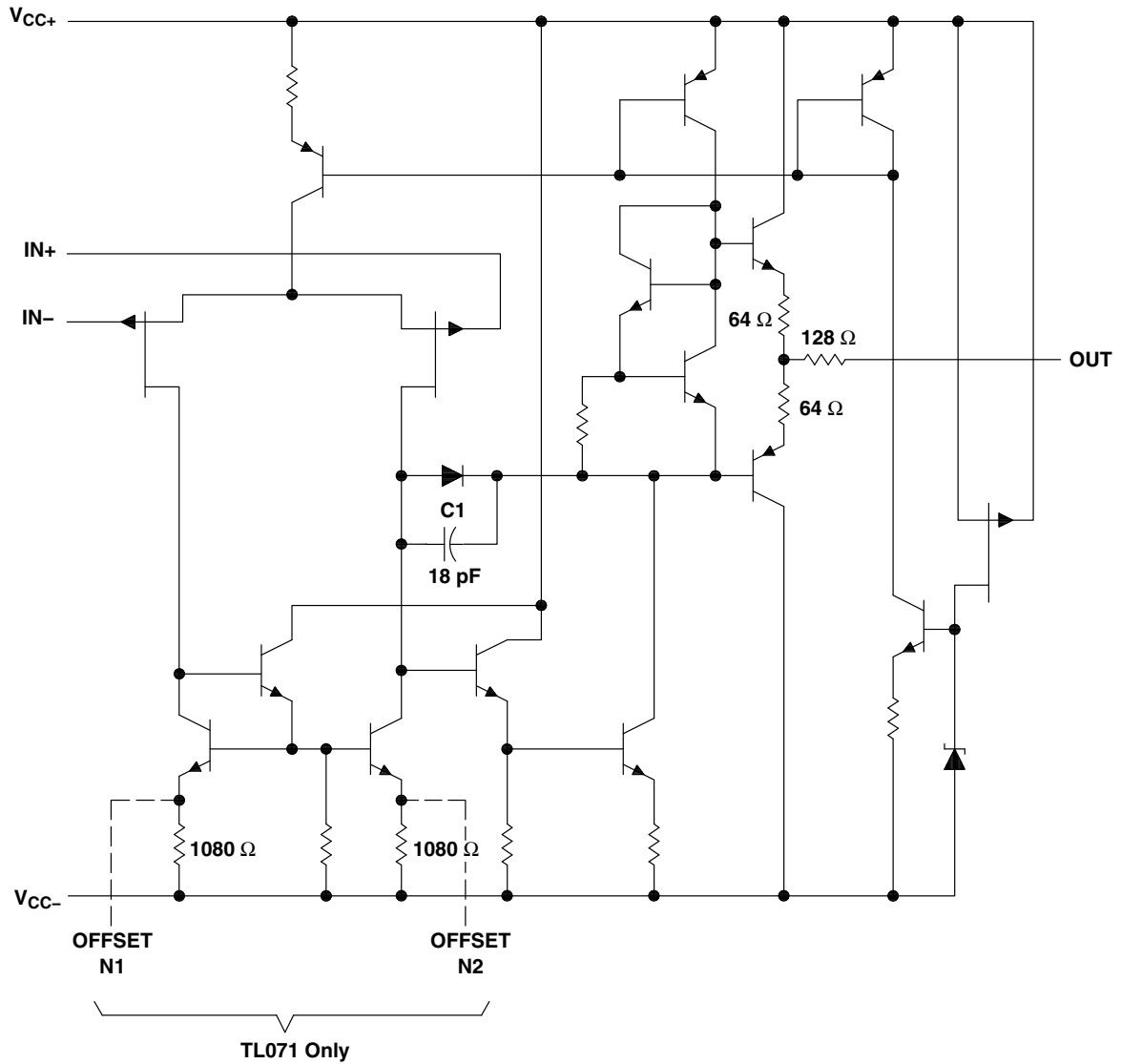
## symbols



**TL071, TL071A, TL071B, TL072  
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schematic (each amplifier)



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	TL071	TL072	TL074
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	6
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

† Includes bias and trim circuitry

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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage (see Note 1): $V_{CC+}$ .....	18 V
$V_{CC-}$ .....	-18 V
Differential input voltage, $V_{ID}$ (see Note 2) .....	$\pm 30$ V
Input voltage, $V_I$ (see Notes 1 and 3) .....	$\pm 15$ V
Duration of output short circuit (see Note 4) .....	Unlimited
Package thermal impedance, $\theta_{JA}$ (see Notes 5 and 6): D package (8 pin) .....	97°C/W
D package (14 pin) .....	86°C/W
N package .....	80°C/W
NS package .....	76°C/W
P package .....	85°C/W
PS package .....	95°C/W
PW package (8 pin) .....	149°C/W
PW package (14 pin) .....	113°C/W
U package .....	185°C/W
Package thermal impedance, $\theta_{JC}$ (see Notes 7 and 8): FK package .....	5.61°C/W
J package .....	15.05°C/W
JG package .....	14.5°C/W
W package .....	14.65°C/W
Operating virtual junction temperature, $T_J$ .....	150°C
Case temperature for 60 seconds: FK package .....	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J, JG, or W package .....	300°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
  2. Differential voltages are at  $IN+$ , with respect to  $IN-$ .
  3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
  4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
  5. Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  6. The package thermal impedance is calculated in accordance with JESD 51-7.
  7. Maximum power dissipation is a function of  $T_J(\max)$ ,  $\theta_{JC}$ , and  $T_C$ . The maximum allowable power dissipation at any allowable case temperature is  $P_D = (T_J(\max) - T_C)/\theta_{JC}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  8. The package thermal impedance is calculated in accordance with MIL-STD-883.



electrical characteristics,  $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	$T_A$ ‡	TL071C TL072C TL074C			TL071AC TL072AC TL074AC			TL071BC TL072BC TL074BC			TL071I TL072I TL074I			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$V_{IO}$	Input offset voltage	$V_O = 0, R_S = 50\ \Omega$	25°C	3	10		3	6		2	3		3	6	mV	
			Full range			13		7.5		5		8				
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage	$V_O = 0, R_S = 50\ \Omega$	Full range	18			18			18			18			$\mu\text{V}/^\circ\text{C}$
$I_{IO}$	Input offset current	$V_O = 0$	25°C	5	100		5	100		5	100		5	100	pA	
			Full range		10		2		2		2					
$I_{IB}$	Input bias current§	$V_O = 0$	25°C	65	200		65	200		65	200		65	200	pA	
			Full range		7		7		7		20					
$V_{ICR}$	Common-mode input voltage range		25°C	$\pm 11$	-12 to 15		$\pm 11$	-12 to 15		$\pm 11$	-12 to 15		$\pm 11$	-12 to 15	V	
$V_{OM}$	Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	$\pm 12$	$\pm 13.5$		$\pm 12$	$\pm 13.5$		$\pm 12$	$\pm 13.5$		$\pm 12$	$\pm 13.5$	V	
			Full range	$R_L \geq 10\ \text{k}\Omega$	$\pm 12$			$\pm 12$			$\pm 12$			$\pm 12$		
				$R_L \geq 2\ \text{k}\Omega$	$\pm 10$			$\pm 10$			$\pm 10$			$\pm 10$		
$A_{VD}$	Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L \geq 2\ \text{k}\Omega$	25°C	25	200		50	200		50	200		50	200	V/mV	
			Full range	15		25		25								
$B_1$	Unity-gain bandwidth		25°C	3			3			3			3			MHz
$r_i$	Input resistance		25°C	$10^{12}$			$10^{12}$			$10^{12}$			$10^{12}$			$\Omega$
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}, V_O = 0, R_S = 50\ \Omega$	25°C	70	100		75	100		75	100		75	100	dB	
$k_{SVR}$	Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = \pm 9\ \text{V to } \pm 15\ \text{V}, V_O = 0, R_S = 50\ \Omega$	25°C	70	100		80	100		80	100		80	100	dB	
$I_{CC}$	Supply current (each amplifier)	$V_O = 0, \text{ No load}$	25°C	1.4	2.5		1.4	2.5		1.4	2.5		1.4	2.5	mA	
$V_{O1}/V_{O2}$	Crosstalk attenuation	$A_{VD} = 100$	25°C	120			120			120			120			dB

† All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.

‡ Full range is  $T_A = 0^\circ\text{C to } 70^\circ\text{C}$  for TL07\_C, TL07\_AC, TL07\_BC and is  $T_A = -40^\circ\text{C to } 85^\circ\text{C}$  for TL07\_I.

§ Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 4. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

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**electrical characteristics,  $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)**

PARAMETER	TEST CONDITIONS†	$T_A$ ‡	TL071M TL072M			TL074M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_O = 0, R_S = 50\ \Omega$	25°C		3	6		3	9	mV
		Full range			9			15	
$\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage	$V_O = 0, R_S = 50\ \Omega$	Full range		18			18		$\mu\text{V}/^\circ\text{C}$
$I_{IO}$ Input offset current	$V_O = 0$	25°C		5	100		5	100	pA
		Full range			20			20	nA
$I_{IB}$ Input bias current‡	$V_O = 0$	25°C		65	200		65	200	pA
		Full range			50			50	nA
$V_{ICR}$ Common-mode input voltage range		25°C	$\pm 11$	-12 to 15		$\pm 11$	-12 to 15		V
$V_{OM}$ Maximum peak output voltage swing	$R_L = 10\ \text{k}\Omega$	25°C	$\pm 12$	$\pm 13.5$		$\pm 12$	$\pm 13.5$		V
	$R_L \geq 10\ \text{k}\Omega$	Full range	$\pm 12$			$\pm 12$			
	$R_L \geq 2\ \text{k}\Omega$		$\pm 10$			$\pm 10$			
$A_{VD}$ Large-signal differential voltage amplification	$V_O = \pm 10\ \text{V}, R_L \geq 2\ \text{k}\Omega$	25°C	35	200		35	200		V/mV
		Full range	15			15			
$B_1$ Unity-gain bandwidth	$T_A = 25^\circ\text{C}$			3			3		MHz
$r_i$ Input resistance	$T_A = 25^\circ\text{C}$			$10^{12}$			$10^{12}$		$\Omega$
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR\text{min}}, V_O = 0, R_S = 50\ \Omega$	25°C	80	86		80	86		dB
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ )	$V_{CC} = \pm 9\ \text{V to } \pm 15\ \text{V}, V_O = 0, R_S = 50\ \Omega$	25°C	80	86		80	86		dB
$I_{CC}$ Supply current (each amplifier)	$V_O = 0, \text{ No load}$	25°C		1.4	2.5		1.4	2.5	mA
$V_{O1}/V_{O2}$ Crosstalk attenuation	$A_{VD} = 100$	25°C		120			120		dB

† Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 4. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

‡ All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ .





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TL072A, TL072B, TL074, TL074A, TL074B**  
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operating characteristics,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TL07xM			ALL OTHERS			UNIT			
		MIN	TYP	MAX	MIN	TYP	MAX				
SR	Slew rate at unity gain $V_I = 10\text{ V}$ , $C_L = 100\text{ pF}$	$R_L = 2\text{ k}\Omega$ , See Figure 1			5	13		8	13	$\text{V}/\mu\text{s}$	
$t_r$	Rise-time overshoot factor $V_I = 20\text{ mV}$ , $C_L = 100\text{ pF}$	$R_L = 2\text{ k}\Omega$ , See Figure 1			0.1			0.1			$\mu\text{s}$
					20%			20%			
$V_n$	Equivalent input noise voltage $R_S = 20\ \Omega$	$f = 1\text{ kHz}$			18			18			$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ Hz to } 10\text{ kHz}$			4			4			$\mu\text{V}$
$I_n$	Equivalent input noise current $R_S = 20\ \Omega$	$f = 1\text{ kHz}$			0.01			0.01			$\text{pA}/\sqrt{\text{Hz}}$
THD	Total harmonic distortion $V_{\text{rms}} = 6\text{ V}$ , $R_L \geq 2\text{ k}\Omega$ , $f = 1\text{ kHz}$	$A_{VD} = 1$ , $R_S \leq 1\text{ k}\Omega$			0.003 %			0.003%			

**PARAMETER MEASUREMENT INFORMATION**

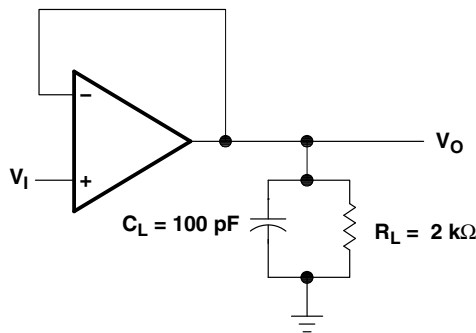


Figure 1. Unity-Gain Amplifier

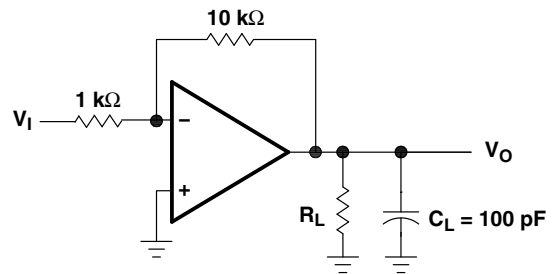


Figure 2. Gain-of-10 Inverting Amplifier

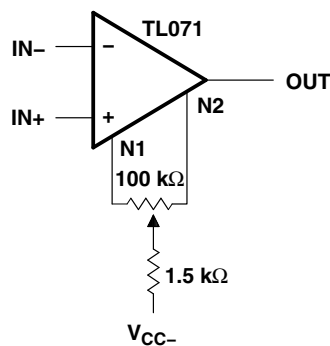


Figure 3. Input Offset-Voltage Null Circuit

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**TYPICAL CHARACTERISTICS**

**Table of Graphs**

			<b>FIGURE</b>
$I_{IB}$	Input bias current	vs Free-air temperature	4
$V_{OM}$	Maximum output voltage	vs Frequency	5, 6, 7
		vs Free-air temperature	8
		vs Load resistance	9
		vs Supply voltage	10
$A_{VD}$	Large-signal differential voltage amplification	vs Free-air temperature	11
		vs Frequency	12
	Phase shift	vs Frequency	12
	Normalized unity-gain bandwidth	vs Free-air temperature	13
	Normalized phase shift	vs Free-air temperature	13
$CMRR$	Common-mode rejection ratio	vs Free-air temperature	14
$I_{CC}$	Supply current	vs Supply voltage	15
		vs Free-air temperature	16
$P_D$	Total power dissipation	vs Free-air temperature	17
		Normalized slew rate	vs Free-air temperature
$V_n$	Equivalent input noise voltage	vs Frequency	19
$THD$	Total harmonic distortion	vs Frequency	20
		Large-signal pulse response	vs Time
$V_O$	Output voltage	vs Elapsed time	22



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### TYPICAL CHARACTERISTICS†

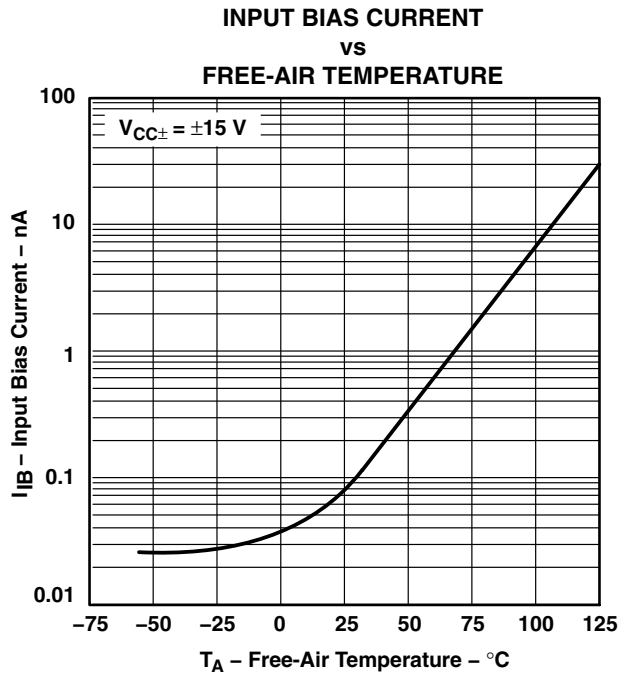


Figure 4

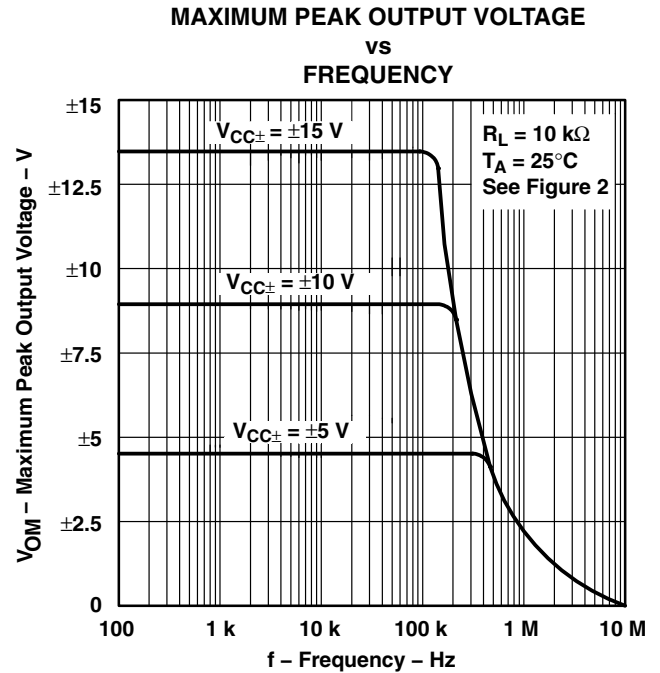


Figure 5

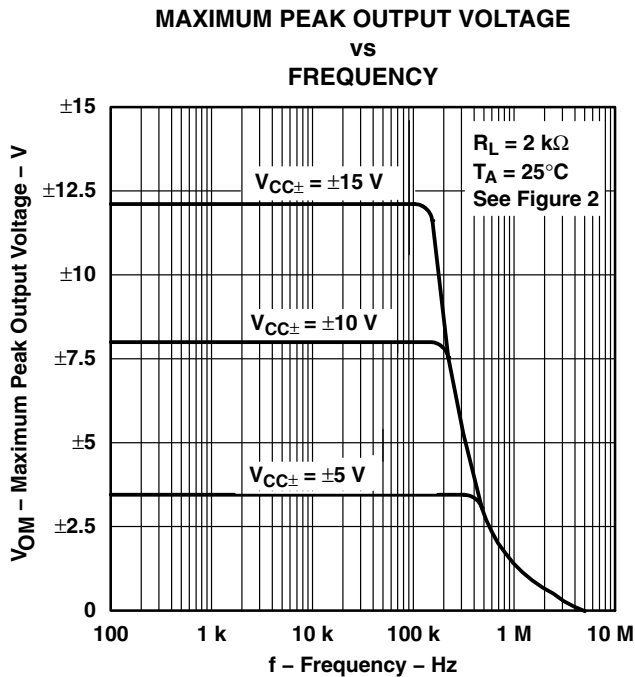


Figure 6

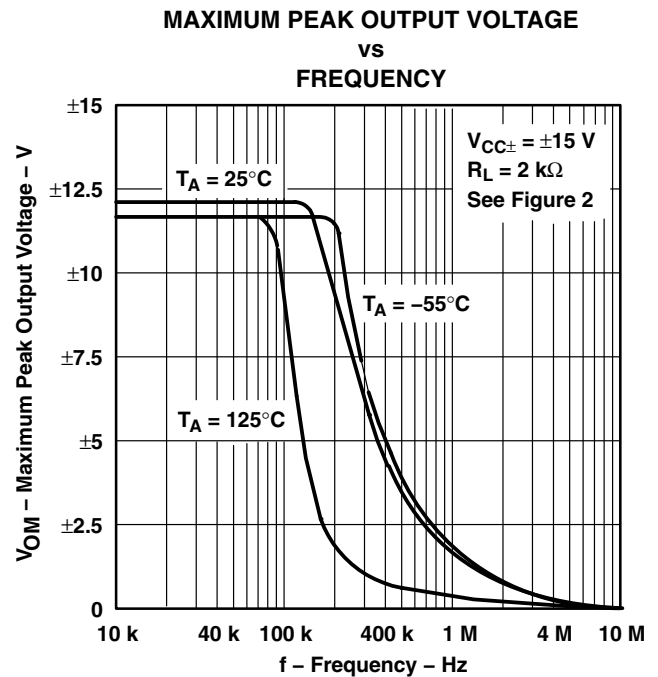


Figure 7

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

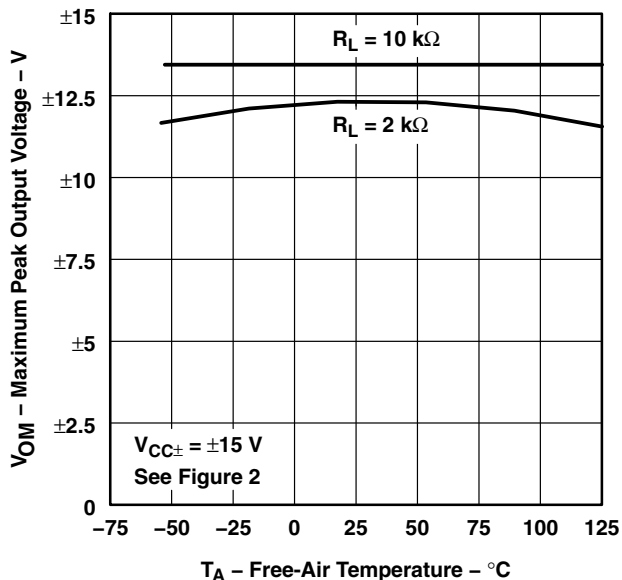


**TL071, TL071A, TL071B, TL072  
TL072A, TL072B, TL074, TL074A, TL074B  
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS**

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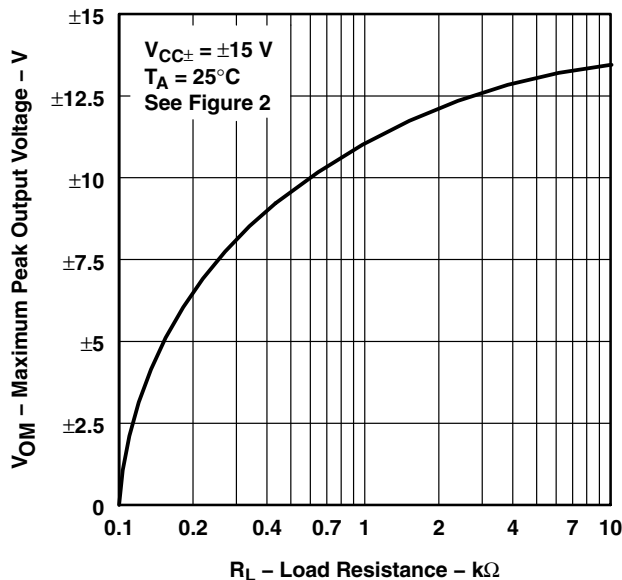
**TYPICAL CHARACTERISTICS†**

**MAXIMUM PEAK OUTPUT VOLTAGE  
vs  
FREE-AIR TEMPERATURE**



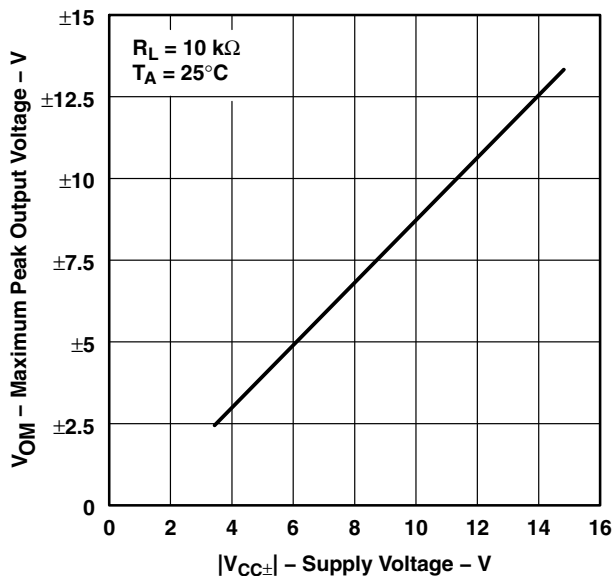
**Figure 8**

**MAXIMUM PEAK OUTPUT VOLTAGE  
vs  
LOAD RESISTANCE**



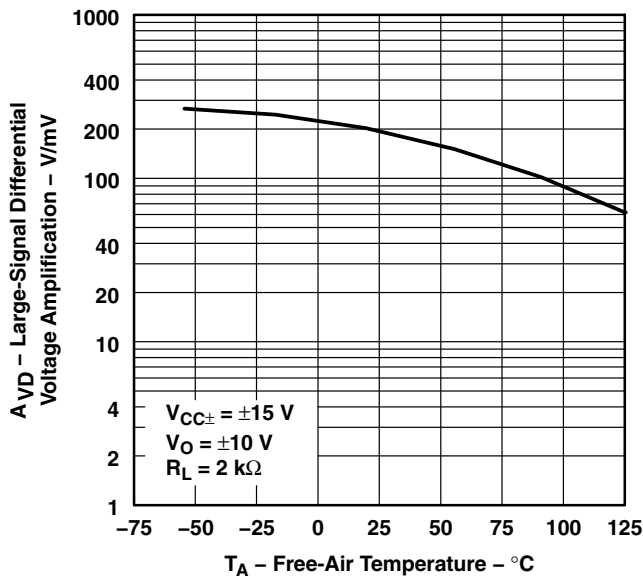
**Figure 9**

**MAXIMUM PEAK OUTPUT VOLTAGE  
vs  
SUPPLY VOLTAGE**



**Figure 10**

**LARGE-SIGNAL  
DIFFERENTIAL VOLTAGE AMPLIFICATION  
vs  
FREE-AIR TEMPERATURE**



**Figure 11**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS†

LARGE-SIGNAL  
 DIFFERENTIAL VOLTAGE AMPLIFICATION  
 AND PHASE SHIFT  
 vs  
 FREQUENCY

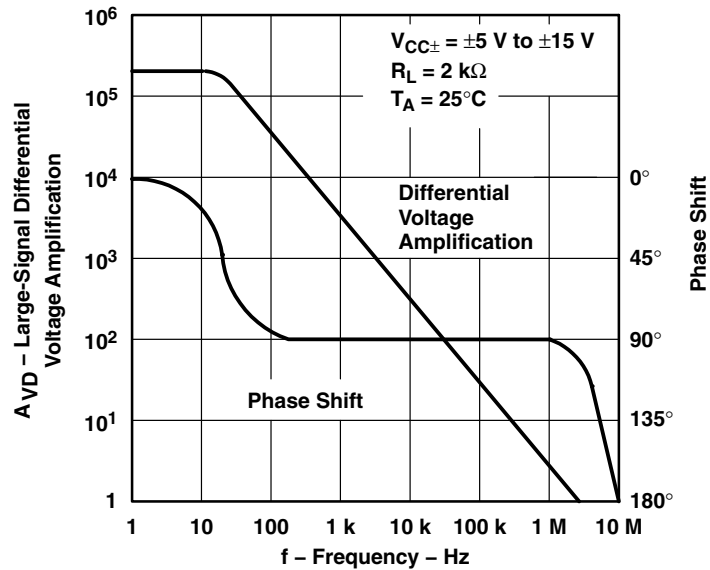


Figure 12

NORMALIZED UNITY-GAIN BANDWIDTH  
 AND PHASE SHIFT  
 vs  
 FREE-AIR TEMPERATURE

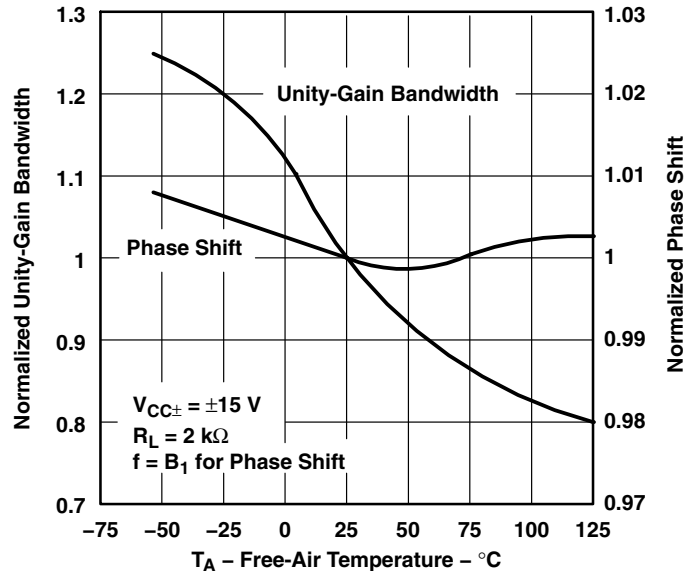


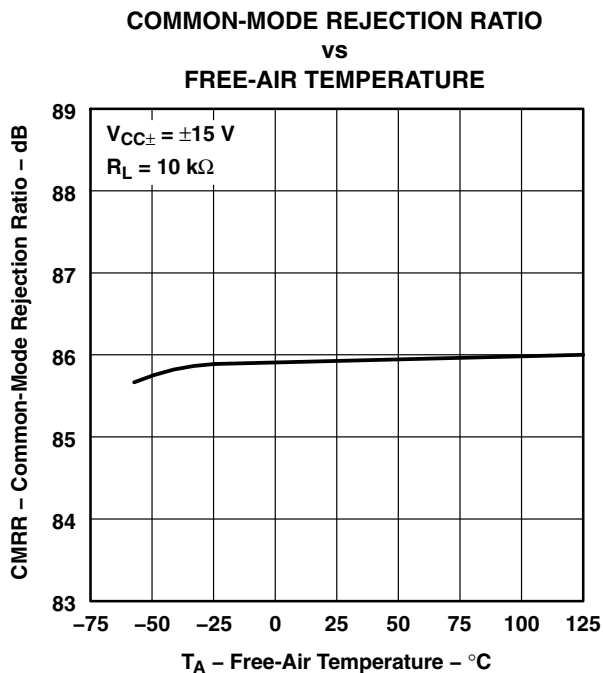
Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

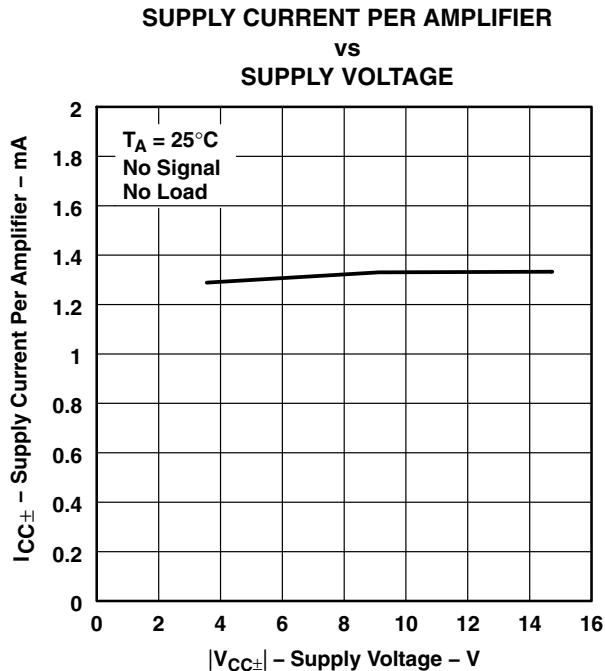
**TL071, TL071A, TL071B, TL072  
TL072A, TL072B, TL074, TL074A, TL074B  
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS**

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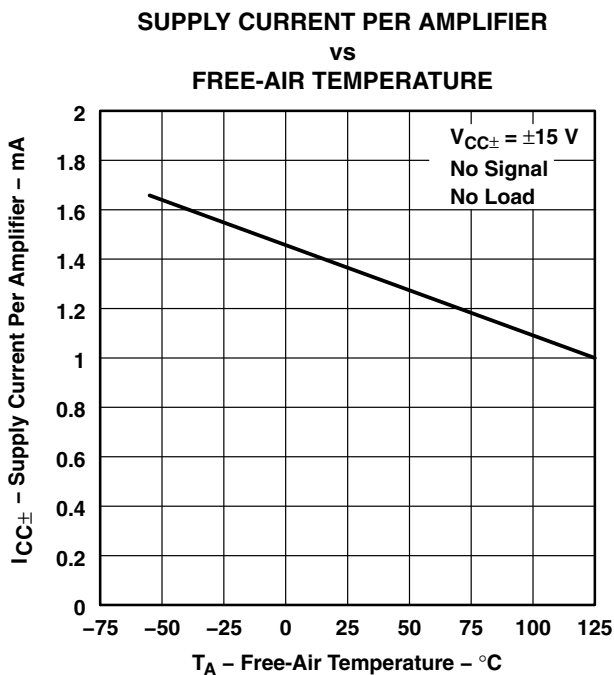
**TYPICAL CHARACTERISTICS†**



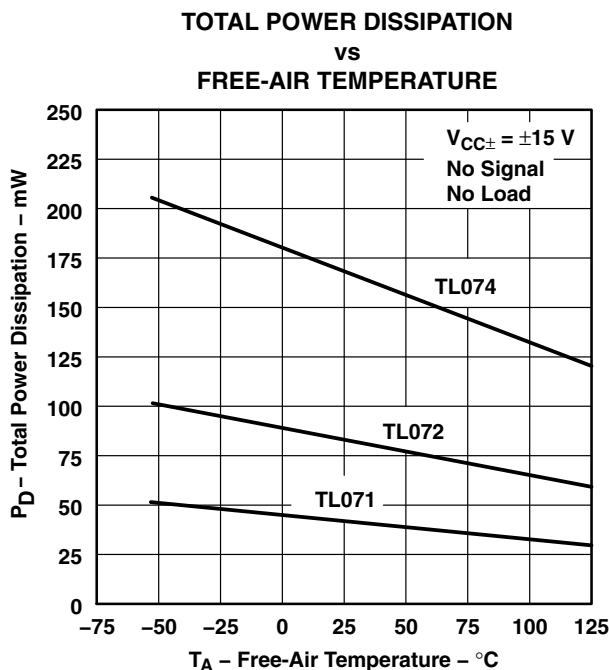
**Figure 14**



**Figure 15**



**Figure 16**



**Figure 17**

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



TYPICAL CHARACTERISTICS

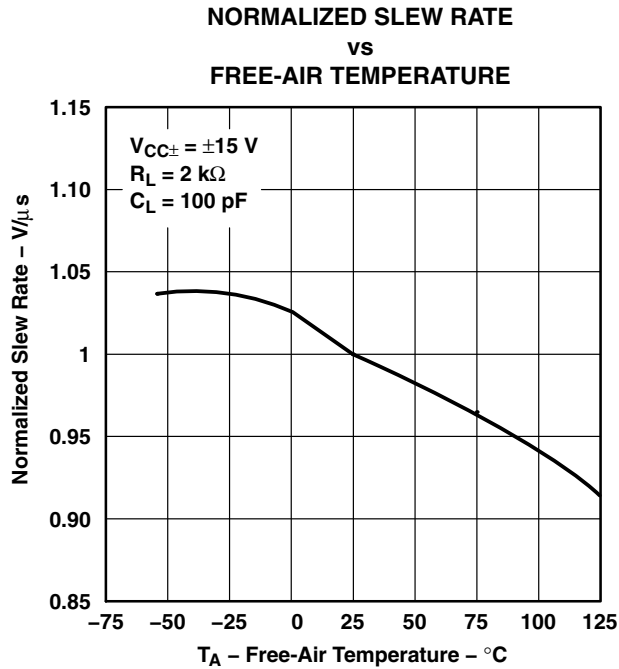


Figure 18

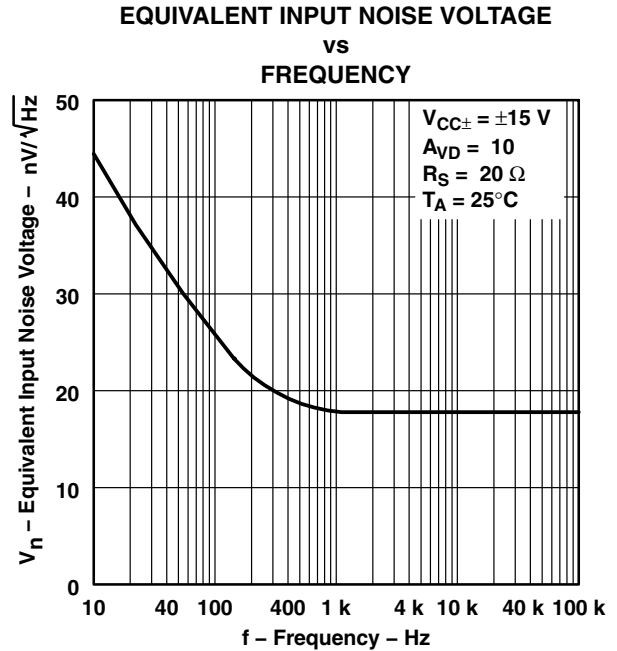


Figure 19

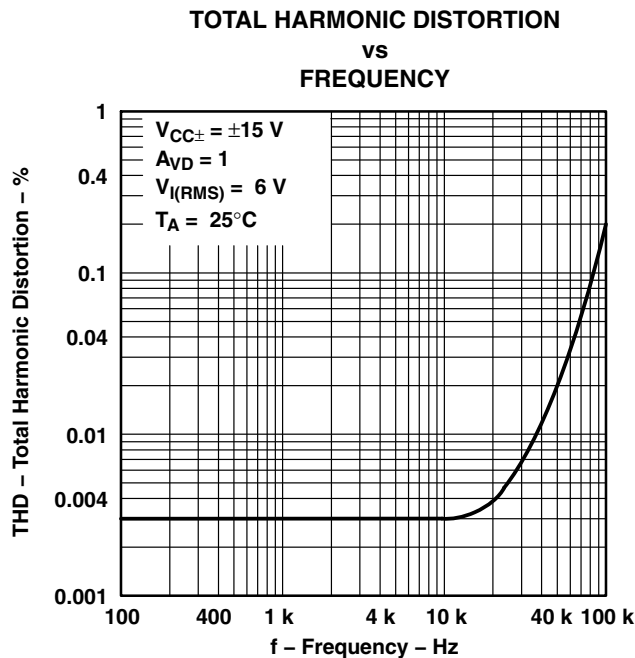


Figure 20

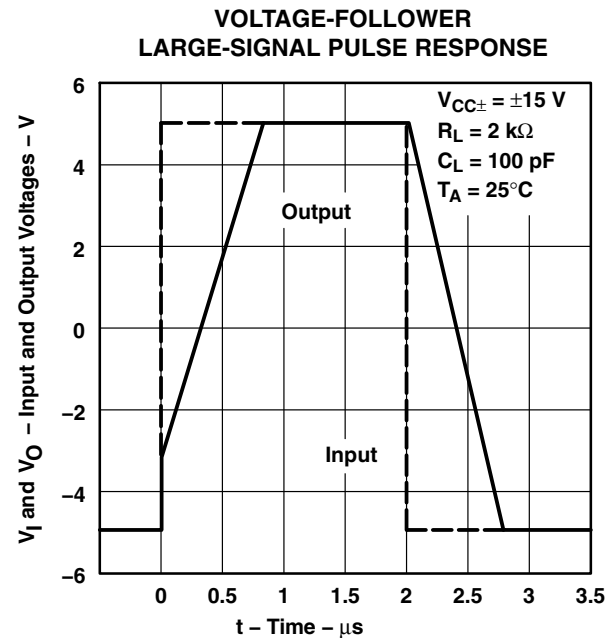


Figure 21

TYPICAL CHARACTERISTICS

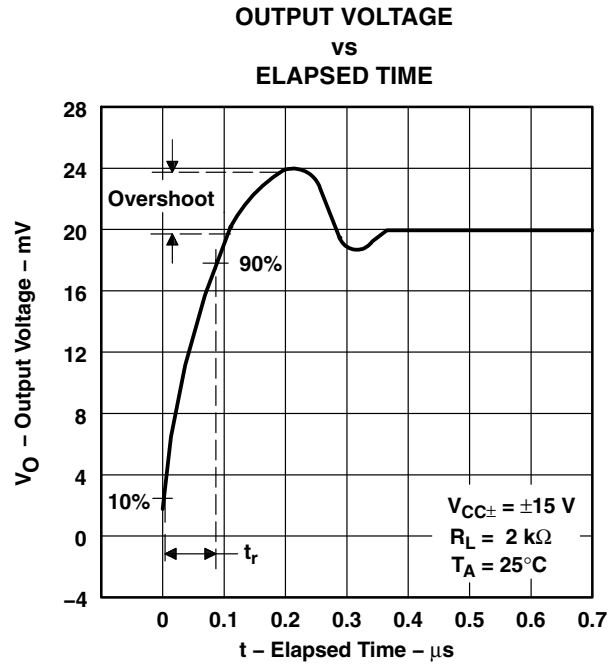


Figure 22



APPLICATION INFORMATION

Table of Application Diagrams

APPLICATION DIAGRAM	PART NUMBER	FIGURE
0.5-Hz square-wave oscillator	TL071	23
High-Q notch filter	TL071	24
Audio-distribution amplifier	TL074	25
100-kHz quadrature oscillator	TL072	26
AC amplifier	TL071	27

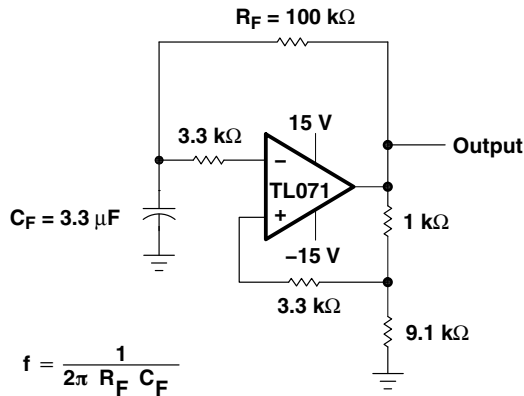


Figure 23. 0.5-Hz Square-Wave Oscillator

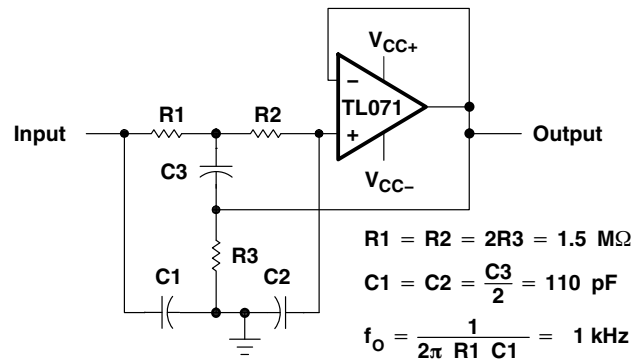


Figure 24. High-Q Notch Filter

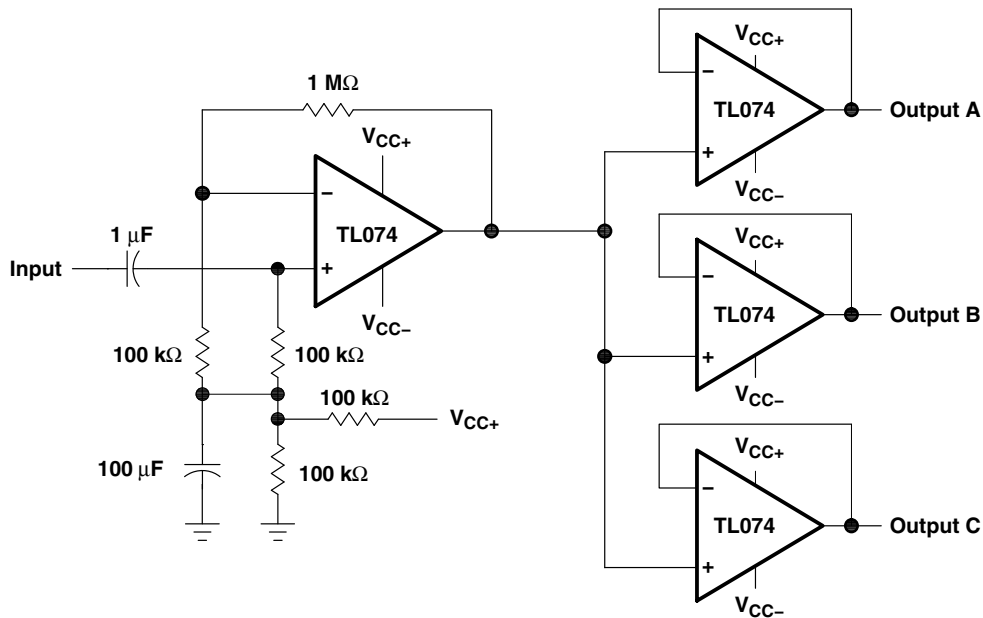
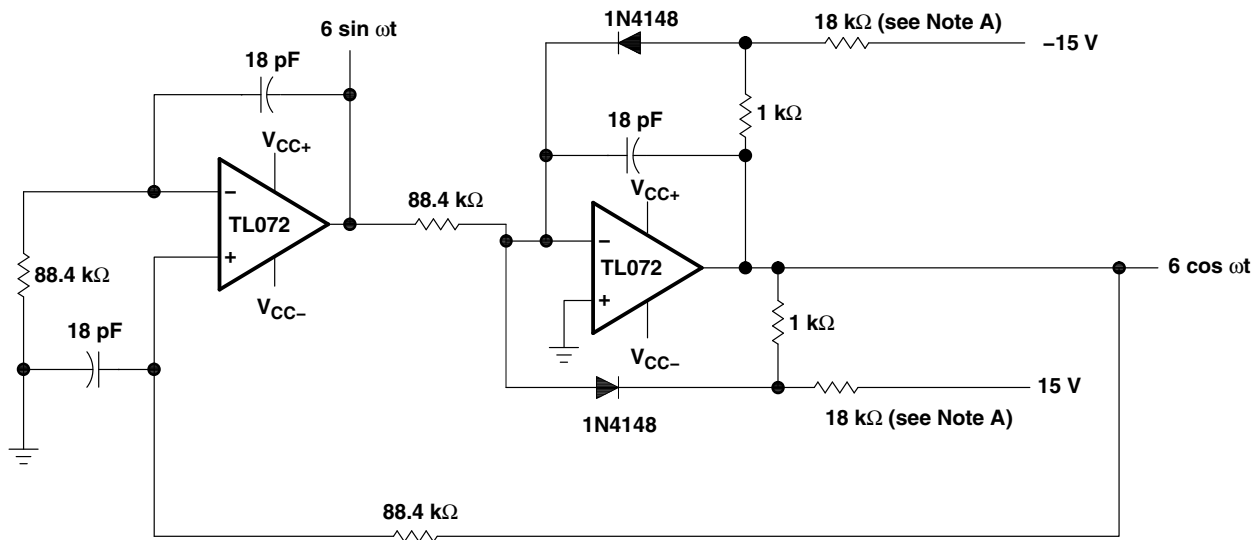


Figure 25. Audio-Distribution Amplifier

**TL071, TL071A, TL071B, TL072**  
**TL072A, TL072B, TL074, TL074A, TL074B**  
**LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS**

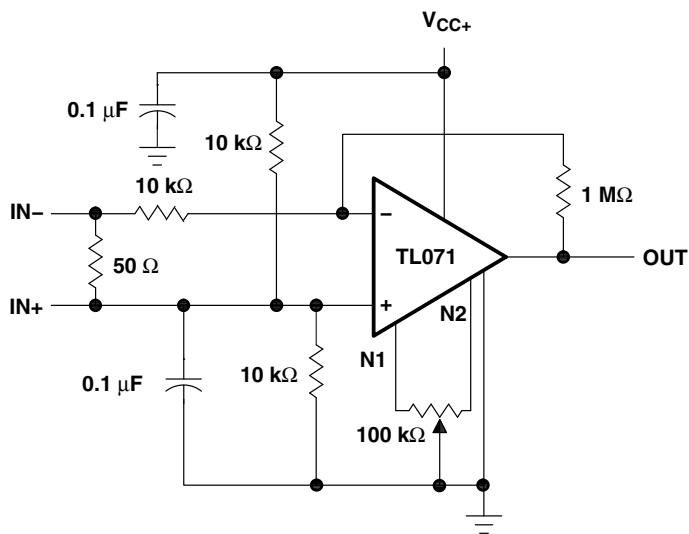
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**APPLICATION INFORMATION**



NOTE A: These resistor values may be adjusted for a symmetrical output.

**Figure 26. 100-kHz Quadrature Oscillator**



**Figure 27. AC Amplifier**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
8102304HA	OBSOLETE			10		TBD	Call TI	Call TI	
81023052A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
8102305HA	ACTIVE	CFP	U	10	1	TBD	Call TI	Call TI	
8102305PA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
81023062A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
8102306CA	ACTIVE	CDIP	J	14	1	TBD	Call TI	Call TI	
8102306DA	ACTIVE	CFP	W	14	1	TBD	Call TI	Call TI	
JM38510/11905BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
JM38510/11906BCA	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
M38510/11905BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
TL071ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL071ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL071BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TL071BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL071BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL071CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL071CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL071CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	
TL071ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TL071IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL071IJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
TL071IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL071IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL071MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	
TL071MJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
TL071MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
TL072ACD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072ACDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072ACDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072ACDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072ACDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072ACDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072ACJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
TL072ACP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL072ACPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TL072ACPSRE4	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI	
TL072ACPSRG4	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI	
TL072BCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072BCDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072BCDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072BCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072BCDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072BCDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072BCP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL072BCPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL072CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL072CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL072CPSLE	OBSOLETE	SO	PS	8		TBD	Call TI	Call TI	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TL072CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072CPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL072IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL072IPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL072MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TL072MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
TL072MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
TL072MUB	ACTIVE	CFP	U	10	1	TBD	A42	N / A for Pkg Type	
TL074ACD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TL074ACDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074ACDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074ACDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074ACDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074ACDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074ACJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
TL074ACN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL074ACNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL074ACNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074ACNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074ACNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074BCD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074BCDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074BCDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074BCDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074BCDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074BCDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074BCN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TL074BCNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL074CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074CDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074CDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL074CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL074CNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074CNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074CNSRG4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074CPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074CPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074CPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074CPWLE	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	
TL074CPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074CPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TL074CPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TL074IJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	
TL074IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL074INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TL074MFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TL074MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TL074MJ	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
TL074MJB	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	
TL074MWB	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TL072, TL072M, TL074, TL074M :**

- Catalog: [TL072](#), [TL074](#)
- Enhanced Product: [TL072-EP](#), [TL072-EP](#), [TL074-EP](#), [TL074-EP](#)
- Military: [TL072M](#), [TL074M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION



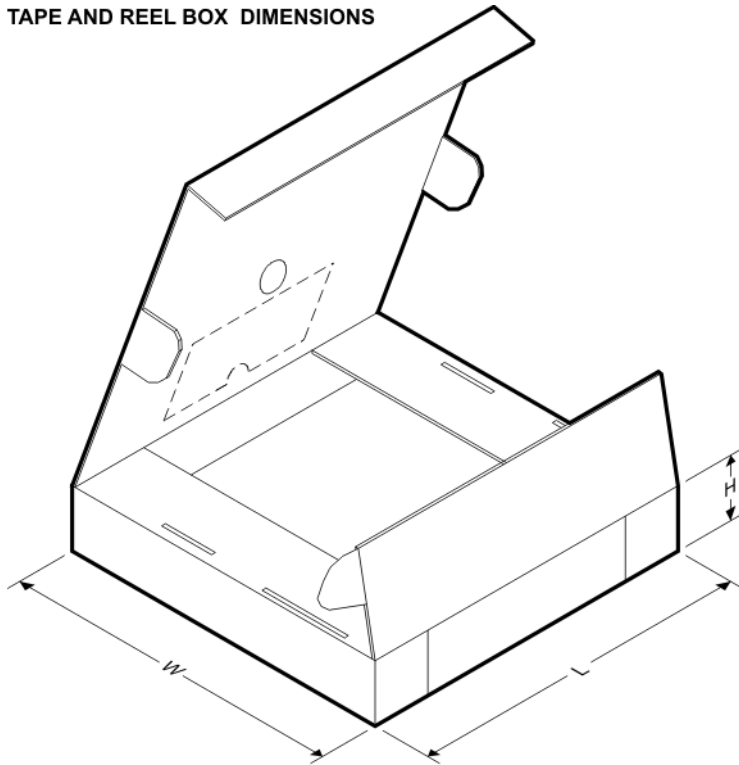
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL071ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL071IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL072CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL074ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074ACNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL074BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL074CPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL074IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

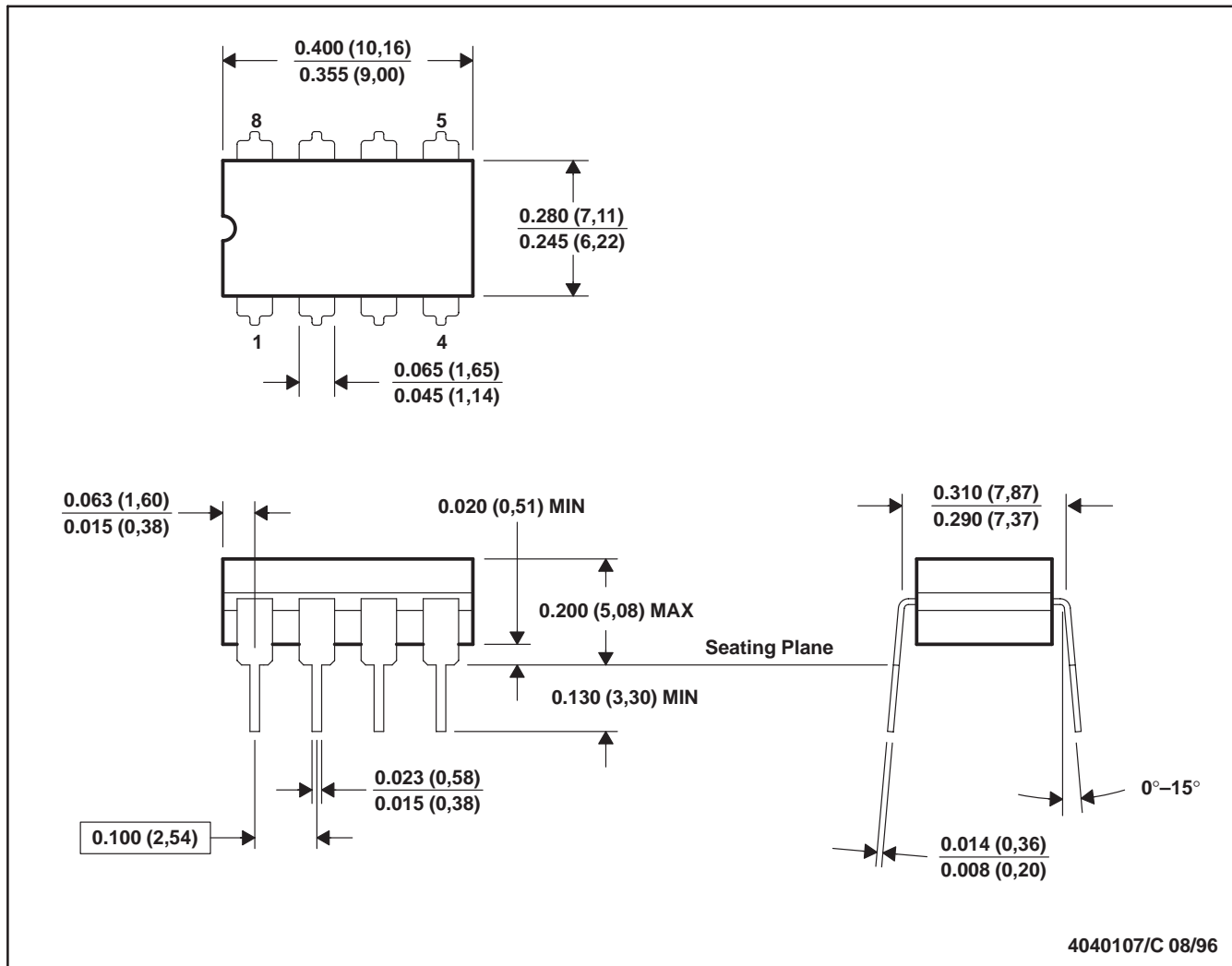
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL071ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071CDR	SOIC	D	8	2500	340.5	338.1	20.6
TL071CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL071CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL071IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072ACDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072BCDR	SOIC	D	8	2500	340.5	338.1	20.6
TL072CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL072CPSR	SO	PS	8	2000	367.0	367.0	38.0
TL072CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL072IDR	SOIC	D	8	2500	340.5	338.1	20.6
TL074ACDR	SOIC	D	14	2500	333.2	345.9	28.6
TL074ACNSR	SO	NS	14	2000	367.0	367.0	38.0
TL074BCDR	SOIC	D	14	2500	333.2	345.9	28.6
TL074CDR	SOIC	D	14	2500	333.2	345.9	28.6

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Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL074CNSR	SO	NS	14	2000	367.0	367.0	38.0
TL074CPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TL074IDR	SOIC	D	14	2500	333.2	345.9	28.6

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



4040107/C 08/96

- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification.  
 E. Falls within MIL STD 1835 GDIP1-T8

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



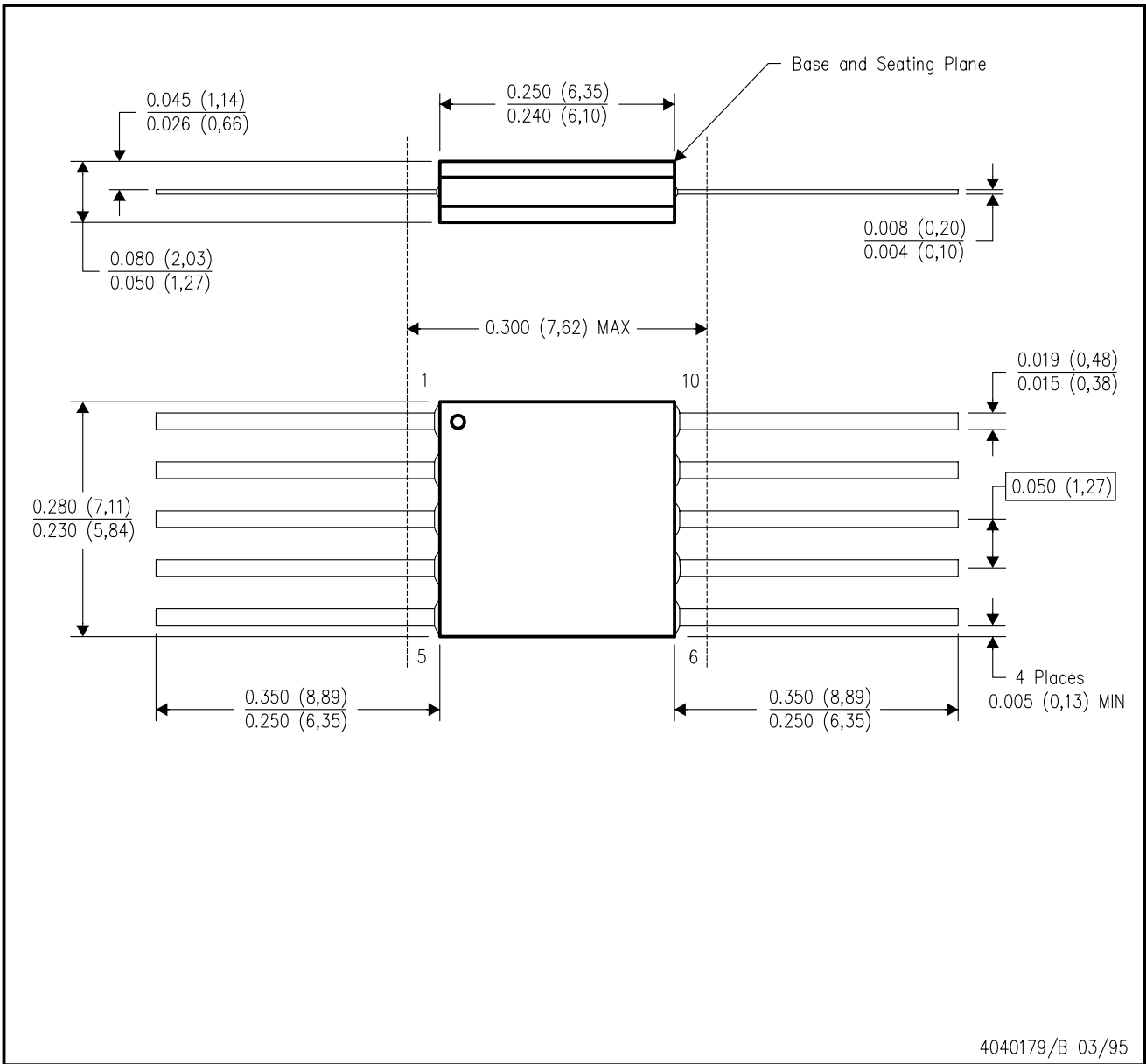
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



U (S-GDFP-F10)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14 and JEDEC MO-092AB

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

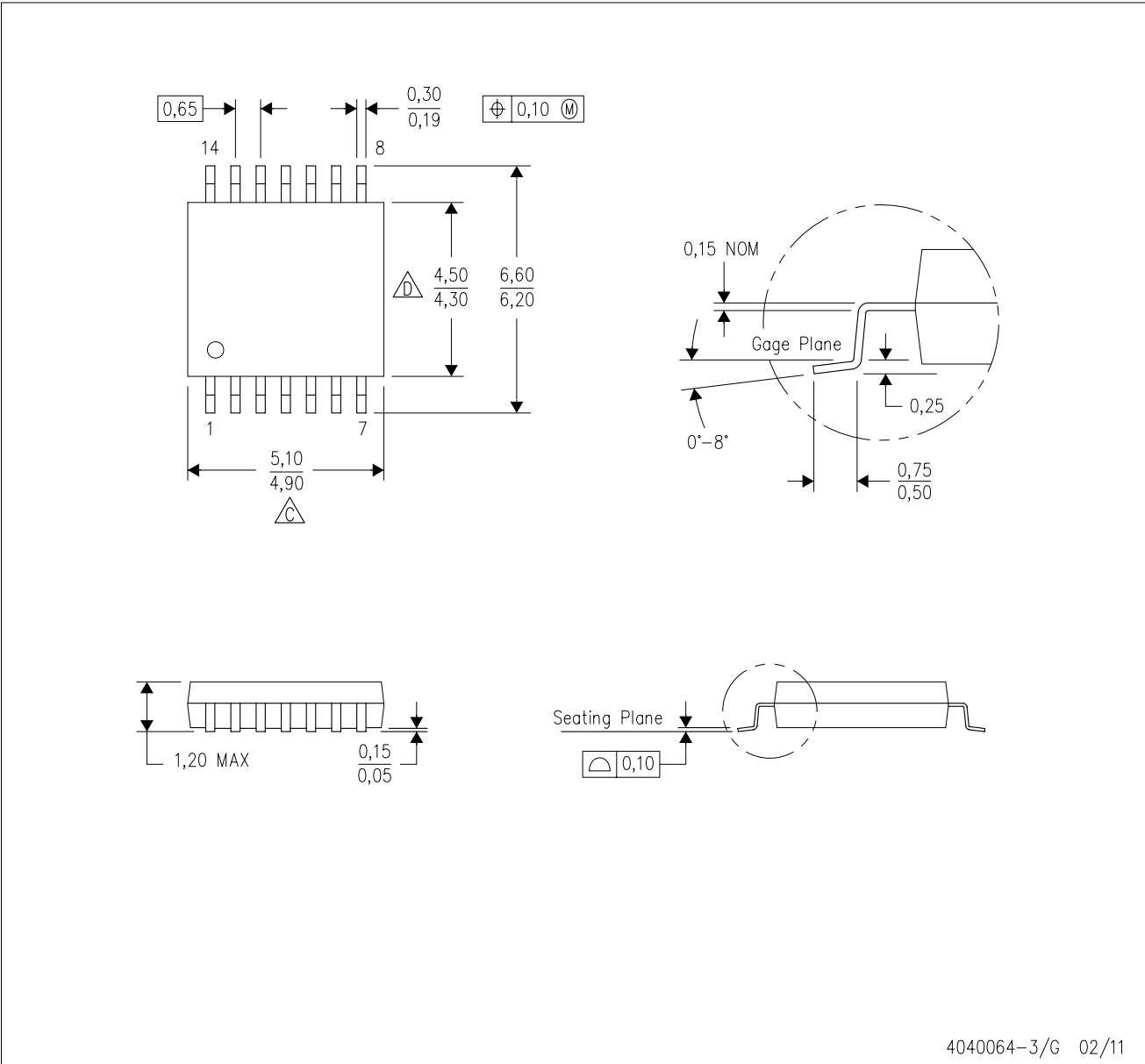


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



**MECHANICAL DATA**

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



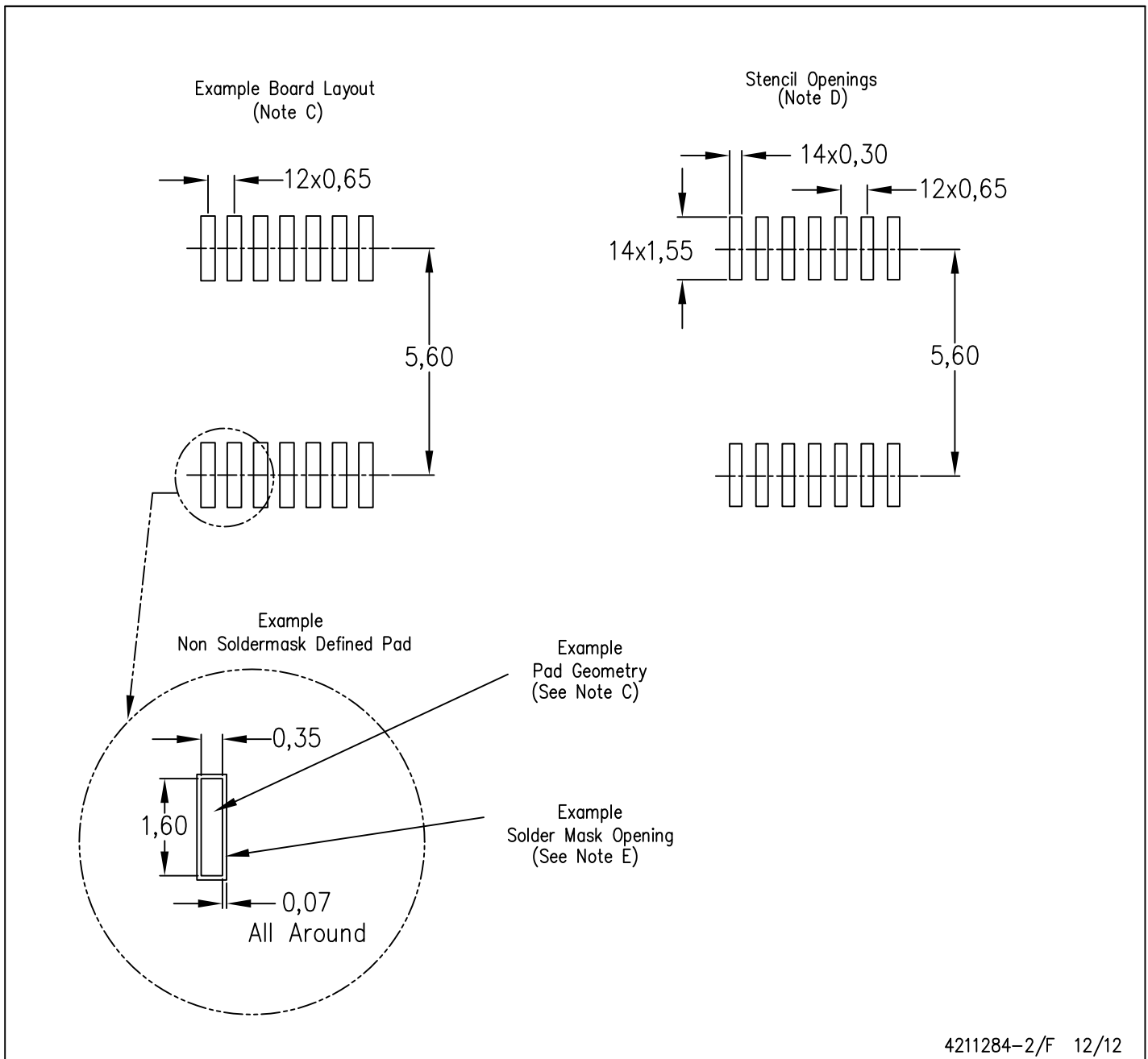
4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153



PW (R-PDSO-G14)

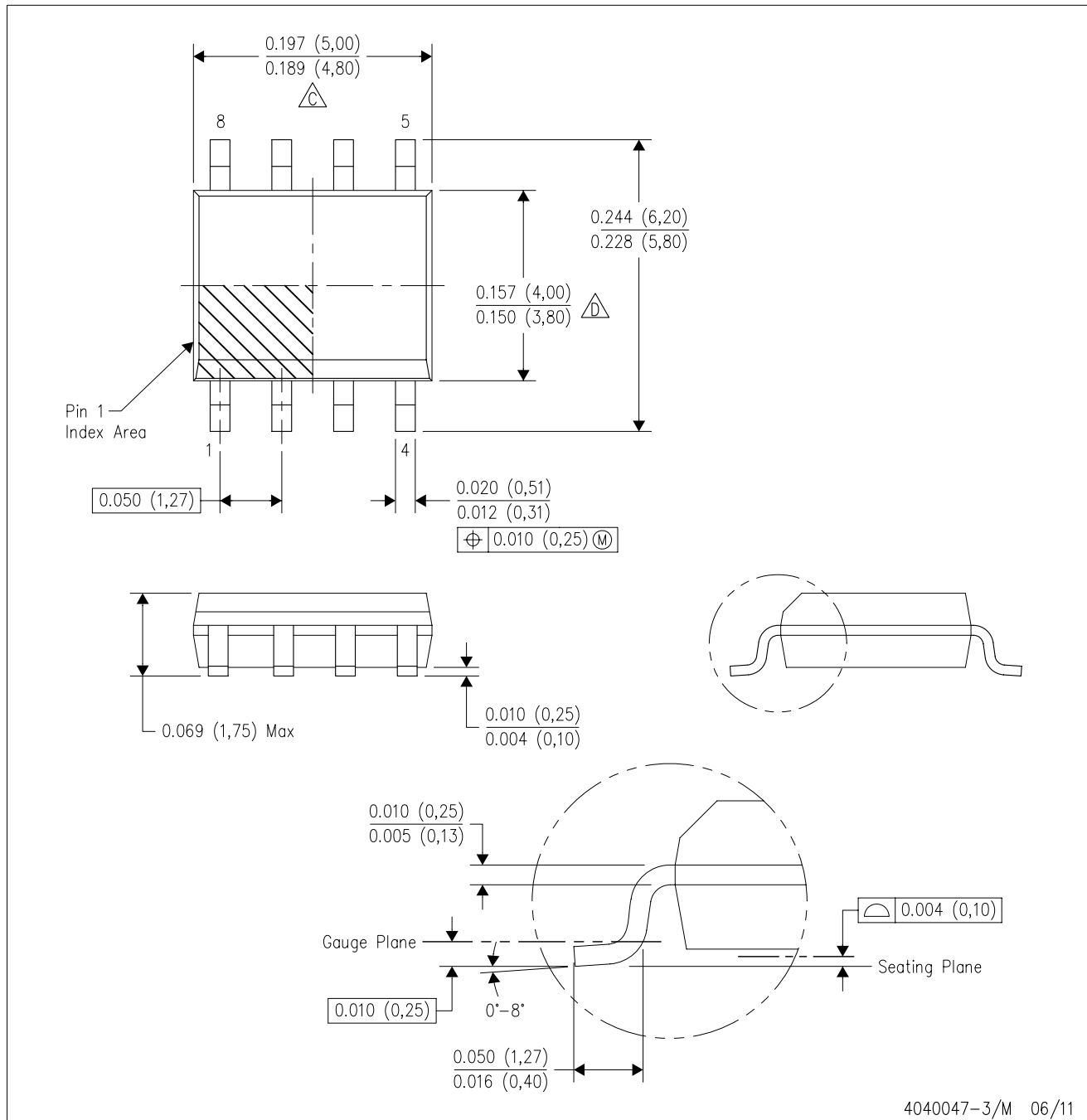
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

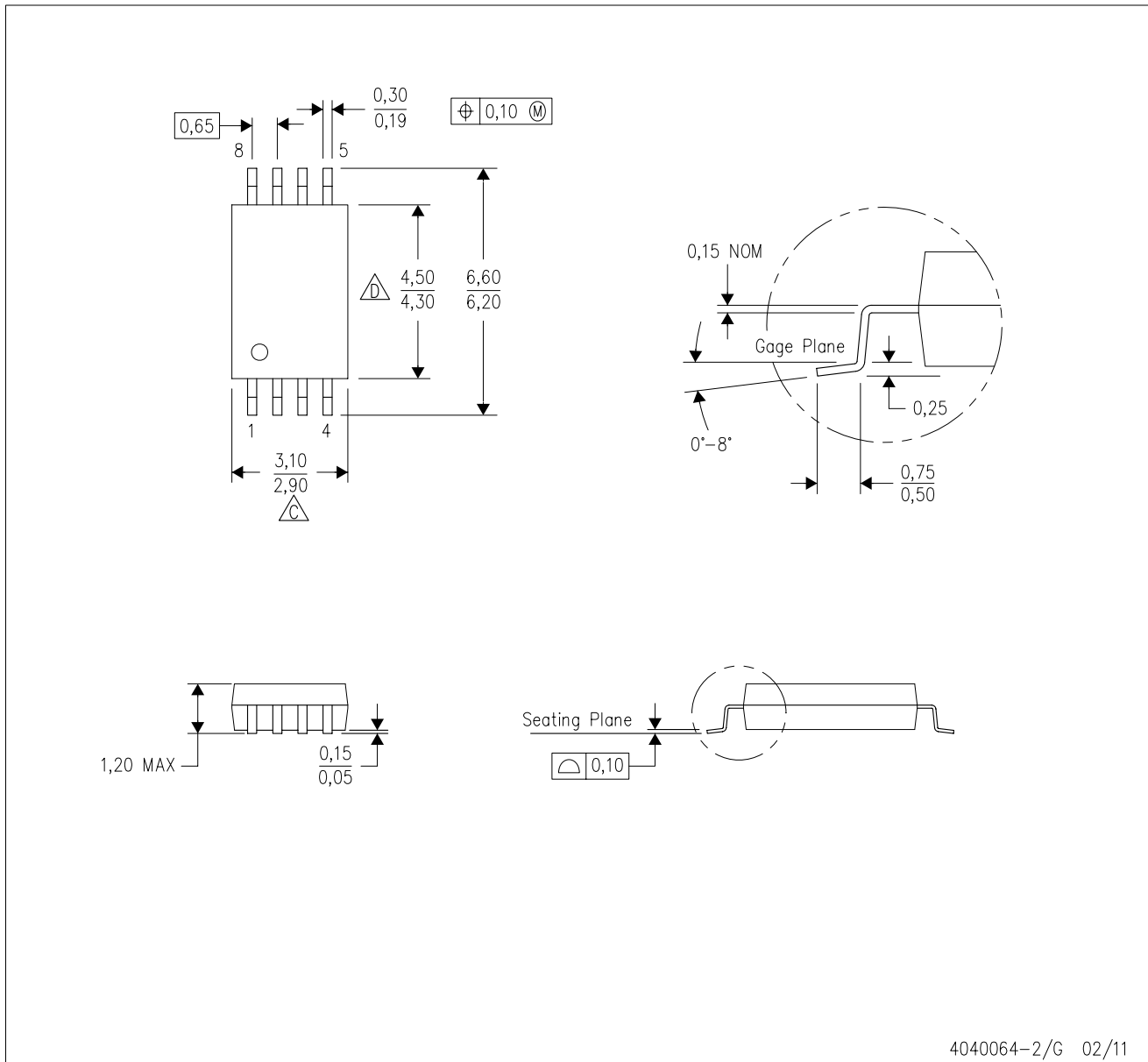
14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040064-2/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

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