



## Features 深圳市俊达微电子 13530777233

- ESD Protect for 1 Line with Bi-directional
- Provide ESD protection for the protected line to  
IEC 61000-4-2 (ESD)  $\pm 15\text{kV}$  (air/contact)  
IEC 61000-4-4 (EFT) 50A (5/50ns)  
IEC 61000-4-5 (Lightning) 5A (8/20 $\mu\text{s}$ )  
Cable Discharge Event (CDE)
- **0402 small DFN package** saves board space
- Protect one I/O line or one power line
- Fast turn-on and Low clamping voltage
- For low operating voltage applications: 3.3V maximum
- Solid-state silicon-avalanche and active circuit triggering technology
- Green part

## Applications

- Mobile Phones
- Hand Held Portable Applications
- Computer Interfaces Protection
- Microprocessors Protection
- Serial and Parallel Ports Protection
- Control Signal Lines Protection
- Power lines on PCB Protection
- Latchup Protection

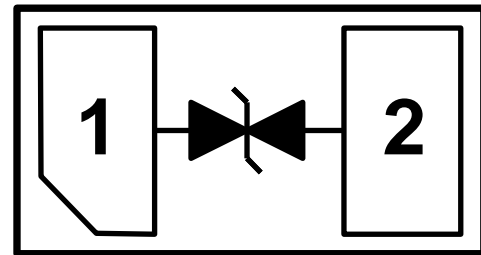
## Description

AZ5123-01J is a design which includes one Bi-directional surge rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic systems. The AZ5123-01J has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

AZ5123-01J is a unique design which includes proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ5123-01J may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ( $\pm 15\text{kV}$  air,  $\pm 8\text{kV}$  contact discharge)

## Circuit Diagram / Pin Configuration



**DFN1006P2X (Bottom View)**  
**(1.0mm x 0.6mm x 0.45mm)**



## SPECIFICATIONS

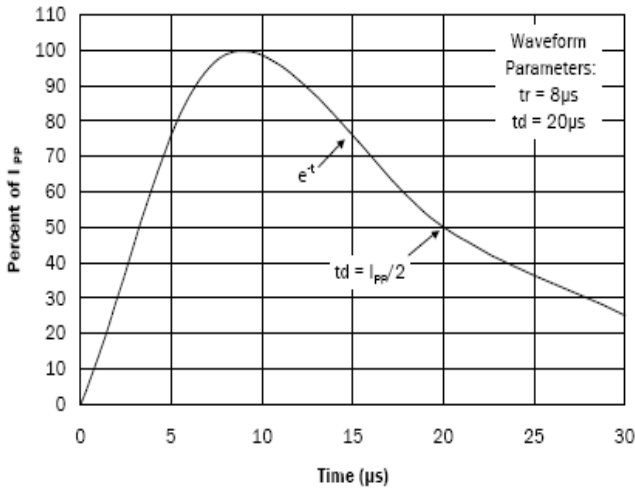
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	PARAMETER	RATING	UNITS
Peak Pulse Current (tp=8/20us)	I <sub>PP</sub>	5	A
Operating Supply Voltage	V <sub>DC</sub>	±3.6	V
ESD per IEC 61000-4-2 (Air)	V <sub>ESD</sub>	±15	kV
ESD per IEC 61000-4-2 (Contact)		±15	
Lead Soldering Temperature	T <sub>SOL</sub>	260 (10sec.)	°C
Operating Temperature	T <sub>OP</sub>	-55to+85	°C
Storage Temperature	T <sub>STO</sub>	-55to+150	°C

ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MINI	TYP	MAX	UNITS
Stand-Off Voltage	V <sub>RWM</sub>	T=25°C.	-3.3		3.3	V
Leakage Current	I <sub>Leak</sub>	V <sub>RWM</sub> =±3.3V, T=25°C.			1.0	μA
Breakdown Voltage	V <sub>BV</sub>	I <sub>BV</sub> =1mA, T=25°C.	4		6.5	V
Surge Clamping Voltage	V <sub>surge_CL</sub>	I <sub>PP</sub> =5A, tp=8/20μs, T=25°C.		6.5	8	V
ESD Clamping Voltage	V <sub>ESD_CL</sub>	IEC 61000-4-2 +6kV, T=25°C, Contact mode.		7		V
Channel Input Capacitance	C <sub>IN</sub>	V <sub>R</sub> =0V, f=1MHz, T=25°C.		13.5	16.5	pF

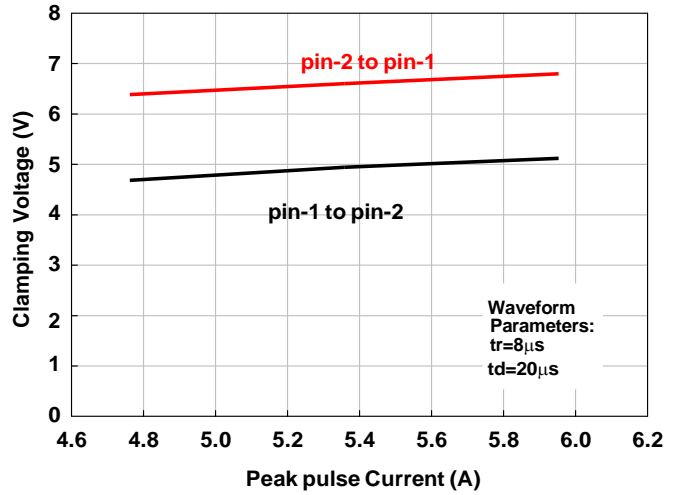


## Typical Characteristics

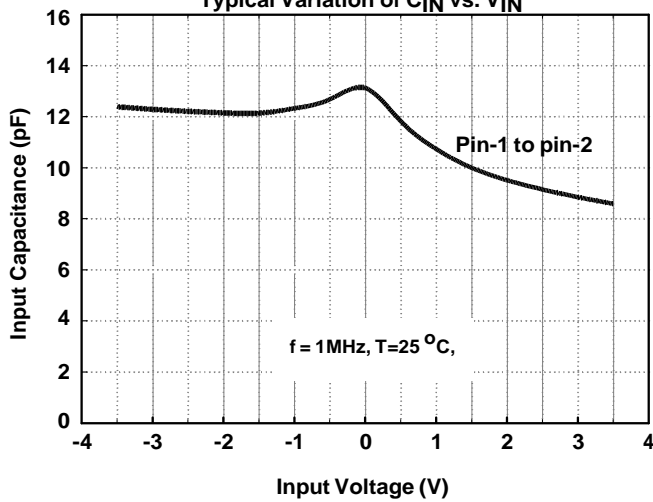
Pulse Waveform



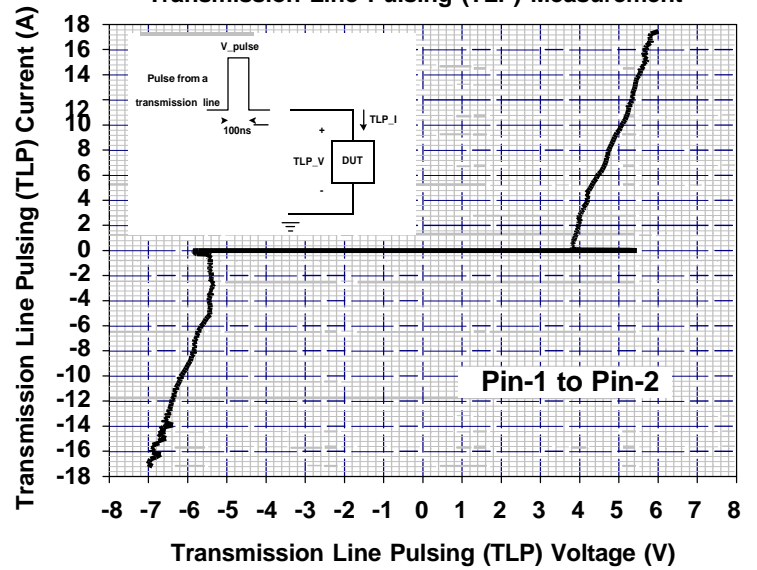
Clamping Voltage vs. Peak Pulse Current



Typical Variation of  $C_{IN}$  vs.  $V_{IN}$



Transmission Line Pulsing (TLP) Measurement



## Applications Information

The AZ5123-01J is designed to protect one line against System ESD/EFT/Lightning pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ5123-01J is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5123-01J should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5123-01J.
- Place the AZ5123-01J near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

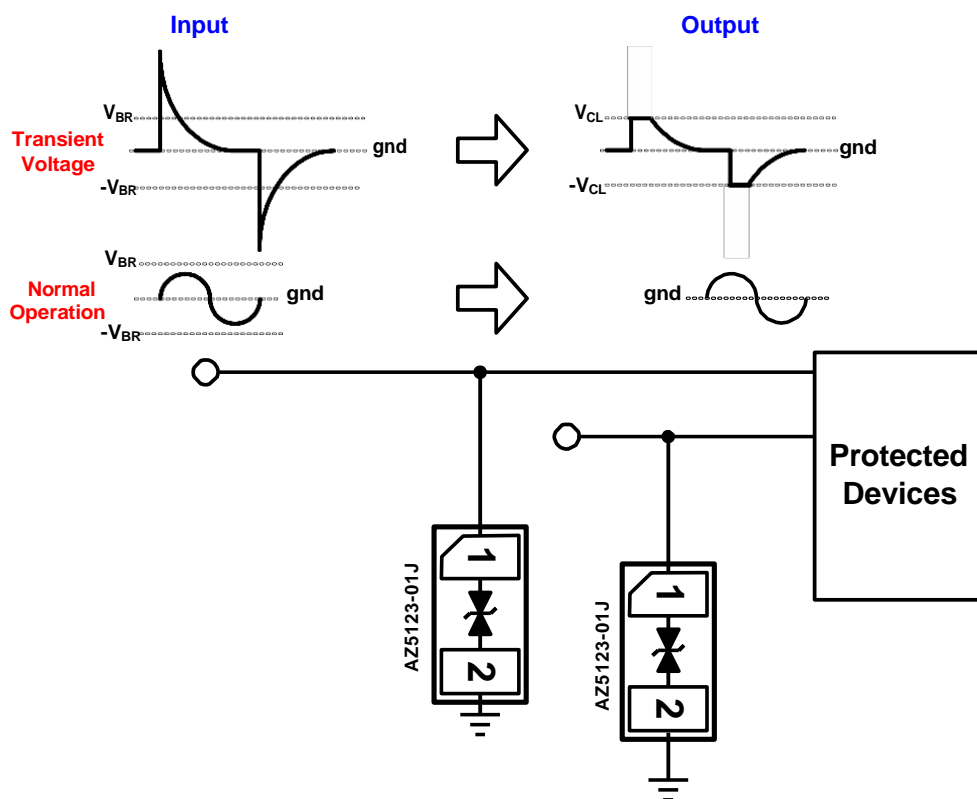


Fig. 1

Fig. 2 shows another simplified example of using AZ5123-01J to protect the control line, low speed data line, and power line from ESD transient stress.

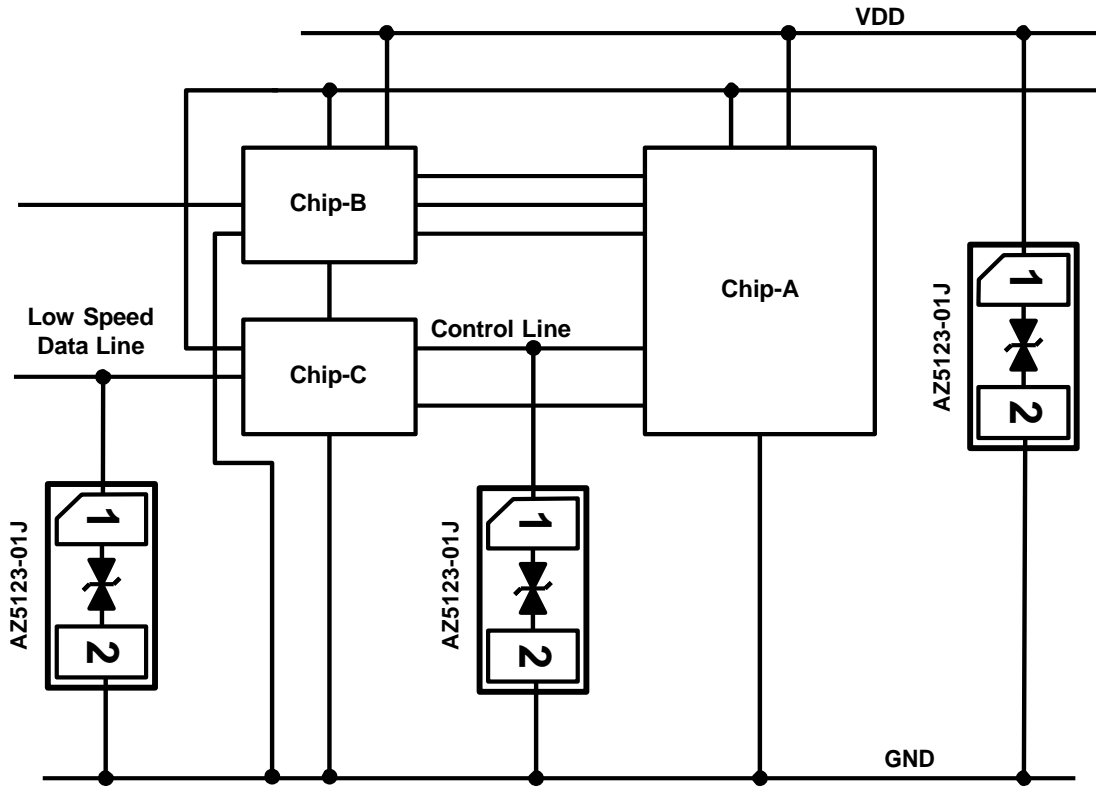


Fig. 2

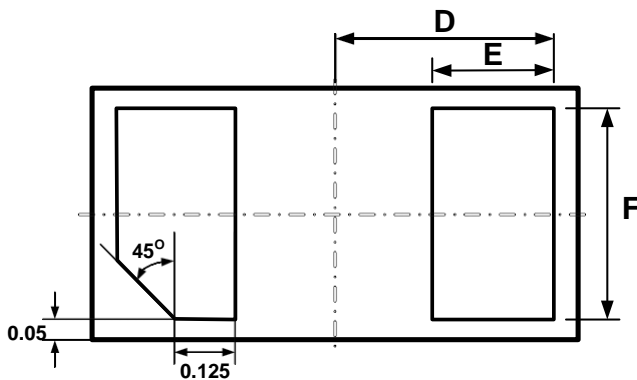


## Mechanical Details

### DFN1006P2X PACKAGE DIAGRAMS



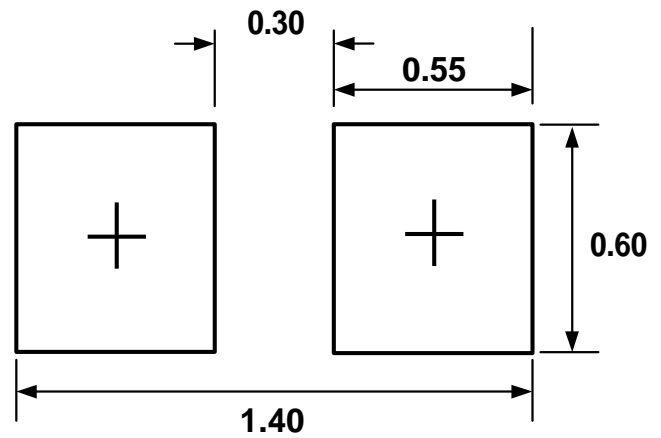
TOP VIEW



BOTTOM VIEW

Symbol	Millimeters		Inches	
	min	max	min	max
A	0.95	1.05	0.037	0.041
B	0.55	0.65	0.022	0.026
C	0.41	0.50	0.016	0.020
D	0.45		0.018	
E	0.20	0.30	0.008	0.012
F	0.45	0.55	0.018	0.022

## LAND LAYOUT

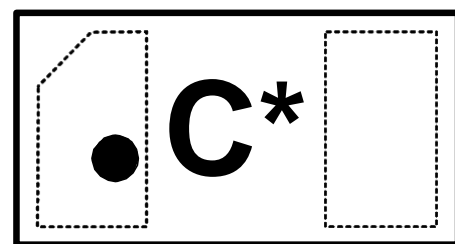


(Unit: mm)

Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

## MARKING CODE



Top View

\* = Month  
C = Deviccode

Part Number	Marking Code
AZ5123-01J	C



## Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ5123-01J.R7G	Green	T/R	7 inch	20,000/reel	4 reel= 80,000/box	6 box =480,000/carton

## Revision History

Revision	Modification Description
Revision 2011/11/09	Formal Release.
Revision 2012/01/18	Add the Ordering Information.