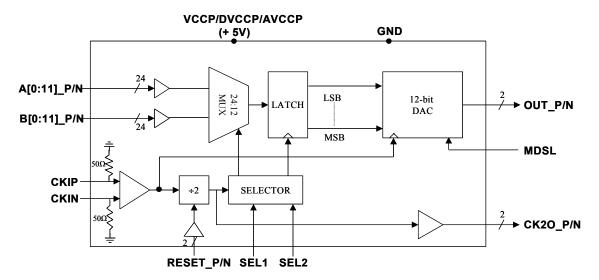
## MD622P - High Speed > 4Gsps MUXDAC



## **Key Features**

- 12-bit resolution DAC with > 4-GSPS rate
- DAC analog output format can be selected between Normal-Hold (NH) mode or Return-to-Zero (RZ) mode
- 2:1 multiplexing ratio for each input bit of DAC
- SFDR better than -50 dBc
- Complementary outputs with  $50-\Omega$  back terminations
- Complementary divided-by-2 LVDS outputs for data synchronization
- Variable 400~800 mV<sub>PP</sub> single-ended output swing
- On-chip 100 ohm termination between each differential LVDS input data and RESET pair
- QFN 10x10 88L package with exposed pad
- Single power supply +5V with 2.3 W power consumption

## **Applications**

- Arbitrary waveform generation
- Radar/Ladar design and testing
- Software defined radio
- Electronic warfare
- Wireless basestations
- RF signal source generation
- Hard disk and magnetic storage testing
- WLAN testing
- Advanced communication modulations

## **Description**

**MD622P** is a high-speed 12-bit Digital to Analog Converter (DAC) integrated with a 24:12 (12 channels of 2:1) input multiplexer. The converter can be operated at a sampling rate up to 4.5 Gsps. The digital data inputs are LVDS with on-chip 100 ohm termination resistors. After the 48 pairs of differential data inputs were multiplexed up to 2 times of speed, the 12 high speed data bits are latched and encoded to drive DAC output stage. The analog outputs of DAC can be selected between Normal-Hold mode (for the 1<sup>st</sup> Nyquist band) or Return-to-Zero mode (for the 1<sup>st</sup>, 2<sup>nd</sup> and 3<sup>rd</sup> Nyquist band) operation. Complementary outputs are available with 50-Ω output back terminations. Divided-by-4 clock LVDS outputs and sampling phase selection (SEL1 and SEL2) are provided to ease the alignment of sampling phase relative to the input data. Divided-by-2 clock LVDS outputs are also provided. A RESET function is provided for system applications which need to synchronize the outputs from multiple **MD622P**'s.