Version :0.1

TECHNICAL SPECIFICATION

MODEL NO. : PM058OX1

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Please contact EIH or its agent for further information.

☐Customer's Confirmation

Customer _____

By _____

☐EIH's Confirmation

Dep	FAE	Panel Design	Electronic Design	Mechanical Design	Product Verification	Prepared by
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Revision History

Rev.	Issued Date	Revised Contents
0.1	Feb. 15, 2011	Preliminary

TECHNICAL SPECIFICATION

CONTENTS

1. Application

This data sheet applies to a color TFT LCD module, PM058OX1. The module applies to OA product, GPS, which require high quality flat panel display. If you must use in high reliability environment, the module can't over reliability test condition. If you use PM058OX1, E Ink Holding Inc. advises your system sides must use NT71355 which one generates signal to control PM058OX1.

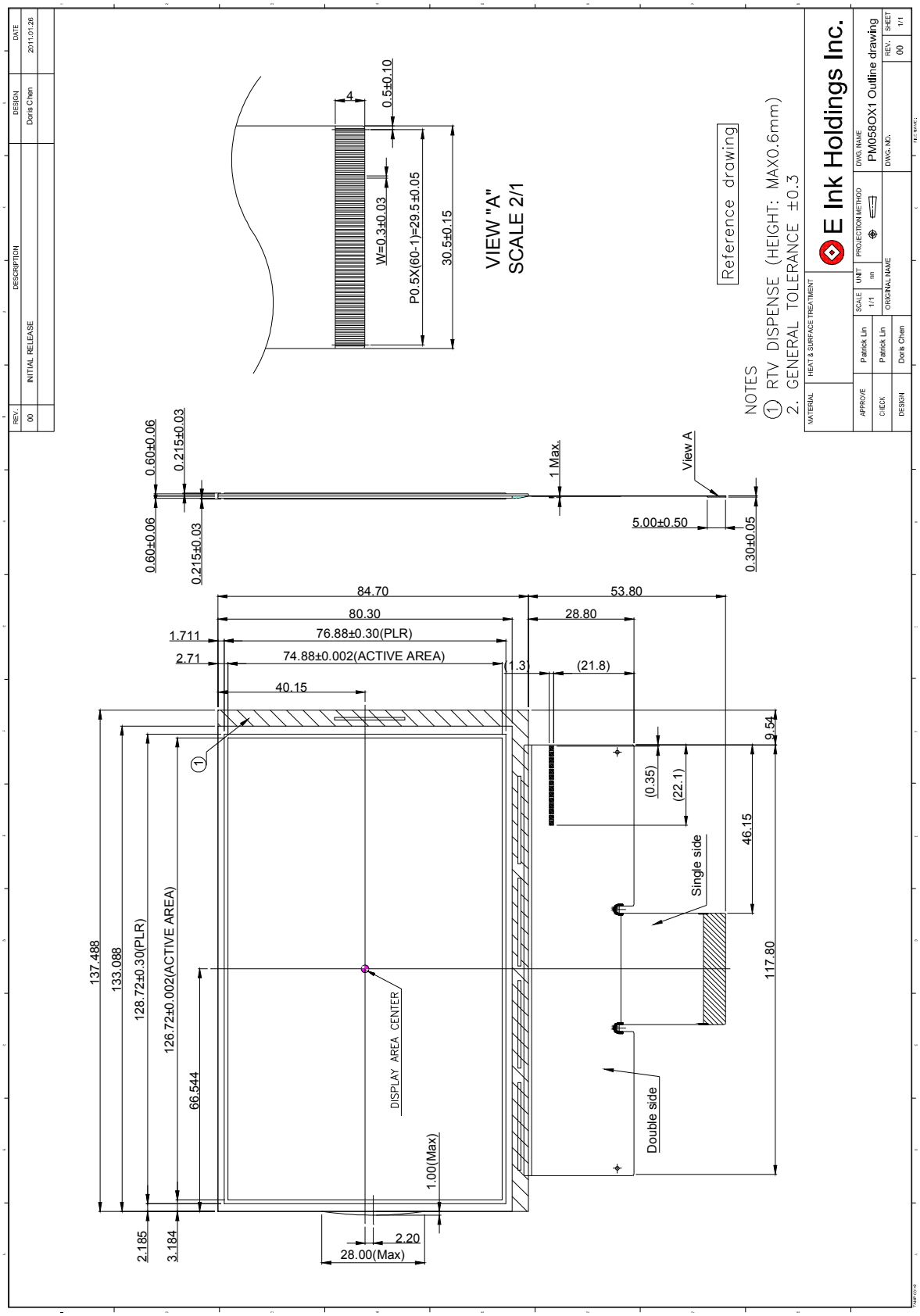
2. Features

. Amorphous silicon TFT LCD panel
. Pixel in stripe configuration
. Display Colors：262,144 colors
. Optimum Viewing Direction：6 o'clock

3. Mechanical Specifications

Parameter	Specifications	Unit
Screen Size	5.8(diagonal)	inch
Display Format	1280×(R, G, B)×768	dot
Display Colors	262,144	
Active Area	126.720(H)×74.880(V)	mm
Pixel Pitch	0.0990(H)×0.0975(V)	mm
Pixel Configuration	Stripe	
Outline Dimension	137.488(W)×84.700 (H)×1.630 (typ.) (D)	mm
Weight	TBD	g
Surface treatment	Normal	
Display mode	Normally White	
Gray scale inversion direction	6 o'clock [ref to Note13-1]	

4. Mechanical Drawing of TFT-LCD Module



5. Input / Output Terminals

TFT-LCD Panel Driving

in No.	Symbol	I/O	Function	Remark
1	VCOM	I	Common Voltage	
2	GND	I	Ground	
3	VCC	I	Voltage for digital circuit	
4	GND	I	Ground	
5	VEE	I	Gate Off Voltage	Note 5-2
6	GND	I	Ground	
7	VGG	I	Gate On Voltage	Note 5-1
8	GND	I	Ground	
9	STVD	I/O	Vertical Shift Pulse Signal Input or Output	Note 5-6
10	STVU	I/O	Vertical Shift Pulse Signal Input or Output	Note 5-6
11	CKV	I	Vertical Shift Clock	Note 5-4
12	UD	I	Up/Down Selection	Note 5-6
13	OE	I	Output Enable	Note 5-5
14	AVDD	I	Power Supply	
15	GND	I	Ground	
16	VDD	I	Voltage for analog circuit	
17	POL	I	Polarity selection	Note 5-9
18	REV	I	Data invert control	Note 5-8
19	LD	I	Load output signal	Note 5-7
20	GND	I	Ground	
21	V14	I	Gamma Voltage 14	Note 5-10
22	V13	I	Gamma Voltage 13	
23	V12	I	Gamma Voltage 12	
24	V11	I	Gamma Voltage 11	
25	V10	I	Gamma Voltage 10	
26	V9	I	Gamma Voltage 9	
27	V8	I	Gamma Voltage 8	
28	V7	I	Gamma Voltage 7	
29	V6	I	Gamma Voltage 6	
30	V5	I	Gamma Voltage 8	
31	V4	I	Gamma Voltage 4	
32	V3	I	Gamma Voltage 3	
33	V2	I	Gamma Voltage 2	
34	V1	I	Gamma Voltage 1	

35	GND	I	Ground	
36	MLV5N		Mini-LVDS data input	
37	MLV5P	I	Mini-LVDS data input	
38	GND	I	Ground	
39	MLV4N	I	Mini-LVDS data input	
40	MLV4P	I	Mini-LVDS data input	
41	GND	I	Ground	
42	MLV3N	I	Mini-LVDS data input	
43	MLV3P	I	Mini-LVDS data input	
44	GND	I	Ground	
45	MLVCLKN	I	Mini-LVDS data input	
46	MLVCLKP	I	Mini-LVDS data input	
47	GND	I	Ground	
48	MLV2N	I	Mini-LVDS data input	
49	MLV2P	I	Mini-LVDS data input	
50	GND	I	Ground	
51	MLV1N	I	Mini-LVDS data input	
52	MLV1P	I	Mini-LVDS data input	
53	GND	I	Ground	
54	MLV0N	I	Mini-LVDS data input	
55	MLV0P	I	Mini-LVDS data input	
56	GND	I	Ground	
57	SHL	I	Left/Right Selection	Note 5-3
58	TTLRSDS	I	Mini-LVDS 3/6 pair input mode	
59	DIO1	I/O	Horizontal Start Pulse Signal Input or Output	Note 5-3
60	DIO2	I/O	Horizontal Start Pulse Signal Input or Output	Note 5-3

Note 5-1：V_{GG}= 18.0V

Note 5-2：V_{EE}= -6V

Note 5-3：Select left or right shift

R/L	DIO1	DIO2	Shift
1	Input	Hi-Z	Left to right
0	Hi-Z	Input	Right to left

Note 5-4：Gate driver shift clock

Note 5-5：When OE is connected to high “1”, the driver outputs are disabled (Gate output = V_{EE}).
Under this condition, the operation of registers will not be affected.

Note 5-6：Select up or down shift

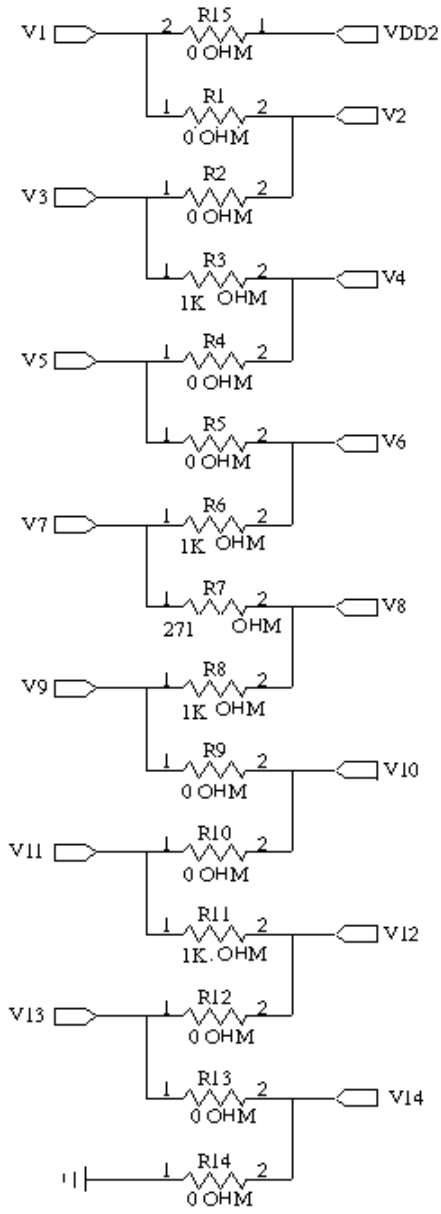
U/D	STVU	STVD	Shift
1	Hi-Z	Input	Down to Up
0	Input	Hi-Z	Up to Down

Note 5-7：Latch the polarity of outputs and switch the new data to outputs
At the rising edge (LD), latch the “POL” signal to control the polarity of the outputs.

Note 5-8：Control whether the Data D00~D25 are inverted or not.
When “REV=1”, these data will be inverted.
EX: “00”→”3F”, “07”→”38”, “15”→”2A”

Note 5-9：Polarity selector for dot-inversion control. Available at the rising edge of LD.
When POL=1：Even outputs range from V1~V7, and Odd outputs range from V8~V14.
When POL=0：Even outputs range from V8~V14, and Odd outputs range from V1~V7.

Note 5-10: Typical Application Circuit(When VDD2=12.5V)



6. Absolute Maximum Ratings：

AVSS=GND=0V, Ta=25℃

Parameters	Symbol	MIN.	MAX.	Unit	Remark
Supply Voltage	V_{DD1}	-0.5	5.0	V	
	V_{CC}	-0.3	7.0	V	
	V_{DD2}	-0.5	15	V	
	V_{GG}	-0.3	42.0	V	
	V_{GG}-V_{EE}	-0.3	40.0	V	
	V_{EE}	-20	0.3	V	
Operating Temperature	Top	-20	70	℃	
Storage Temperature	Tst	-30	80	℃	

7. Electrical Characteristics

7-1) Recommended Operating Conditions

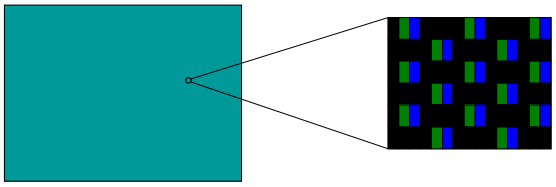
AVSS=GND = 0V，Ta = 25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Source Driver	V_{DD1}	3.0	3.3	3.6	V	
	V_{DD2}	-	12.5	-	V	
Supply Voltage for Gate Driver	V_{GG}	-	18	-	V	
	V_{EE}	-	-6.0	-	V	
	V_{CC}	3.0	3.3	3.6	V	
Supply Voltage for Vcom	V_{com}	-	4.5	-	V	

7-2) Power Consumption

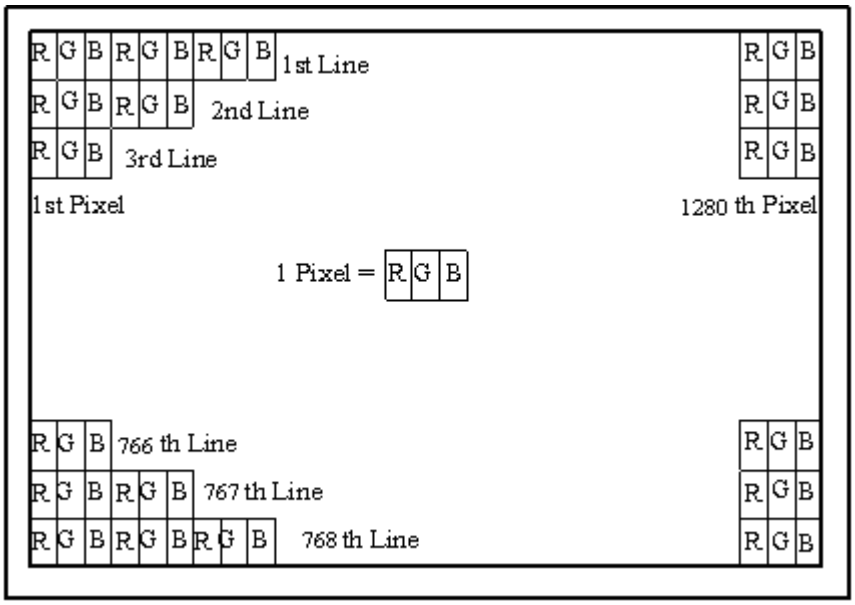
Parameter	Symbol	Condition	Typ.	Max.	Unit	Remark
Supply Current for Gate Driver (Hi level)	I_{GG}	V_{GG}= 18V	TBD	TBD	mA	Note 7-2
Supply Current for Gate Driver (Low level)	I_{EE}	V_{EE}= -6.0V	TBD	TBD	mA	
Supply Current for Source Driver (Digital)	I_{DD1}	V_{DD1}=3.3V	TBD	TBD	mA	
Supply Current for Source Driver (Analog)	I_{DD2}	V_{DD2}= 12.5V	TBD	TBD	mA	
Supply Current for Gate Driver (Digital)	I_{CC}	V_{CC}=3.3V	TBD	TBD	mA	
LCD Panel Power Consumption	-	-	TBD	TBD	mW	Note 7-1

Note 7-1:The power consumption for back light is not included.
Note7-2:Test pattern for dissipative current.



8. Pixel Arrangement

The LCD module pixel arrangement is the stripe.

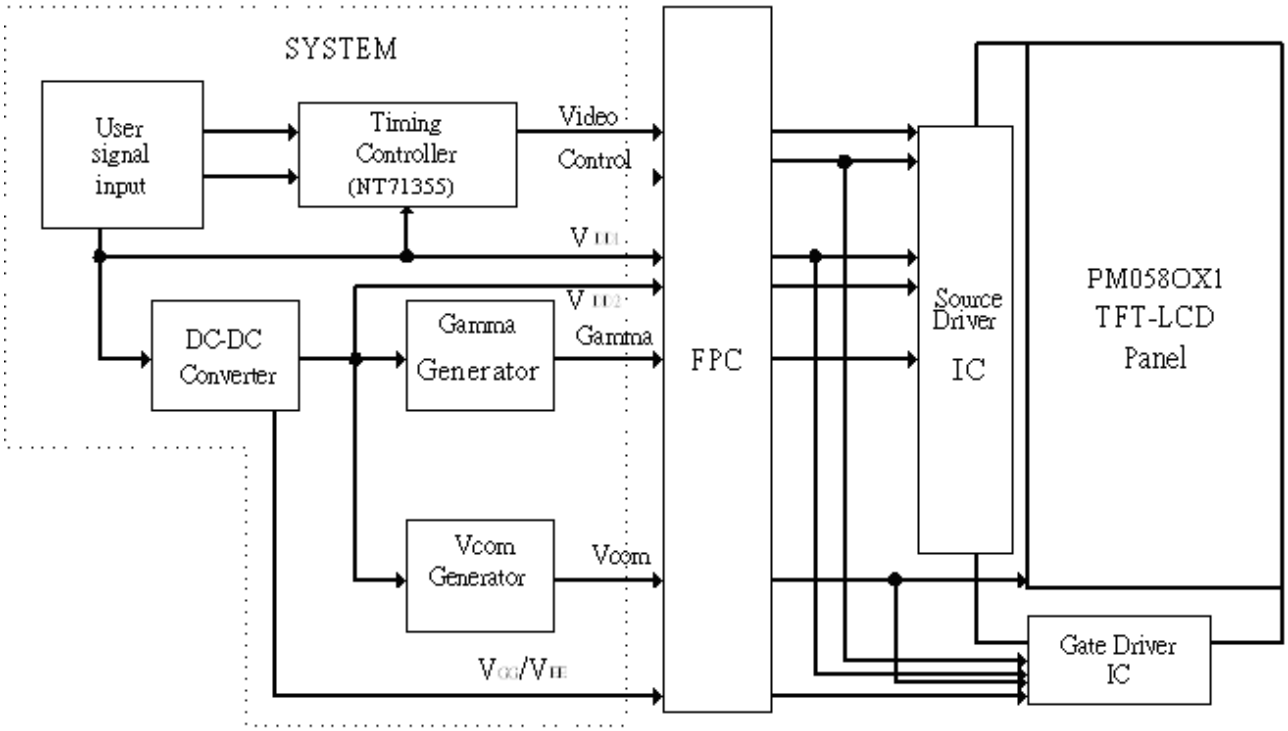


9. Display Color and Gray Scale Reference

Color		Input Color Data																	
		Red						Green						Blue					
		R5	**R4**	**R3**	**R2**	**R1**	**R0**	**G5**	**G4**	**G3**	**G2**	**G1**	**G0**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Red	Red (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (01)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (02)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Red (61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red (62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Green	Green (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (01)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green (02)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Green (61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green (62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green (63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Blue	Blue (00)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (01)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (02)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Darker																		
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
	Brighter																		
	Blue (61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue (62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue (63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

10. Block Diagram

10-1) TFT-module Block Diagram



If you use PM058OX1 , you must apply NT71355 (Timing controller) which Will gernerate signal to support PM058OX1

11. Interface Timing

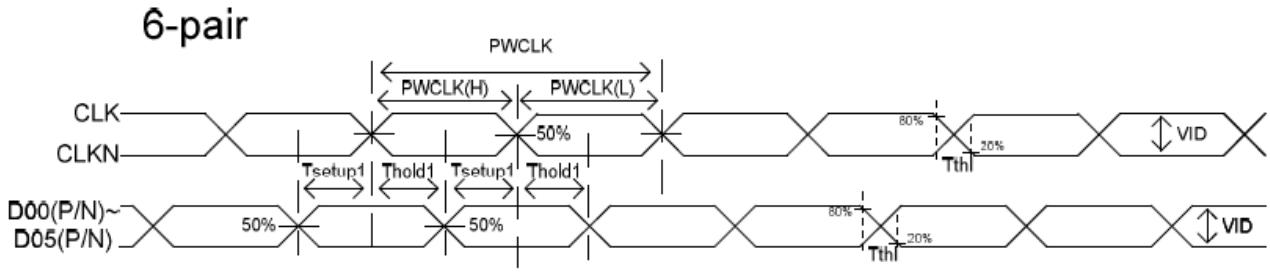
11.1) Timing Parameters

AVSS=GND = 0V，Ta = 25℃

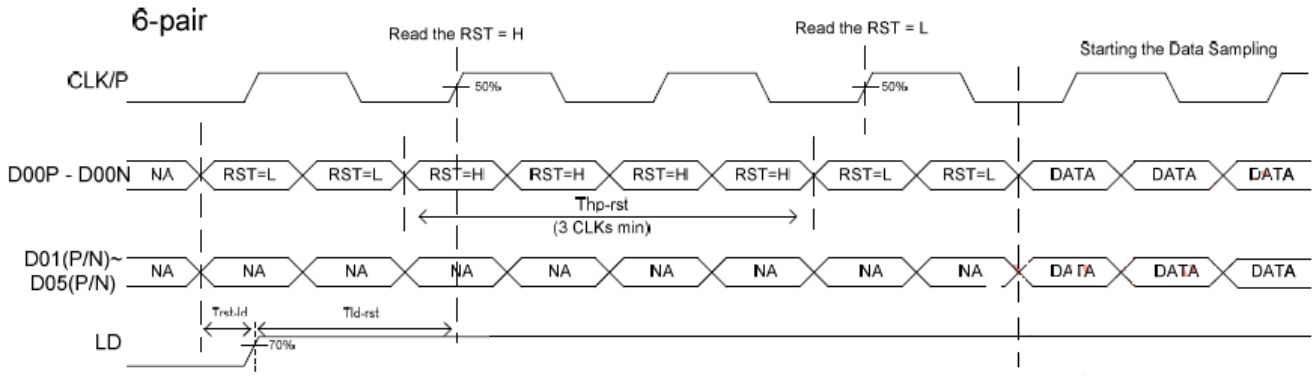
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
CLK Frequency	Fclk	-	80	135	MHz	
CLK Pulse Width	PWCLK	7.41	-	-	ns	3.0V~3.6V
CLK Pulse Low Period	PWCLK(L)	0.4 CLKN	-	0.6 CLKN	CLK	
CLK Pulse High Period	PWCLK(H)	0.4 CLKN	-	0.6 CLKN	CLK	
Data Setup Time	Tsetup1	0.9	-	-	ns	PWCLK=7.41ns
Data Hold Time	Thold1	0.9	-	-	ns	PWCLK=7.41ns
DIO SETUP Time	Tsetup2	0	-	-	ns	
DIO Signal Delay Time	Tplh	-	-	3	CLK	Load=25pF
DIO Pulse Width	Twd	-	-	6	CLK	
CLK, D00~D05, D10~D15 Rising Time	Tthl	-	-	0.5	ns	PWCLK=7.41ns
CLK, D00~D05, D10~D15 Falling Time	Ttlh	-	-	0.5	ns	PWCLK=7.41ns
Reset(RST) High Period	Thp-rst	3	-	-	CLK	>50ns
Receive Off to LD Timing	Tro-ld	6	-	-	CLK	
LD High Pulse Width	PWLD	21	-	-	CLK	
POL Setup Time	Tsetup3	14	-	-	ns	
POL Hold Time	Thold3	10	-	-	ns	
LD to Reset Input Time	Tld-rst	21	-	-	CLK	Also more than 200ns
Reset Low to LD Rising Time	Trst-ld	0	-	-	ns	

11.2) Timing Diagram

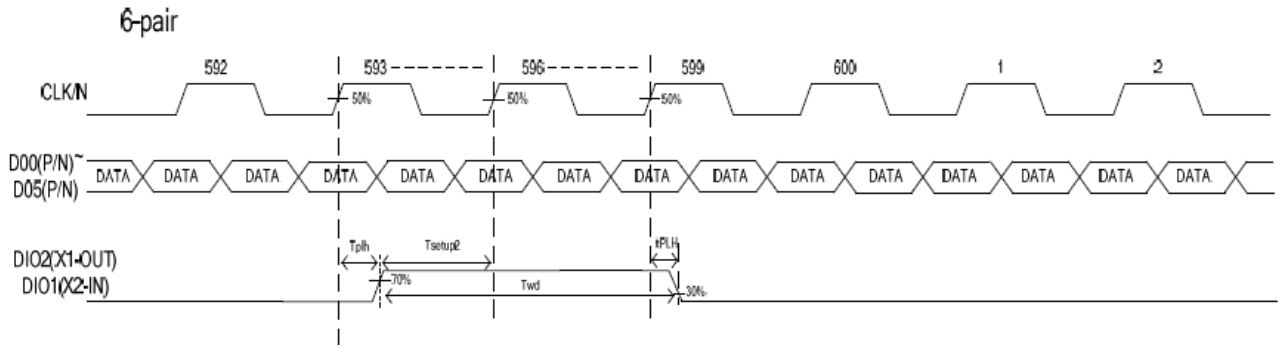
※Timing for receiving data



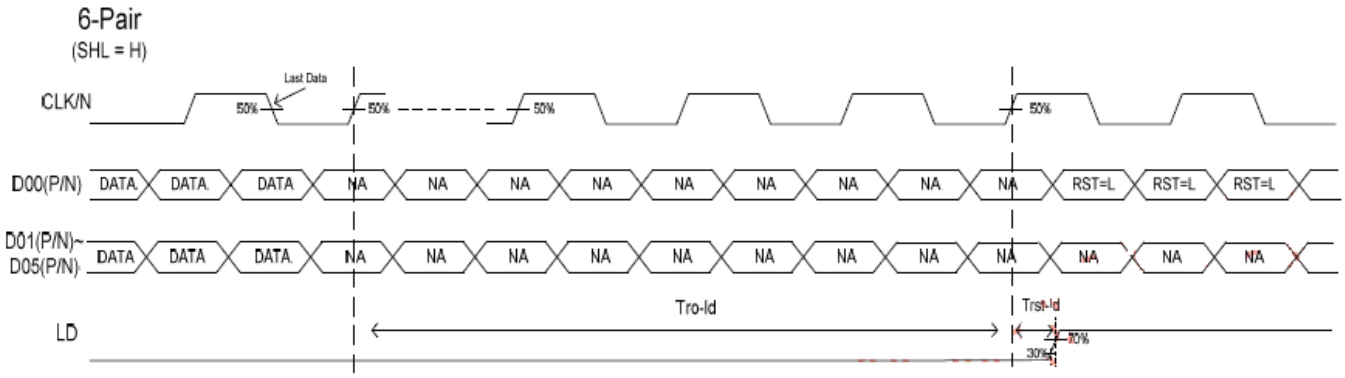
※ Input data timing



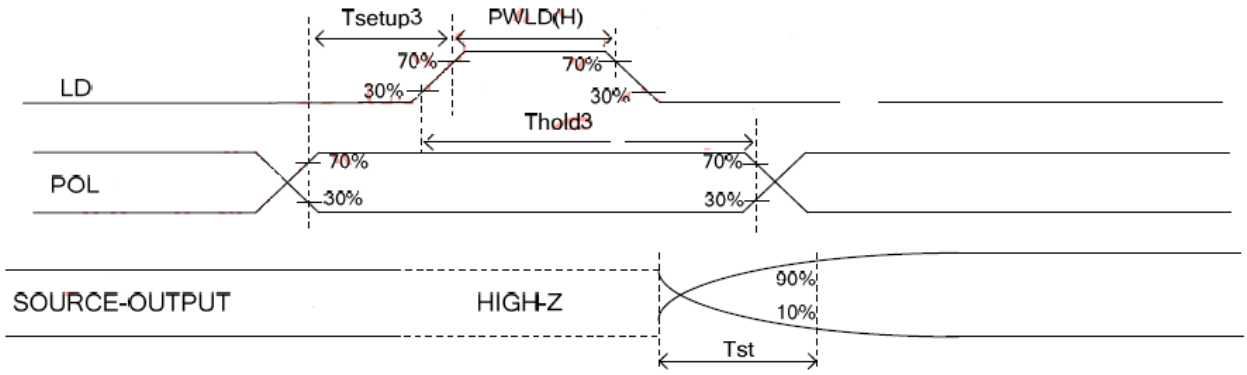
※ Input data timing(Cascade Chip)



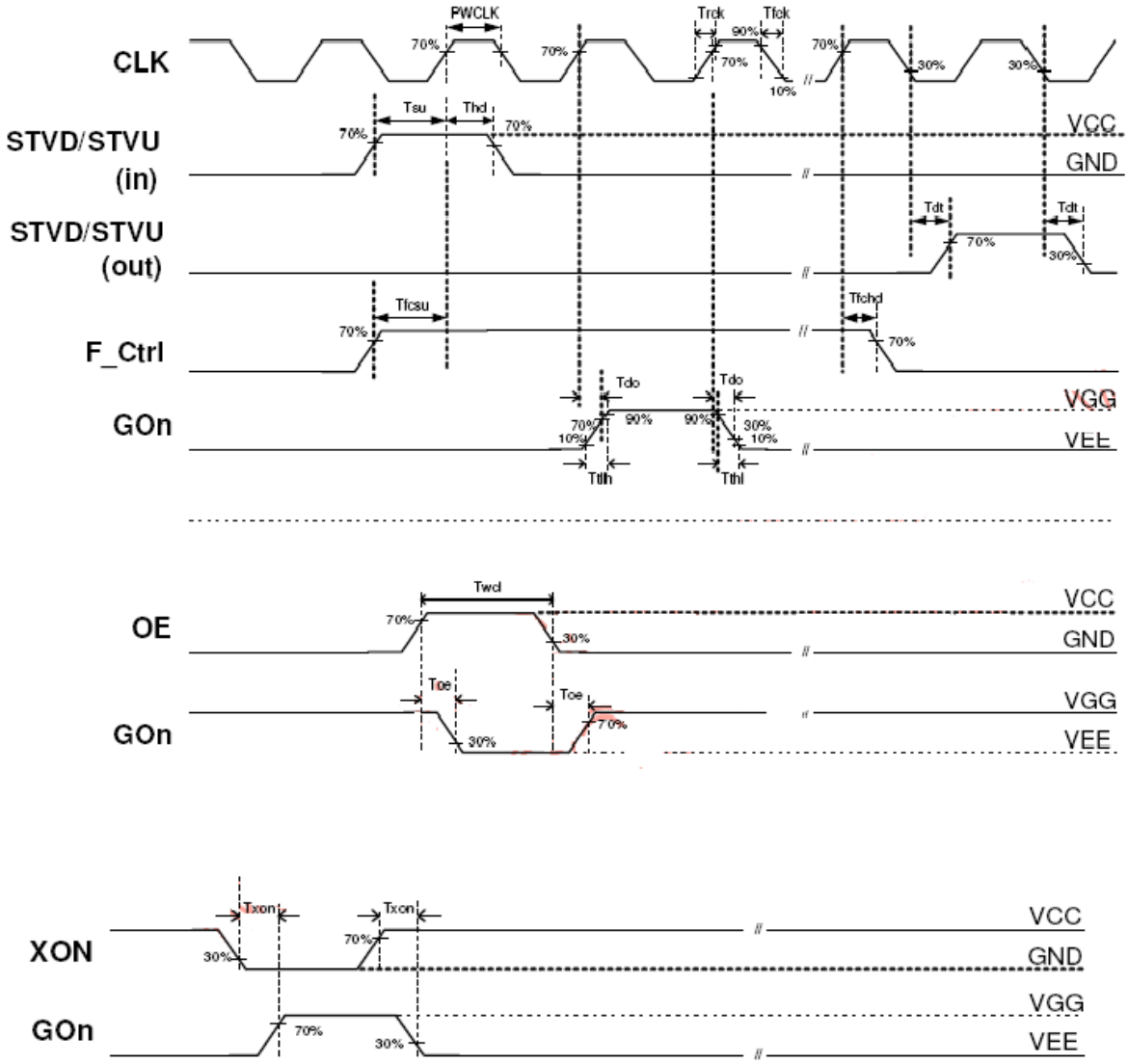
※ Last Data Sampling to LD Timing



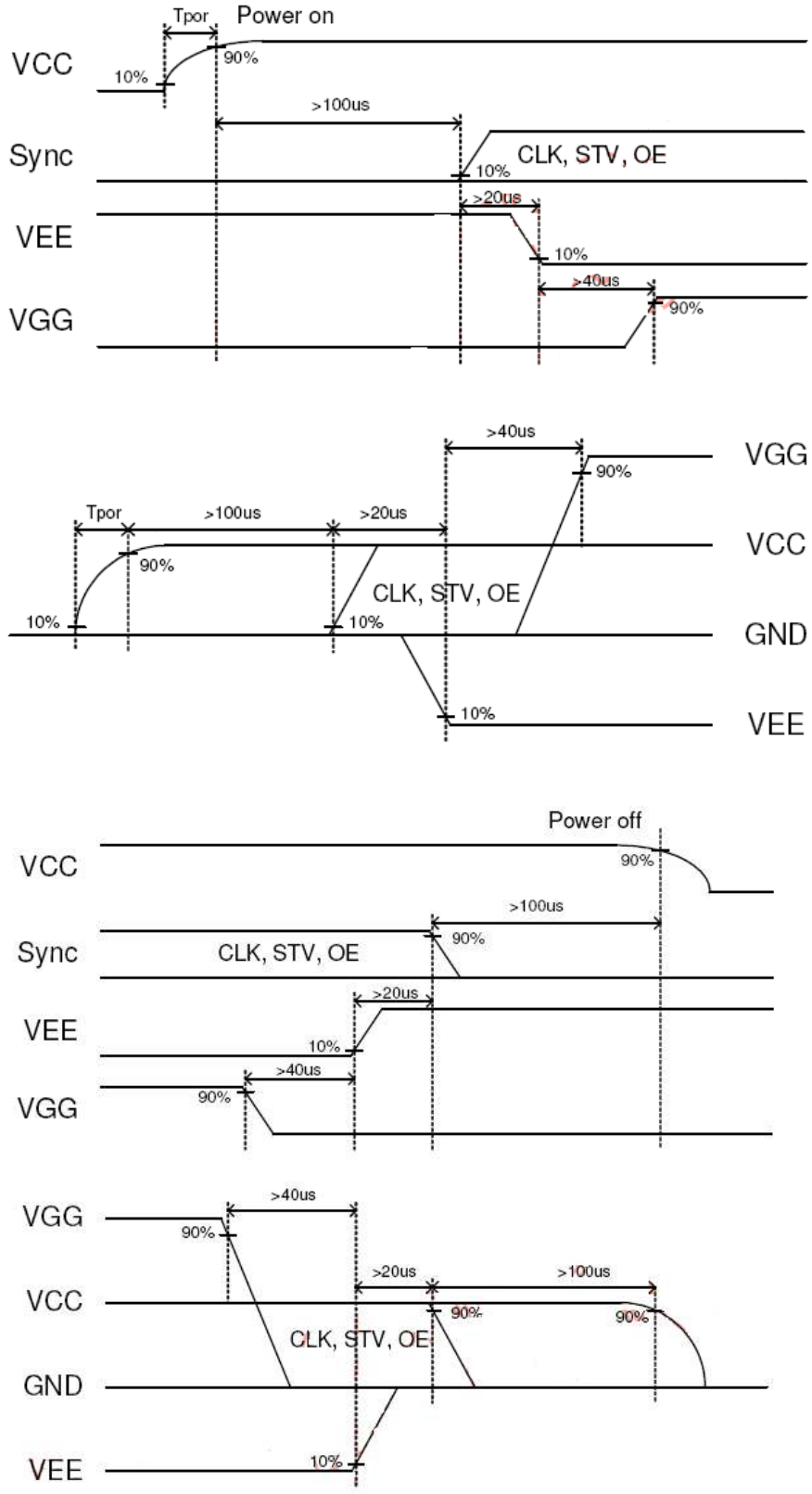
※ Output Timing



※Timing waveform



12. Power On Sequence



13. Optical Characteristics

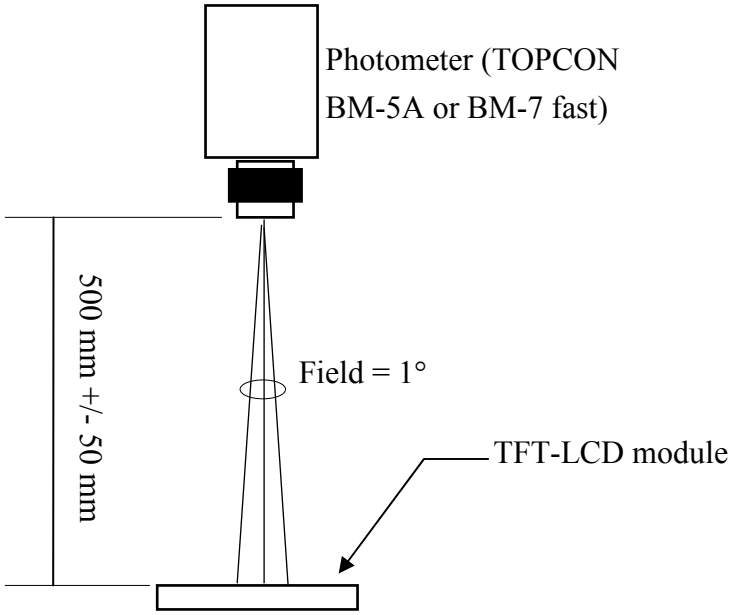
13-1) Specification：

The backlight which EIH used is LED for optical measuring and the specification of average brightness is 10930(cd/m^2).

Ta=25℃

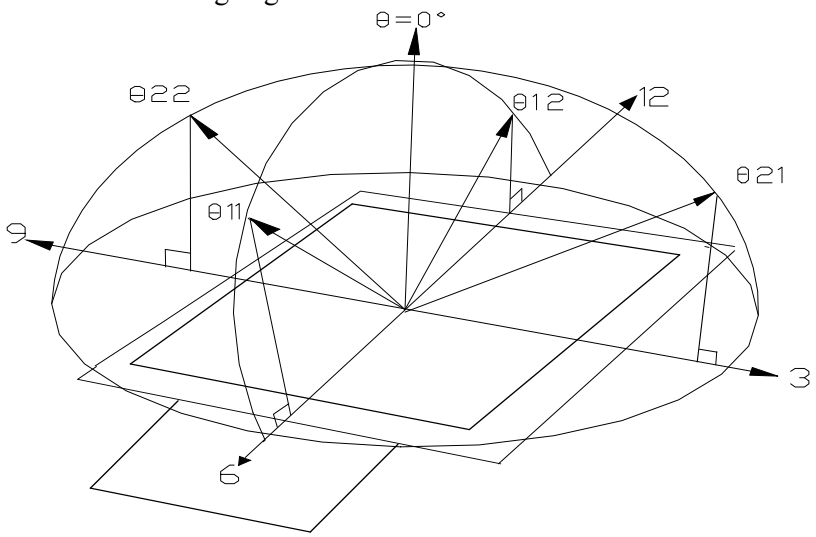
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ 21, θ 22	CR≧10	45	50	-	deg	Note 13-1
	Vertical	θ 12(to 12 o'clock)		10	15	-	deg	
		θ 11(to 6 o'clock)		30	35	-	deg	
Contrast Ratio		CR	At optimized Viewing angle	TBD	TBD	-	-	Note 13-3
Response time	Rise	Tr	θ =0°	-	15	30	ms	Note 13-2
	Fall	Tf		-	25	50	ms	
Transmission ratio		T	θ =0°	TBD	TBD	-	-	-
Cross talk			θ =0°	-	-	3.5	%	Note 13-4

All the optical measurement shall be executed 30 minute after backlight being turn-on. The optical characteristics shall be measured in dark room (ambient illumination on panel surface less than 1 Lux). The measuring configuration shows as following figure.

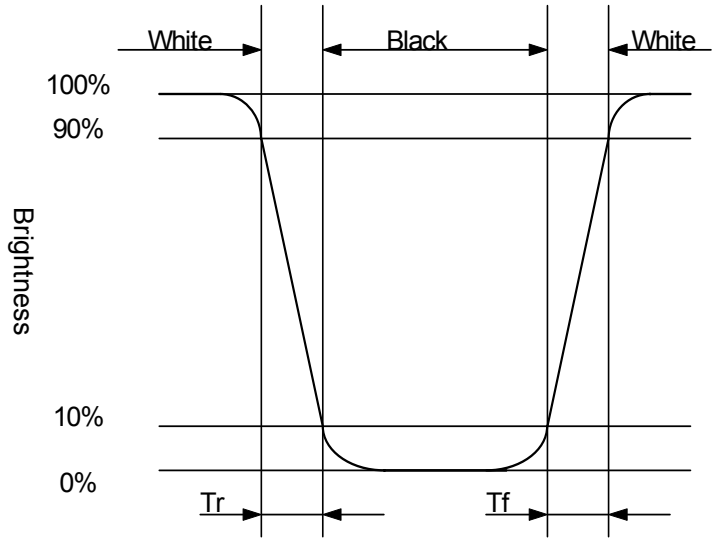


Optical characteristics measuring configuration

Note 13-1：The definitions of viewing angles are as follow



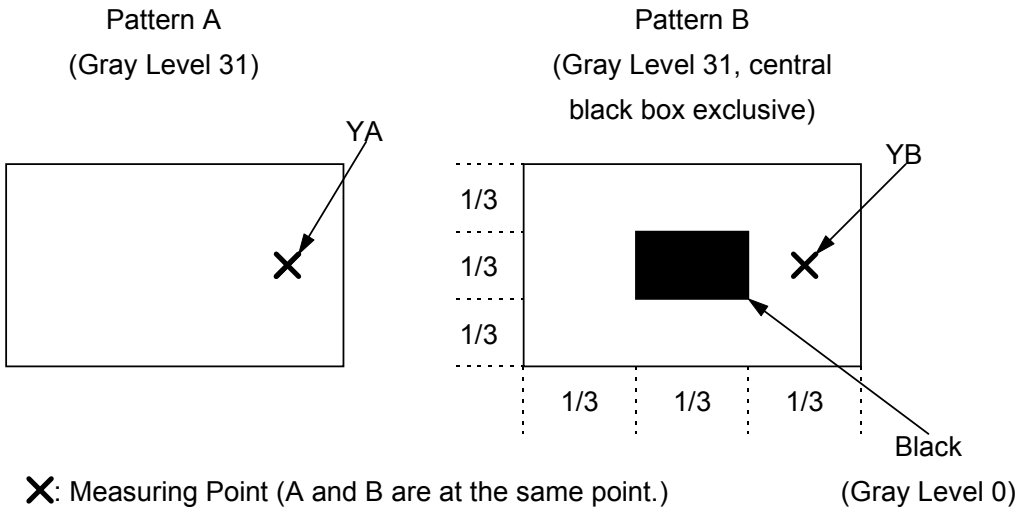
Note 13-2：Definition of Response Time T_r and T_f



Note 13-3：The definition of contrast ratio $CR = \frac{\text{Luminance at White Pattern}}{\text{Luminance at Black Pattern}}$

Note 13-4: Cross Talk (CTK) = $\frac{|YA-YB|}{YA} \times 100\%$

YA: Brightness of Pattern A
YB: Brightness of Pattern B
Luminance meter: BM 5A or BM-7 fast (TOPCON)
Measurement distance: 500 mm +/- 50 mm
Ambient illumination: < 1 Lux
Measuring direction: Perpendicular to the surface of module



14. Handling Cautions

14-1) Mounting of module

a) Please power off the module when you connect the input/output connector.
b) Polarizer which is made of soft material and susceptible to flaw must be handled carefully.
c) Protective film (Laminator) is applied on surface to protect it against scratches and dirt.
d) Please following the tear off direction as figure14-1 to remove the protective film as slowly as possible, so that electrostatic charge can be minimized.
e) After combining the plastic frame with the top chassis,user must reserve enough space to FPC to avoid FPC damage due to lack of space Figure 14-2.

14-2) Precautions in mounting

a) When metal part of the TFT-LCD module (shielding lid and rear case) is soiled, wipe it with soft dry cloth.
b) Wipe off water drops or finger grease immediately. Long contact with water may cause discoloration or spots.
c) TFT-LCD module uses glass which breaks or cracks easily if dropped or bumped on hard surface. Please handle with care.
d) Since CMOS LSI is used in the module. So take care of static electricity and earth yourself when handling.

14-3) Adjusting module

a) Adjusting volumes on the rear face of the module have been set optimally before shipment.
b) Therefore, do not change any adjusted values. If adjusted values are changed, the specifications described may not be satisfied.

14-4) Others

a) Do not expose the module to direct sunlight or intensive ultraviolet rays for many hours.
b) Store the module at a room temperature place.
c) The voltage of beginning electric discharge may over the normal voltage because of leakage current from approach conductor by to draw lump read lead line around.
d) If LCD panel breaks, it is possibly that the liquid crystal escapes from the panel. Avoid putting it into eyes or mouth. When liquid crystal sticks on hands, clothes or feet. Wash it out immediately with soap.
e) Observe all other precautionary requirements in handling general electronic components.
f) Please adjust the voltage of common electrode as material of attachment by 1 module.

14-5) Polarizer mark

The polarizer mark is to describe the direction of wide view angle film how to mach up with the rubbing direction.

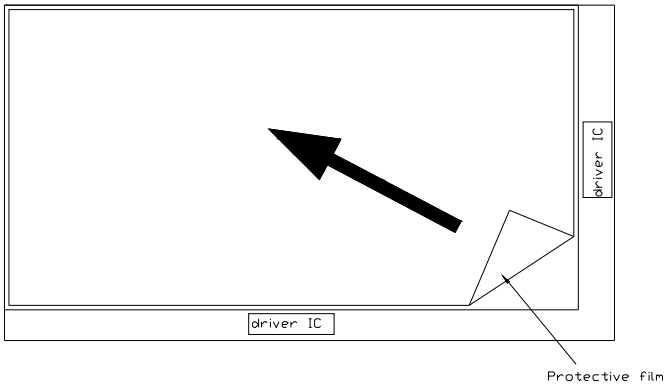


Figure 14-1 the way to peel off protective film

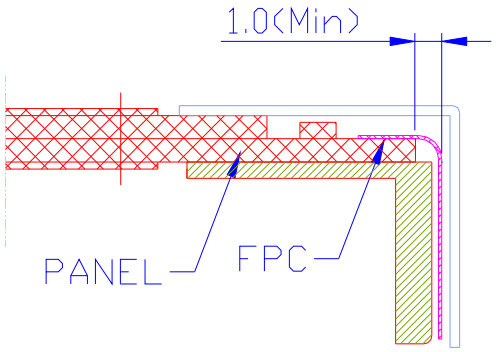


Figure 14-2

15. Reliability Test

No	Test Item	Test Condition	Remark
1	High Temperature Storage Test	Ta = +80℃, 240 hrs	
2	Low Temperature Storage Test	Ta = -30℃, 240 hrs	
3	High Temperature Operation Test	Ta = +70℃, 240 hrs	
4	Low Temperature Operation Test	Ta = -20℃, 240 hrs	
5	High Temperature & High Humidity Operation Test	Ta = +60℃, 90%RH, 240 hrs (No Condensation)	
6	Thermal Cycling Test (non-operating)	-20℃→+70℃, 200 Cycles (30min – 30min)	
7	Electrostatic Discharge Test (non-operating)	200pF, 0Ω ±200V 1 time / each terminal	

Ta：ambient temperature
Note：The protective film must be removed before temperature test.

[Criteria]
In the standard conditions, there is not display function NG issue occurred. (including：line defect ,no image).All the cosmetic specification is judged before the reliability stress.

16. Packing Diagram

TBD