



# ORAP-29044 Datasheet

## ORAP-29044 Datasheet Revision log

Version	Author	Issue date	Other
V 1.0	HJ	2012-05-31	Pre-release



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ORIENT



## 1 Introduction

The ORAP-29044 is an integrated ambient and infrared light-to-digital converter with a built-in IR LED and I2C Interface (SMBus Compatible). This device uses two independent ADCs for concurrently measuring ambient light and proximity in parallel. The flexible interrupt scheme is designed for minimal microcontroller utilization.

For ambient light sensor (ALS) data conversions, an ADC converts photodiode current (with a light sensitivity range up to 2000 Lux) in 100ms per sample. The ADC rejects 50Hz/60Hz flicker noise caused by artificial light sources.

For proximity sensor (Prox) data conversions, the built-in driver turns on an internal infrared LED and the proximity sensor ADC converts the reflected IR intensity to digital. This ADC rejects ambient IR noise (such as sunlight) and has a 540 $\mu$ s conversion time.

The ORAP-29044 provides low power operation of ALS and proximity sensing with a typical 138 $\mu$ A normal operation current (112 $\mu$ A for sensors and internal circuitry, ~28 $\mu$ A for LED) with 220mA current pulses for a net 100 $\mu$ s, repeating every 800ms (or under).

The ORAP-29044 uses both a hardware pin and software bits to indicate an interrupt event has occurred. An ALS interrupt is defined as a measurement that is outside a set window. A proximity interrupt is defined as a measurement over a threshold limit. The user may also require that both ALS/Prox interrupts occur at once, up to 16 times in a row before activating the interrupt pin.

The ORAP-29044 is designed to operate from 2.25V to 3.63V over the -40°C to +85°C ambient temperature range. It is packaged in a clear, lead-free 8 Ld ODFN package.

## 2 Features

Internal LED + Sensor = Complete Solution  
Works Under All Light Sources Including Sunlight  
Dual ADCs Measure ALS/Prox Concurrently  
<1.0 $\mu$ A Supply Current When Powered Down  
Temperature Compensated  
Pb-Free (RoHS compliant)

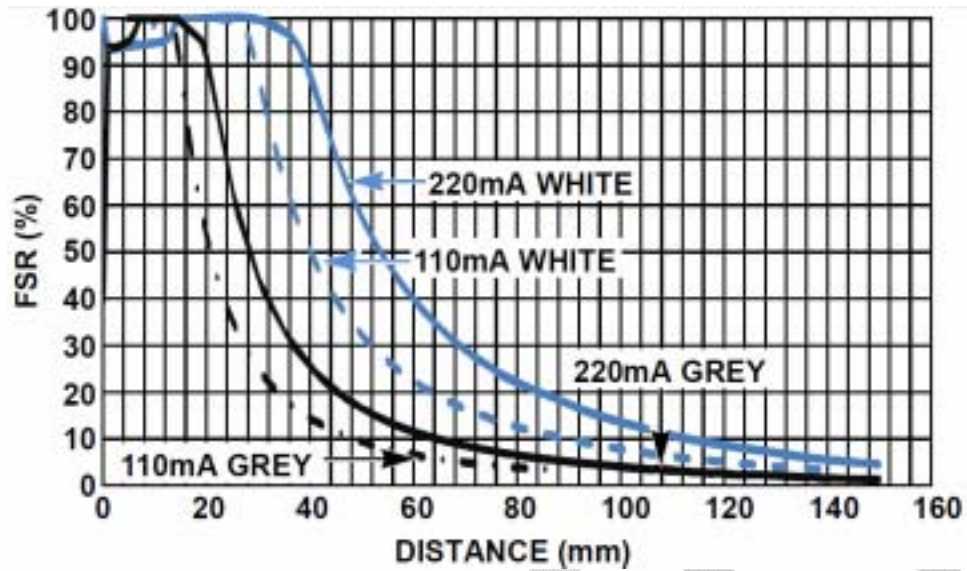
### **Intelligent and Flexible Interrupts**

Independent ALS/Prox Interrupt Thresholds  
Adjustable Interrupt Persistency

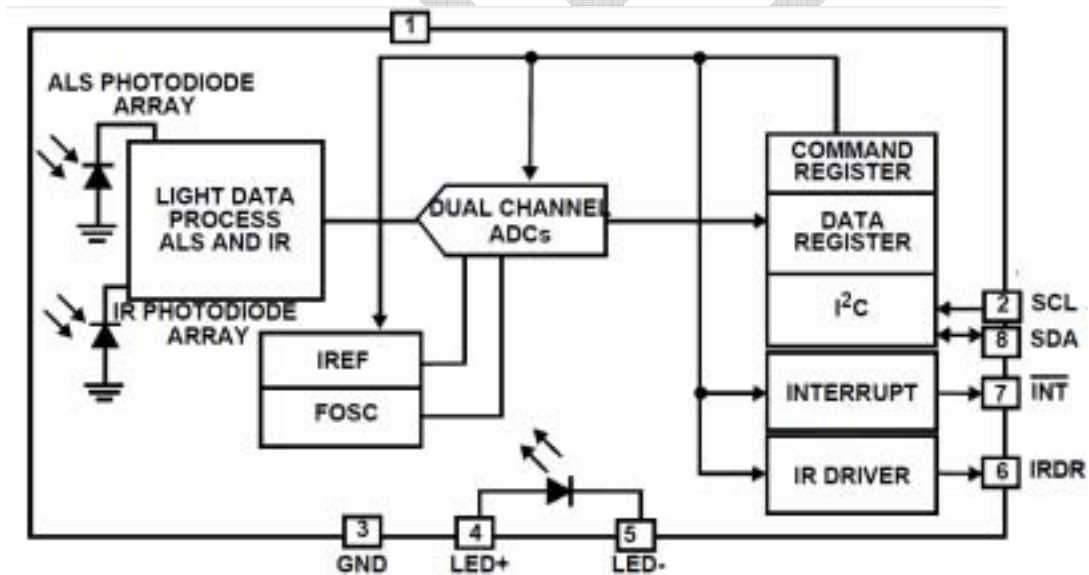
- 1/4/8/16 Consecutive Triggers Required Before Interrupt



## Proximity response vs distance

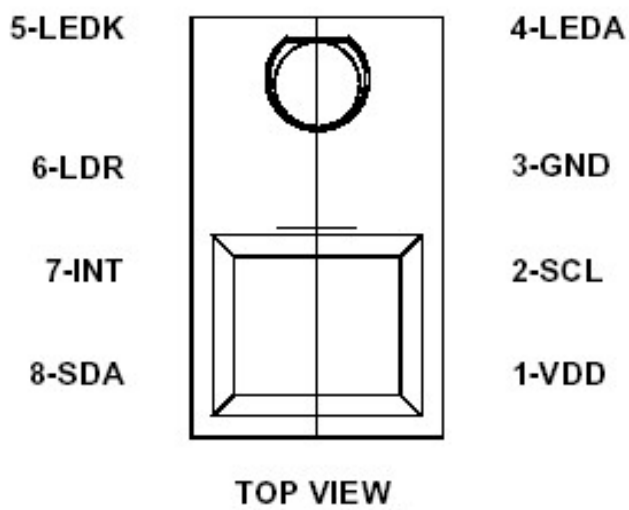


## 4 ORAP-29044 Block Diagram



### 4.1 Pin Configuration

ORAP-29044  
 (8 LD 2.36X3.94 (mm) OPTICAL CO-PACKAGE)



## 4.2 Pin Descriptions

pin	Pin name	Descriptions
1	VDD	Voltage supply 2.25V to 3.63V.
2	SCL	I2C clock line can be pulled from 1.7V to above VDD, 3.63V max.
3	GND	Ground
4	LED+	Anode of IR LED
5	LED-	Cathode of IR LED
6	IRDR	IR-LED driver pin - current flows into ORAP-29044 from LED cathode.
7	INT	Interrupt pin; Logic output (open-drain) for interrupt.
8	SDA	I2C data line can be pulled from 1.7V to above VDD, 3.63V max.



### 4.3 Absolute Maximum Ratings (TA = +25°C)

VDD Supply Voltage between VDD and GND	4.0V
I2C Bus Pin Voltage (SCL, SDA)	-0.5V to 4.0V
I2C Bus Pin Current (SCL, SDA)	<10mA
IRDR Pin Voltage	5.5V
INT Pin Voltage	-0.5V to 4.0V
INT Pin Current	<10mA
ESD Rating	
Human Body Model	TBD

### 4.4 Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
8 Ld Optical Module Package	113	58
Maximum Die Temperature	+90°C	
Storage Temperature	-40°C to +85°C	
Operating Temperature	-40°C to +85°C	

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

$\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air.

For  $\theta_{JC}$ , the “case temp” location is the center of the exposed metal pad on the package underside.

ESD is rated at 2kV HBM on all pins except IRDR, which is rated at 1kV.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_j = T_c = T_a$ .





## 4.5 Electrical Specifications (V<sub>DD</sub> = 3.0V, T<sub>A</sub> = +25°C.)

PARAMETER	DESCRIPTION	CONDITION	MIN	TYPE	MAX	UNIT
V <sub>DD</sub>	Power Supply Range		2.25	3.0	3.63	V
SR_V <sub>DD</sub>	Input Power-up Slew Rate	V <sub>DD</sub> Rising Edge between 0.4V and 2.25V	0.5			V/ms
I <sub>DD_OFF</sub>	Supply Current when Powered Down	ALS_EN = 0; PROX_EN = 0		0.1	0.8	uA
I <sub>DD_NORM</sub>	Supply Current for ALS+Prox in Sleep Time	ALS_EN = 1; PROX_EN = 1		112	125	uA
I <sub>DD_PRX_SLP</sub>	Supply Current for Prox in Sleep Time	ALS_EN = 0; PROX_EN = 1		73		uA
I <sub>DD_ALS</sub>	Supply Current for ALS	ALS_EN = 1; PROX_EN = 0		97		uA
f <sub>OSC</sub>	Internal Oscillator Frequency			5.25		MHz
t <sub>INTGR_ALS</sub>	12-bit ALS Integration/Conversion Time		TBD	TBD	TBD	Ms
t <sub>INTGR_PROX</sub>	8-bit Prox Integration/Conversion Time			0.54		ms
DATA <sub>ALS_0</sub>	ALS Result when Dark	EAMBIENT = 0 lux, 2k Range		1	TBD	Counts
DATA <sub>ALS_F</sub>	Full Scale ALS ADC Code	EAMBIENT > Selected Range Maximum Lux			4095	Counts
ΔDATA DATA	Count Output Variation Over Three Light Sources: Ambient Light Sensing Fluorescent, Incandescent and Sunlight	Ambient Light Sensing		TBD		%
DATA <sub>ALS_1</sub>	Light Count Output with LSB of 0.0326 lux/count	E = 53 lux, Fluorescent , ALS_RANGE = 0		TBD		Counts
DATA <sub>ALS_2</sub>	Light Count Output With LSB of 0.522 lux/count	E = 320 lux, Fluorescent , ALS_RANGE = 1	TBD	TBD	TBD	Counts
DATA <sub>PROX_0</sub>	Prox Measurement w/o Object in Path			TBD		Counts
DATA <sub>PROX_F</sub>	Full Scale Prox ADC Code				255	Counts
t <sub>r</sub>	Rise Time for IRDR Sink Current	R <sub>LOAD</sub> = 15Ω at IRDR pin, 20% to 80%		500		ns
t <sub>f</sub>	Fall time for IRDR Sink Current	R <sub>LOAD</sub> = 15Ω at IRDR pin, 80% to 20%		500		ns
I <sub>IRDR_0</sub>	IRDR Sink Current	PROX_DR = 0; V <sub>IRDR</sub> = 0.5V	TBD	TBD	TBD	mA
I <sub>IRDR_1</sub>	IRDR Sink Current	PROX_DR = 1; V <sub>IRDR</sub> = 0.5V		TBD		mA
I <sub>IRDR_LEAK</sub>	IRDR Leakage Current	PROX_EN = 0; V <sub>DD</sub> = 3.63V (Note 10)		0.001	1	uA
V <sub>IRDR</sub>	Acceptable Voltage Range on IRDR Pin	Register bit PROX_DR = 0	0.5		4.3	V
t <sub>PULSE</sub>	Net IIRDR On Time Per PROX Reading			100		us
F <sub>I<sup>2</sup>C</sub>	I <sup>2</sup> C Clock Rate Range				400	KHz



$V_{I^2C}$	Supply Voltage Range for I <sup>2</sup> C Interface		1.7		3.63	V
$V_{IL}$	SCL and SDA Input Low Voltage				0.55	V
$V_{IH}$	SCL and SDA Input High Voltage		1.25			V
$I_{SDA}$	SDA Current Sinking Capability	$V_{OL} = 0.4V$	3	5		mA
$I_{INT}$	INT Current Sinking Capability	$V_{OL} = 0.4V$	3	5		mA
$PSRR_{IRDR}$	$(\Delta I_{IRDR})/(\Delta V_{IRDR})$	PROX_DR = 0; $V_{IRDR} = 0.5V$ to 4.3V		3		mA/V

**NOTES:**

Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

An LED is used in production test. The LED irradiance is calibrated to produce the same DATA count against a fluorescent light source of the same lux level.

An 850nm infrared LED is used to test PROX/IR sensitivity in an internal test mode.

Ability to guarantee  $I_{IRDR}$  leakage of ~1nA is limited by test hardware.

For ALS applications under light-distorting glass, please see the section titled “ALS Range 1 Considerations”

## 4.6 IR-LED Specifications TA = +25°C

PARAMETER	DESCRIPTION	CONDITION	MIN	TYPE	MAX	UNIT
$V_F$	IR-LED Forward Voltage Drop	$I_F = 10\mu A$		1.0		V
		$I_F = 100mA$		1.6	1.8	V
$I_R$	IR-LED Reverse-Bias Current	$V_R = 10V$			5	$\mu A$
$\lambda_P$	IR-LED Peak Output Wavelength	$I_F = 100mA$	480	855	870	nm
$\Delta\lambda$	IR-LED Spectral Half-Width	$I_F = 100mA$		30		nm
$\Phi_E$	IR-LED Radiant Power	$I_F = 100mA$	27			mW
		$I_F = 100mA$	33			mW
$I$	IR-LED Radiant Intensity (in 0.01sr)	$I_F = 100mA$				mW/SR

## 4.7 I2C Electrical Specifications



For SCL and SDA unless otherwise noted, VDD = 3V, TA = +25°C

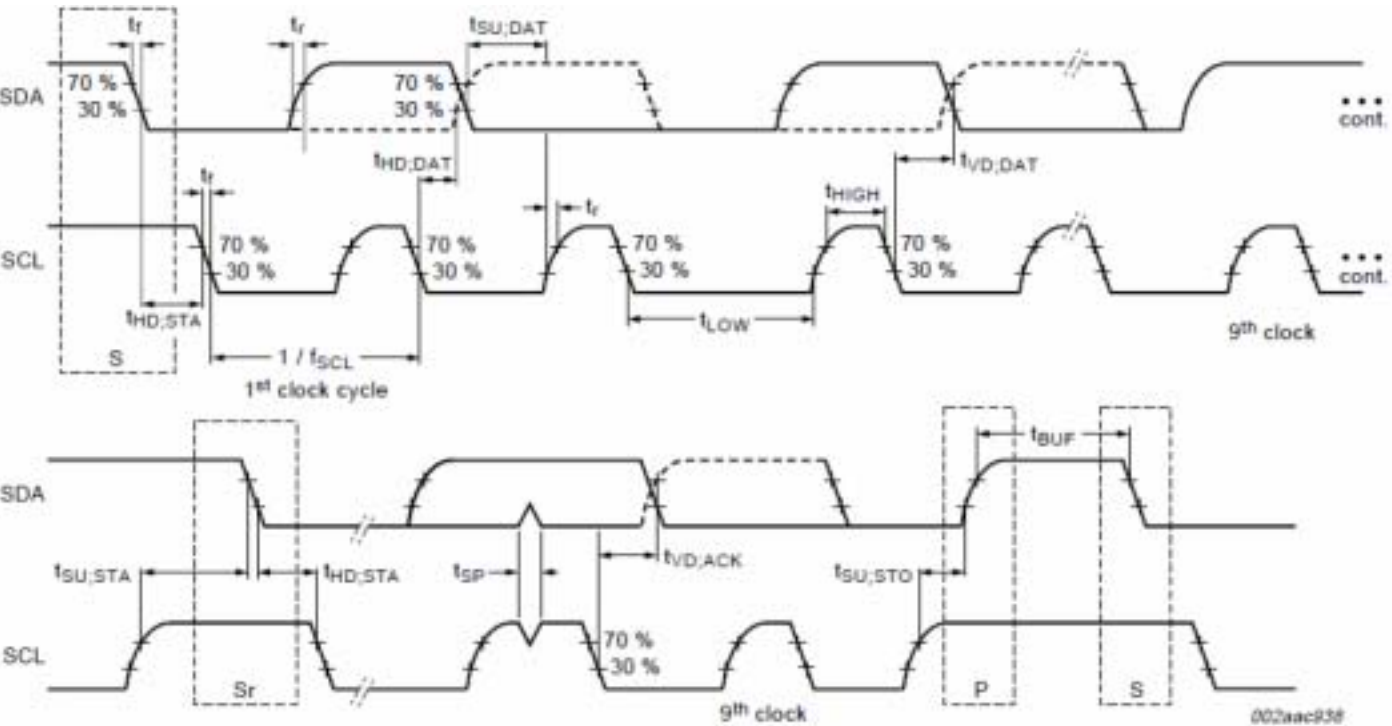
PARAMETER	DESCRIPTION	CONDITION	MIN	TYP E	MAX	UNIT
V <sub>I<sup>2</sup>C</sub>	Supply Voltage Range for I <sup>2</sup> C Interface		1.7		3.63	V
f <sub>SCL</sub>	SCL Clock Frequency				400	KHz
V <sub>IL</sub>	SCL and SDA Input Low Voltage				0.55	V
V <sub>IH</sub>	SCL and SDA Input High Voltage		1.25			V
V <sub>hys</sub>	Hysteresis of Schmitt Trigger Input		0.05V <sub>DD</sub>			V
V <sub>OL</sub>	Low-level Output Voltage (Open-drain) at 4mA Sink Current				0.4	V
I <sub>i</sub>	Input Leakage for each SDA, SCL Pin		-10		10	uA
t <sub>SP</sub>	Pulse Width of Spikes that must be Suppressed by the Input Filter				50	ns
t <sub>AA</sub>	SCL Falling Edge to SDA Output Data Valid				900	ns
C <sub>i</sub>	Capacitance for each SDA and SCL Pin				10	pF
t <sub>HD:STA</sub>	Hold Time (Repeated) START Condition	After this period, the first clock pulse is generated.	600			ns
t <sub>LOW</sub>	LOW period of the SCL Clock	Measured at the 30% of VDD crossing.	1300			ns
t <sub>HIGH</sub>	HIGH period of the SCL Clock		600			ns
t <sub>SU:STA</sub>	Set-up Time for a Repeated START Condition		600			ns
t <sub>HD:DAT</sub>	Data Hold Time		30			ns
t <sub>SU:DAT</sub>	Data Set-up Time		100			ns
t <sub>R</sub>	Rise Time of both SDA and SCL Signals		20 + 0.1×C <sub>b</sub>			ns
t <sub>F</sub>	Fall Time of both SDA and SCL Signals		20 + 0.1×C <sub>b</sub>			ns
t <sub>SU:STO</sub>	Set-up Time for STOP Condition		600			ns
t <sub>BUF</sub>	Bus Free Time Between a STOP and START Condition		1300			ns
C <sub>b</sub>	Capacitive Load for Each Bus Line				400	pF
R <sub>pull-up</sub>	SDA and SCL System Bus Pull-up Resistor	Maximum is determined by t <sub>R</sub> and t <sub>F</sub>	1			kΩ
t <sub>VD:DAT</sub>	Data Valid Time				0.9	us
t <sub>VD:ACK</sub>	Data Valid Acknowledge Time				0.9	us
V <sub>nL</sub>	Noise Margin at the Low Level		0.1V <sub>DD</sub>			V



V <sub>NH</sub>	Noise Margin at the High Level		0.2V <sub>DD</sub>			V
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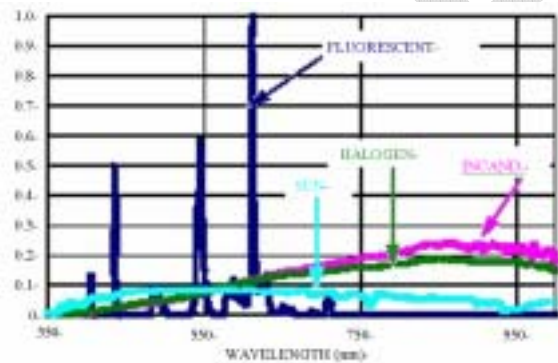
Note:

All parameters in I<sup>2</sup>C Electrical Specifications table are guaranteed by design and simulation.  
 C<sub>b</sub> is the capacitance of the bus in pF.

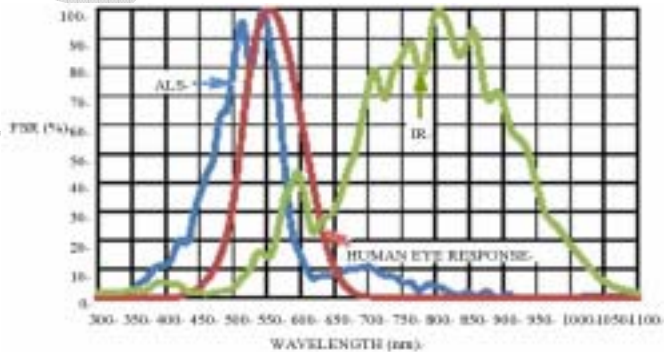


I<sup>2</sup>C TIMING DIAGRAM

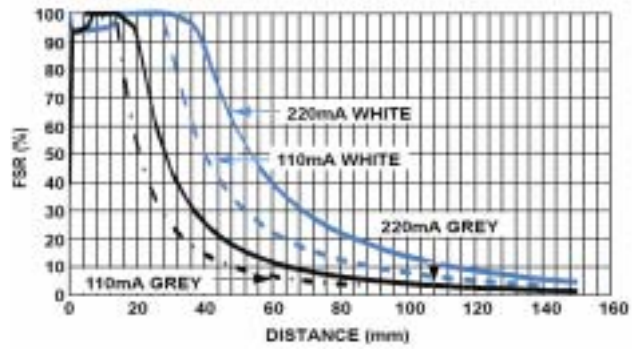
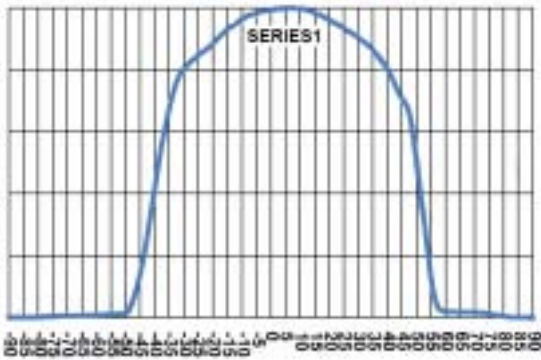
### 4.8 Typical Performance Curves (V<sub>DD</sub>=3.0)



SPECTRUM OF FOUR LIGHT SOURCES  
 NORMALIZED BY LUMINOUS INTENSITY (LUX)

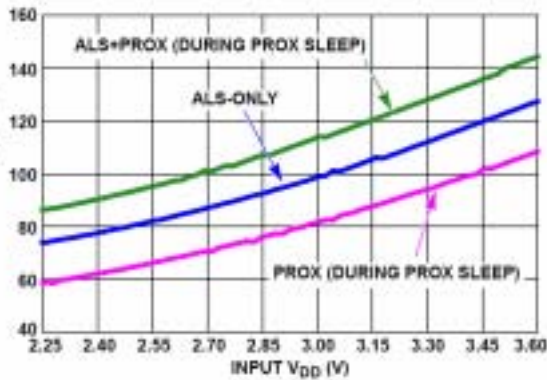


ORAP-29044 SENSITIVITY TO DIFFERENT WAVELENGTHS



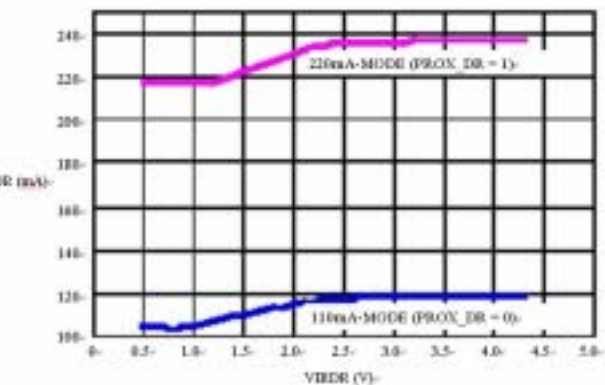
ANGULAR SENSITIVITY OF ALS PROX COUNTS VS DISTANCE

WITH 10cmx10cm REFLECTORS

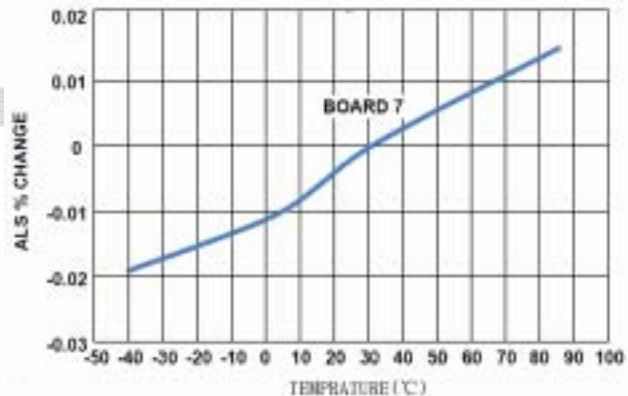


V<sub>DD</sub> VS I<sub>DD</sub> FOR VARIOUS MODES OF OPERATION

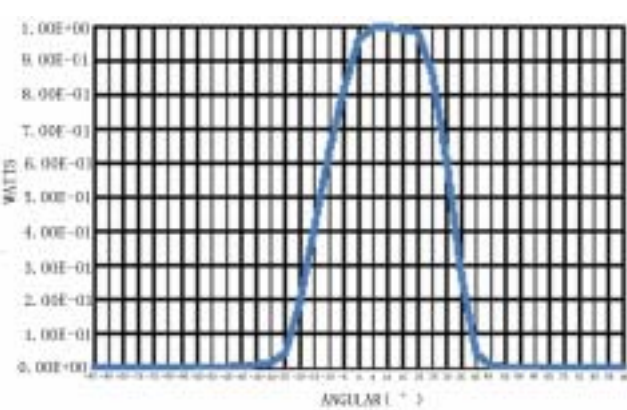
## 4.9 Typical Performance Curves



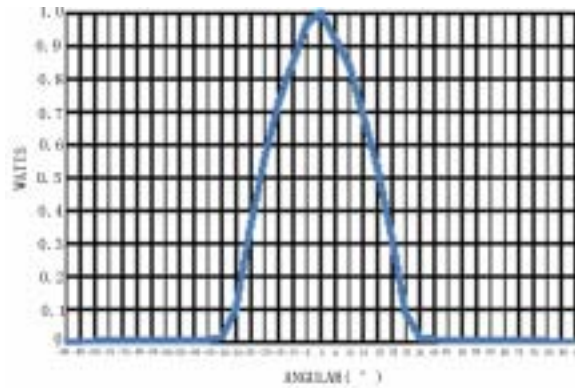
IRDR PULSE AMPLITUDE VS V<sub>IRDR</sub>



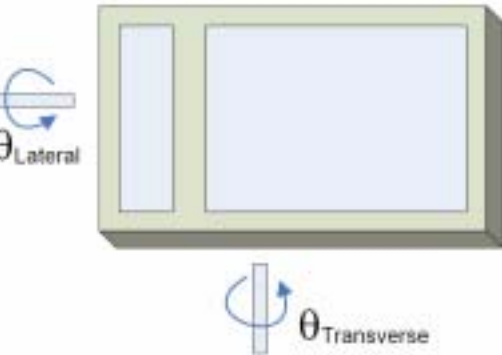
ALS RANGE1 OVER TEMP AT 75 LUX WHITE LED



RADIATION EMISSION PATTERN IRLED LATERAL



IR-LED TRANSVERSE EMISSION PATTERN (NORMALIZED INTENSITY VS  $\Theta_{TRANS}$ )



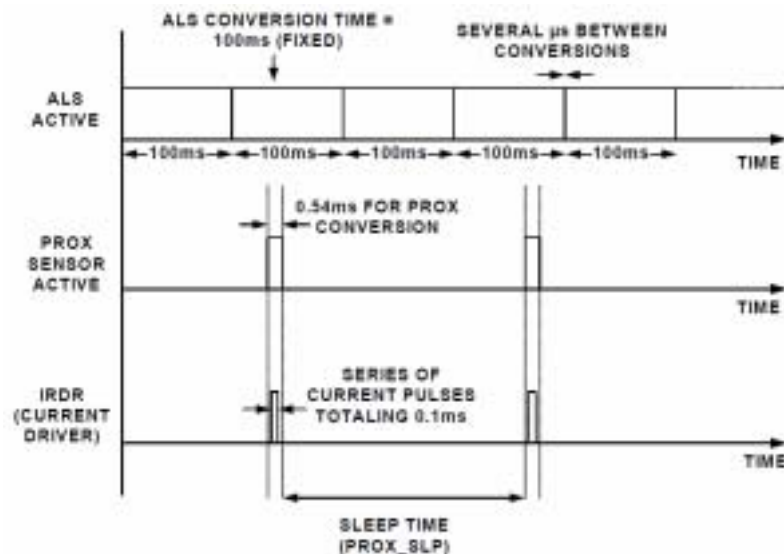
DEFINITION OF LATERAL AND TRANSVERSE AXES

## 5 Principles of Operation

### 5.1 Photodiodes and ADCs

The ORAP-29044 contains two photodiode arrays, which convert photons (light) into current. The ALS photodiodes are constructed to mimic the human eye's wavelength response curve to visible light. The ALS photodiodes' current output is digitized by a 12-bit ADC in 100ms. These 12 bits can be accessed by reading from I<sup>2</sup>C registers 0x9 and 0xA when the ADC conversion is completed.

The ALS converter is a charge-balancing, integrating 12-bit ADC. Charge-balancing is best for converting small current signals in the presence of periodic AC noise. Integrating over 100ms highly rejects both 50Hz and 60Hz light flicker by picking the lowest integer number of cycles for both 50Hz/60Hz frequencies.



TIMING DIAGRAM FOR PROX/ALS EVENTS - NOT TO SCALE

The proximity sensor is an 8-bit ADC that operates in a similar fashion. When proximity sensing is enabled, the IRDR pin will drive the internal infrared LED, the emitted IR reflects off an object (e.g., a human head) back into the ORAP-29044, and a sensor converts the reflected IR wave to a current signal in 0.54ms. The ADC subtracts the IR reading before and after the LED is driven (to remove ambient IR such as sunlight), and converts this value to a digital count stored in Register 0x8.

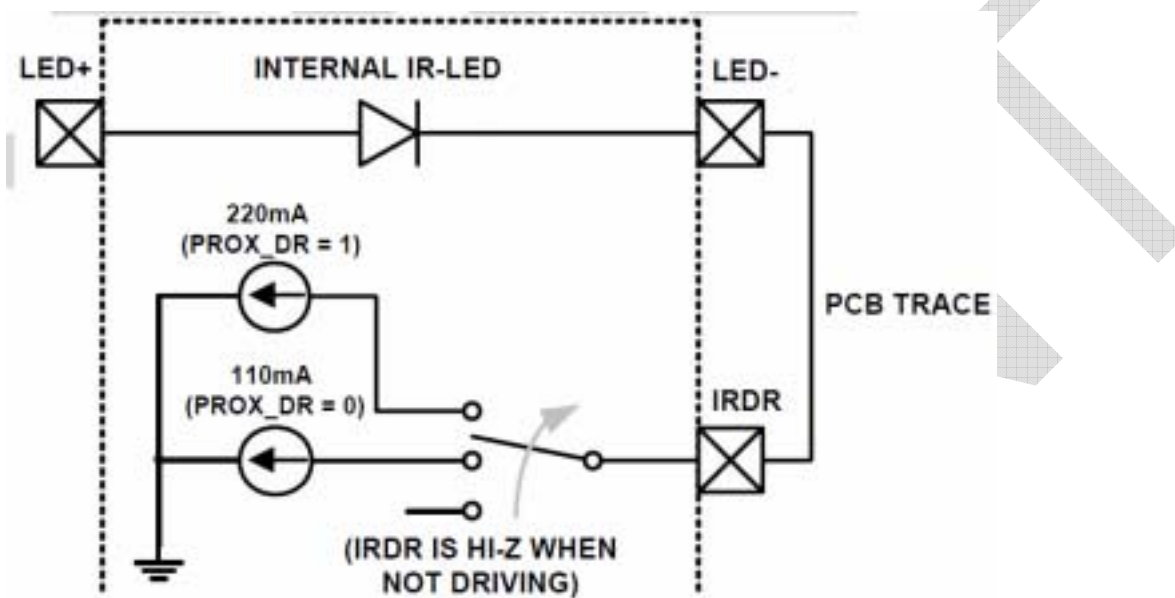
The ORAP-29044 is designed to run two conversions concurrently: a proximity conversion and an ALS (or IR) conversion. Please note that because of the conversion times, the user must let the ADCs perform one full conversion first before reading from I2C Registers PROX\_DATA (wait 0.54ms) or ALSIR\_DT1/2 (wait 100ms). The timing between ALS and Prox conversions is arbitrary. The ALS runs continuously with new data available every 100ms. The proximity sensor runs continuously with a time between conversions decided by PROX\_SLP (Register 1 Bits [6:4]).

## 5.2 Ambient Light and IR Sensing

The ORAP-29044 is set for ambient light sensing when Register bit ALSIR\_MODE = 0 and ALR\_EN = 1. ALS measuring mode (as opposed to IR measuring mode) is set by default. When the part is programmed for infrared (IR) sensing (ALSIR\_MODE = 1; ALS\_EN = 1), infrared light is converted into a current and digitized by the same ALS ADC. The result of an IR conversion is strongly related to the amount of IR energy incident on our sensor, but is unitless and is referred to in digital counts.

### 5.3 Proximity Sensing

When proximity sensing is enabled (PROX\_EN = 1), the internal IR LED is driven for 0.1ms by the built-in IR LED driver through the IRDR pin. The amplitude of the IR LED current depends on Register 1 bit 3: PROX\_DR. If this bit is low, the load will see a fixed 110mA current pulse. If this bit is high, the load on IRDR will see a fixed 220mA current pulse.



#### CURRENT DRIVE MODE OPTIONS

When the IR from the LED reaches an object and gets reflected back into the ORAP-29044, the reflected IR light is converted into current as per the IR spectral response shown in Figure 5. One entire proximity measurement takes 0.54ms for one conversion (which includes 0.1ms spent driving the LED), and the period between proximity measurements is decided by PROX\_SLP (sleep time) in Register 1 Bits 6:4.

Average LED driving current consumption is given by next Equation:

$$I_{IRDR:AVG} = \frac{I_{IRDR:PEAK} \times 100\mu s}{t_{SLEEP}}$$

A typical IRDR scheme is 220mA amplitude pulses every 800ms, which yields 28µA DC.

### 5.4 Total Current Consumption

Total current consumption is the sum of IDD and IIRDR. The IRDR pin sinks current and the average IRDR current can be calculated using the Equation. IDD depends on voltage and the mode-of-operation.





## 5.5 Interrupt Function

The ORAP-29044 has an intelligent interrupt scheme designed to shift some logic processing away from intensive microcontroller I<sup>2</sup>C polling routines (which consume power) and towards a more independent light sensor, which can instruct a system to “wake up” or “go to sleep”.

An ALS interrupt event (ALS\_FLAG) is governed by Registers 5 through 7. The user writes a high and low threshold value to these registers and the ORAP-29044 will issue an ALS interrupt flag if the actual count stored in Registers 0x9 and 0xA are outside the user’s programmed window. The user must write 0 to clear the ALS\_FLAG.

A proximity interrupt event (PROX\_FLAG) is governed by the high and low thresholds in registers 3 and 4 (PROX\_LT and PROX\_HT). PROX\_FLAG is set when the measured proximity data is more than the higher threshold X-times-in-a-row (X is set by user; see following paragraph). The proximity interrupt flag is cleared when the prox data is lower than the low proximity threshold X-times-in-a-row, or when the user writes “0” to PROX\_FLAG.

Interrupt persistency is another useful option available for both ALS and proximity measurements. Persistency requires X-in-a-row interrupt flags before the INT pin is driven low. Both ALS and Prox have their own independent interrupt persistency options. See ALS\_PRST and PROX\_PRST bits in Register 2.

The final interrupt option is the ability to AND or OR the two interrupt flags using Register 2 Bit 0 (INT\_CTRL). If the user wants both ALS/Prox interrupts to happen at the same time before changing the state of the interrupt pin, set this bit high. If the user wants the interrupt pin to change state when either the ALS or the Proximity interrupt flag goes high, leave this bit to its default of 0.

## 5.6 ALS Range 1 Considerations

When measuring ALS counts higher than 1800 on range 1 (ALSIR\_MODE = 0, ALS\_RANGE = 0, ALS\_DATA > 1800), switch to range 2 (change the ALS\_RANGE bit from “0” to “1”) and re-measure ALS counts. This recommendation pertains only to applications where the light incident upon the sensor is IR-heavy and is distorted by tinted glass that increases the ratio of infrared to visible light. For more information, please contact the factory.

## 5.7 V<sub>DD</sub> Power-up and Power Supply Considerations

Upon power-up, please ensure a V<sub>DD</sub> slew rate of 0.5V/ms or greater. After power-up, or if the user’s power supply temporarily deviates from our specification (2.25V to 3.63V), Orient recommends the user write the following: write 0x00 to register 0x01, write 0x29 to register 0x0F, write 0x00 to register 0x0E, and write 0x00 to register 0x0F. The user should then wait ~1ms or



more and then rewrite all registers to the desired values. If the user prefers a hardware reset method instead of writing to test registers: set  $V_{DD} = 0V$  for 1 second or more, power back up at the required slew rate, and write registers to the desired values.

## 5.8 Power-Down

To put the ORAP-29044 into a power-down state, the user can set both PROX\_EN and ALS\_EN bits to 0 in Register 1 or more; simply set all of Register 1 to 0x00.

## 5.9 Serial Interface

The ORAP-29044 supports the Inter-Integrated Circuit (I<sup>2</sup>C) bus data transmission protocol. The I<sup>2</sup>C bus is a two wire serial bidirectional interface consisting of SCL (clock) and SDA (data). Both the wires are connected to the device supply via pull-up resistors. The I<sup>2</sup>C protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The transmitting device pulls down the SDA line to transmit a “0” and releases it to transmit a “1”. The master always initiates the data transfer, only when the bus is not busy, and provides the clock for both transmit and receive operations. The ORAP-29044 operates as a slave device in all applications. The serial communication over the I<sup>2</sup>C interface is conducted by sending the most significant bit (MSB) of each byte of data first.

## 5.10 Start Condition

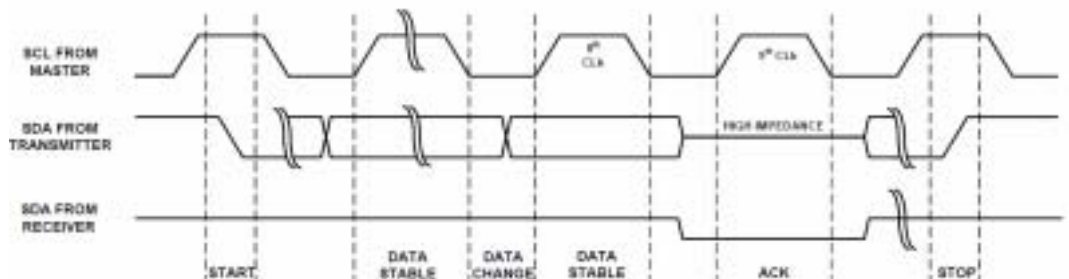
During data transfer, the SDA line must remain stable while the SCL line is HIGH. All I<sup>2</sup>C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ORAP-29044 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met. A START condition is ignored during the power-up sequence.

## 5.11 Stop Condition

All I<sup>2</sup>C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH. A STOP condition at the end of a read/write operation places the device in its standby mode. If a stop is issued in the middle of a Data byte, or before 1 full Data byte + ACK is sent, then the serial communication of ORAP-29044 resets itself without performing the read/write. The contents of the array are not affected.

## 5.12 Acknowledge

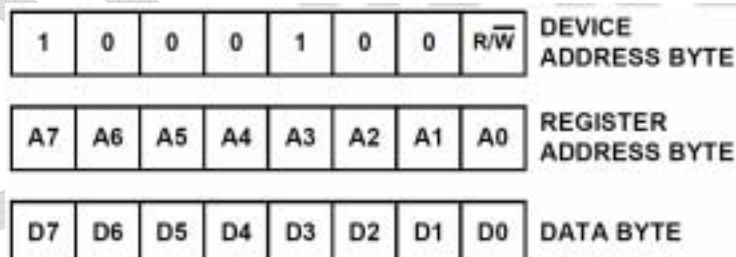
An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device releases the SDA bus after transmitting 8-bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data. The ORAP-29044 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again, after successful receipt of an Address Byte. The ORAP-29044 also responds with an ACK after receiving a Data byte of a write operation. The master must respond with an ACK after receiving a Data byte of a read operation.



START, DATA STABLE, ACKNOWLEDGE, AND STOP CONDITION

## 5.13 Device Addressing

Following a START condition, the master must output a Device Address byte. The 7 MSBs of the Device Address byte are known as the device identifier. The device identifier bits of ORAP-29044 are internally hard-wired as “1000100”. The LSB of the Device Address byte is defined as read or write (R/W) bit. When this R/W bit is a “1”, a read operation is selected and when “0”, a write operation is selected. The master generates a START condition followed by Device Address byte 1000100x (x as R/W) and the ORAP-29044 compares it with the internal device identifier. Upon a correct comparison, the device outputs an acknowledge (LOW) on the SDA line

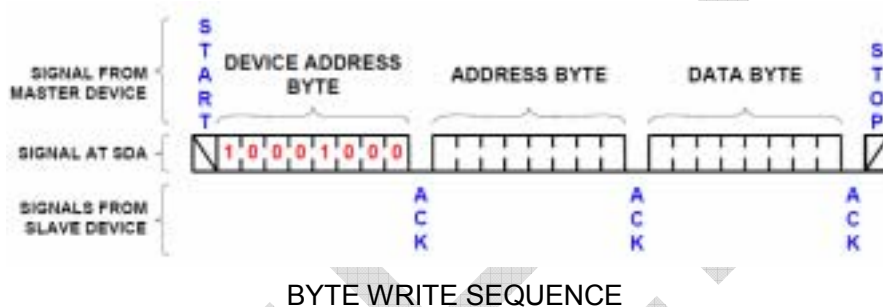


DEVICE ADDRESS, REGISTER ADDRESS, & DATA BYTE

## 5.14 Write Operation

### BYTE WRITE:

In a byte write operation, ORAP-29044 requires the Device Address byte, Register Address byte, and the Data byte. The master starts the communication with a START condition. Upon receipt of the Device Address byte, Register Address byte, and the Data byte, the ORAP-29044 responds with an acknowledge (ACK). Following the ORAP-29044 data acknowledge response, the master terminates the transfer by generating a STOP condition. ORAP-29044 then begins an internal write cycle of the data to the volatile memory. During the internal write cycle, the device inputs are disabled and the SDA line is in a high impedance state, so the device will not respond to any requests from the master



### BURST WRITE:

The ORAP-29044 has a burst write operation, which allows the master to write multiple consecutive bytes from a specific address location. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first Data byte is transferred, the master can write to the whole register array. After the receipt of each byte, the ORAP-29044 responds with an acknowledge, and the address is internally incremented by one. The address pointer remains at the last address byte written. When the counter reaches the end of the register address list, it “rolls over” and goes back to the first Register Address.

## 5.15 Read Operation

ORAP-29044 has two basic read operations: Byte Read and Burst Read.

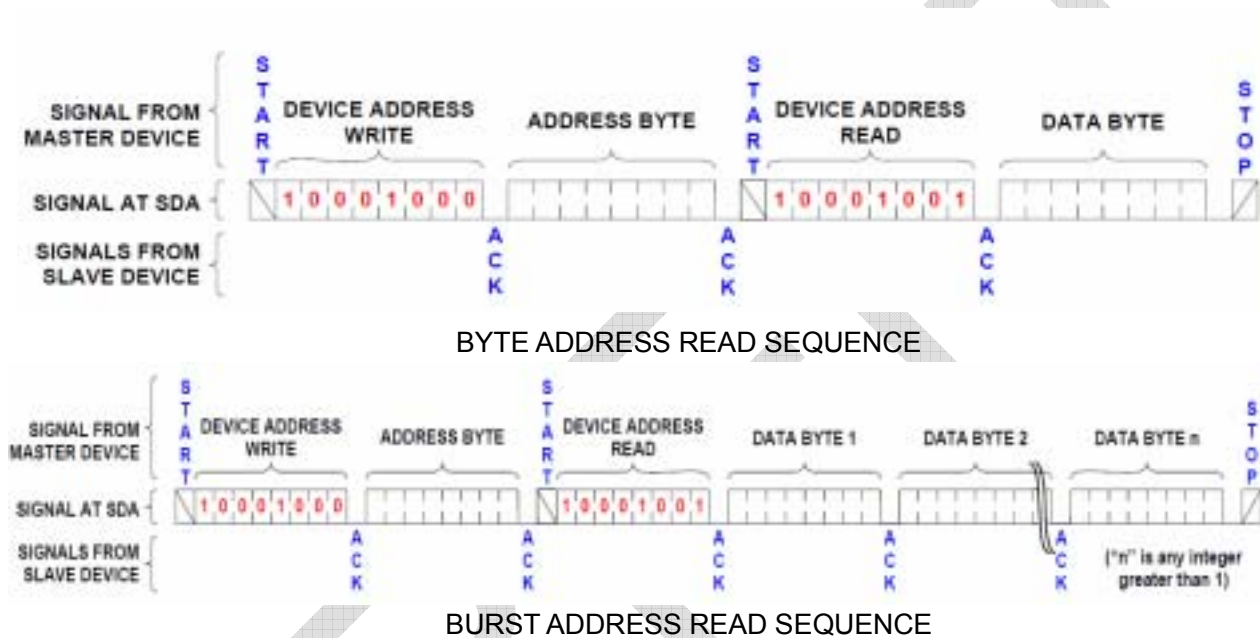
### Byte read:

Byte read operations allow the master to access any register location in the ORAP-29044. The Byte read operation is a two step process. The master issues the START condition and the Device Address byte with the R/W bit set to “0”, receives an acknowledge, then issues the Register Address byte. After acknowledging receipt of the register address byte, the master immediately issues another START condition and the Device Address byte with the R/W bit set to

“1”. This is followed by an acknowledge from the device and then by the 8-bit data word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition

## BURST READ:

Burst read operation is identical to the Byte Read operation. After the first Data byte is transmitted, the master responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge but issuing a STOP condition . For more information about the I<sup>2</sup>C standard, please consult the Philips™ I<sup>2</sup>C specification documents.



## 6 Register Map

Following are detailed descriptions of the control registers related to the operation of the ORAP-29044 ambient light sensor device. These registers are accessed by the I<sup>2</sup>C serial interface. For details on the I<sup>2</sup>C interface.

All the functionalities of the device are controlled by the registers. The ADC data can also be read. The following sections explain the details of each register bit. All RESERVED bits must be set to zero, unless otherwise specified.

### 6.1 Register Descriptions



address	Register name	bit								default
		7	6	5	4	3	2	1	0	
0x00	(n/a)									(n/a)
0x01	CONFIGURE	PROX_EN	PROX_SLP[2:0]		PROX_DR	ALS_EN	ALS_RANGE	ALSIR_MODE	0x00	
0x02	INTERRUPT	PROX_FLAG	PROX_PRST[1:0]	(Write 0)	ALS_FLAG	ALS_PRST[1:0]		INT_CTRL	0x00	
0x03	PROX_LT	PROX_LT[7:0]								0x00
0x04	PROX_HT	PROX_HT[7:0]								0xFF
0x05	ALSIR_TH1	ALSIR_TH1 [7:0]								0x00
0x06	ALSIR_TH2	ALSIR_HT[3:0]			ALSIR_LT[11:8]					0xF0
0x07	ALSIR_TH3	ALSIR_HT[11:4]								0xFF
0x08	PROX_DATA	PROX_DATA[7:0]								0x00
0x09	ALSIR_DT1	ALSIR_DATA[7:0]								0x00
0x0A	ALSIR_DT2	(Unused)			ALSIR_DATA[11:8]					0x00

Register (Address: 0x00)  
 COMMAND-I REGISTER ADDRESS

Register name	Access	Address	Register bit								default
			B7	B6	B5	B4	B3	B2	B1	B0	
N/A	RO	0x00									N/A

This is a reserved register. Do not write or read

Configure Register (Address: 0x01)

Register name	Access	Address	Register bit								default
			B7	B6	B5	B4	B3	B2	B1	B0	
Configure	RW	0x01	PROX_EN	PROX_S2	PROX_S1	PROX_X0	PROX_DR	ALS/IR_EN	ALS_RANGE	ALS/IRdata	0x00

The Configure register consists all of control bits for both ALS Sensing and Proximity Sensing. This register determines operation mode. The register has one Enable Prox sensing bit, three Proximity Sleep mode bits, one proximity current driver bit, one Enable ALS/IR sensing bit, one ALS/IR range bit, and one ALS/IR sensing data bits. The default register value is 0x00 at power on.



#### ALS/IR DATA BIT [B0]

The ALS/IR data mode bit is a select mode for fetching data from the data register (reg 0x09 and reg 0x0A). If B0 is set to 0, the ALS/IR data register will contain visible spectrum ALS sensing data. If B0 is set to 1, the ALS/IR data register will contain IR spectrum sensing data.

Bit0	Operation
0	Visible Spectrum ALS sensing data
1	IR Spectrum sensing data

#### FULL SCALE RANGE [B1]

The Full Scale Range (FSR) has two selectable ranges. Each range has a maximum allowable lux value. The higher the range value, the better the resolution and the wider the ALS lux value.

Bit1	RANGE(k)	FSR (LUX) @ VISIBLE ALS SENSING
0	Range1	125
1	Range2	2000

#### ALS/IR\_EN [B2]

The ALS/IR\_EN bit[B2] is the enable bit for both ALS sensing and IR sensing. If [B2] is 0, ALS sensing and IR sensing is disabled. If [B2] is 1, ALS sensing and IR sensing is enabled.

Bit2	Operation
0	Disable ALS sensing and IR sensing
1	Enable ALS sensing and IR sensing

#### PROX\_DR[B3]

PROX\_DR bit[B3] selects the IR driver current strength. The IR driver sinks current through the LDR pin. The drive capability can be programmed through [B3] either a pulse 110mA current sink or 220mA pulse current sink. The higher the amplitude, the better the range of detection.

Bit3	Operation
0	110mA current sink
1	220mA current sink



### PROX SLEEP MODE [B6,B5,B4]

ORAP-29044 is equipped with multiple sleep modes in proximity sensing. It is a good power saving feature. The different sleep modes can be selected by setting [B6-B4] bits on register 0x01. When proximity sensing is enabled, the ADC converts for 0.54ms and sleeps for 800ms by default.

The next lists the possible operating sleep modes.

Bit4	Bit5	Bit6	SLEEP TIME OPERATION(msec)
0	0	0	800(default)
0	0	1	400
0	1	0	200
0	1	1	100
1	0	0	75
1	0	1	50
1	1	0	12.5
1	1	1	0.0 (Sleep Mode Disabled)

### PROX\_EN[B7]

Proximity is enabled when PROX\_EN[B7] is set to high.

Bit7	CURRENT DRIVER OPERATION
0	Disable proximity sensing (Default)
1	Enable proximity sensing

### Interrupt Register (Address: 0x02)

Register name	Access	Address	Register bit								default
			B7	B6	B5	B4	B3	B2	B1	B0	
INTERRUPT	RW	0x02	PROX_FLG	PROX_PRST1	PROX_PRST0	0	ALS/IR_F LAG	ALS/IR_P RST1	ALS/IR_P RSST0	INT_CTRL	0x00

The Interrupt register consists of all status bits. The ORAP-29044 has an interrupt scheme





designed for both ALS/IR sensing and Proximity logic detection sensing. The register has one proximity sensing flag bit, two proximity sensing persistent bits, one ALS/IR sensing flag bit and two ALS/IR persistent bits. The default register value is 0x00.

**INT\_CTRL[B0]:**

INT\_CTRL [B0] can be programmed to cause an interrupt when either ALS\_FLAG or PROX\_FLAG go high or when both go high. Writing '0' will do a logical OR and a one will do a logical AND. The INT pin is open-drain therefore, in this INT\_CTRL bit, there are two options to make the INT pin go low. Once the interrupt is triggered, the INT pin goes low if the PROX\_FLAG bit or ALS\_FLAG goes high in logic OR option. Otherwise, the interrupt is triggered and the INT pin goes low if the PROX\_FLAG bit and ALS\_FLAG go high in logic AND option. Both the INT pin and these interrupt status bits are automatically cleared when writing '0' to those flag bits.

Bit0	OPERATION
0	Logical OR
1	Logical AND

**ALS/IR INTERRUPT PERSIST BITS [B2,B1]**

The interrupt persist bits[B2LOL,B1] provide control when interrupts occur. There are four different selections for this feature. A value of N (where N is 1, 4, 8, and 16) results in an interrupt only if the value remains outside the threshold window for N consecutive integration cycles. For example, if N is equal to 8 and the integration time is 100ms. An interrupt is generated whenever the last conversion results in a value outside of the programmed threshold window.

INTERRUPT PERSIST BITS

Bit1	Bit2	NUMBER OF INTEGRATION CYCLES (n)
0	0	1
0	1	4
1	0	8
1	1	16

**ALS\_FLAG BIT [B3]**

The ALS\_FLAG[B3] bit is a status bit for light intensity detection. The bit is set to logic HIGH when the light intensity result at (register 0x09, 0x0A) crosses the interrupt threshold's window (register address 0x05 - 0x07), and is set to logic LOW when its within the interrupt threshold's window. Once the interrupt is triggered, the ALS\_FLAG bit goes HIGH. The ALS/IR\_FLAG bit is cleared by writing '0' to [B3].

Bit3	OPERATION
0	Interrupt is cleared or not triggered yet



1	Interrupt is triggered
---	------------------------

#### PROXIMITY INTERRUPT PERSIST BITS [B6,B5]

The interrupt persist bits provide control over when interrupts occur. There are four different selections for this feature. A value of N (where N is 1, 4, 8, and 16) results in an interrupt only if the value remains above the PROX\_HT (reg0x04) threshold for N consecutive integration. At that moment, the PROX\_FLAG is high and remains asserted until cleared by writing the '0' to PROX\_FLAG bit or if the value is below PROX\_LT (reg0x03) threshold for N consecutive integration, it will also clear the PROX\_FLAG.

For example, if N is equal to 8, then an interrupt is generated whenever the last conversion results in a value above the PROX\_HT threshold, then PROX\_FLAG = 1. There are two ways of clearing the PROX\_FLAG. You can write a 0h to Reg0x02 to manually clear the flag, or if the conversion results are less than the PROX\_LT value, upon completion of the measurement, the Reg0x02 will be set to 0h and thus, the PROX\_FLAG will be automatically cleared.

#### PROXIMITY LOGIC PERSIST BITS

Bit6	Bit5	NUMBER OF INTEGRATION CYCLES (n)
0	0	1
0	1	4
1	0	8
1	1	16

#### PROX\_FLAG BIT [B7]

PROX\_FLAG bit [B7] is a status bit for IR light intensity detection. [B7] is set to logic HIGH when the IR light intensity reflected from the object to the sensor(register 0x08) crosses the PROX\_HT(register address 0x04), and if [B7] is set to logic LOW when the IR light intensity goes lower than PROX\_LT (register address 0x03) or to clear by writing '0' to PROX\_FLAG.

Bit7	OPERATION
0	Logic Low (Far)
1	Logic High (Near)

#### PROX\_TL Registers (Address: 0x03)

#### PROX\_TL REGISTER BITS

Register name	Access	Addresses	Register bit								default
			B7	B6	B5	B4	B3	B2	B1	B0	



PROX_LT	RW	0x03	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0	0x00
---------	----	------	-----	-----	-----	-----	-----	-----	-----	-----	------

The lower interrupt threshold registers are used to set the lower trigger point for interrupt generation. If the Prox value crosses below or is equal to the lower threshold, it will be clear the last state of Interrupt. For example, if PROX\_FLAG is high at the last state then the proximity value is below the PROX\_LT threshold and the PROX\_FLAG will go low at this moment. The register defaults to 0x00 on power up.

PROX\_TH Registers (Address: 0x04)

PROX\_TH REGISTER BITS

Register name	Access	Address	Register bit								default
			B7	B6	B5	B4	B3	B2	B1	B0	
PROX_TH	RW	0x04	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0	0xFF

The upper proximity threshold registers are used to set the upper trigger point for Logic HIGH(Near). If the Prox value crosses above or is equal to the upper threshold, a Logic HIGH(Far) is asserted on the interrupt flag. Registers PROX\_HT(0x04) are set to upper threshold. 0x04 register is defaulted to 0xFF on power up.

ALS\_TH1 & ALS\_TH2 Registers (Address: 0x05 & 0x06[B3,B2,B1,B0])

INTERRUPT THRESHOLD LOW REGISTER BITS

Register name	Access	Address	Register bit								default
			B7	B6	B5	B4	B3	B2	B1	B0	
ALS_TH2_MSB	RW	0x06					TL3	TL2	TL1	TL0	0x00
ALS_TH1_LSB	RW	0x05	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0	0x00

The lower interrupt threshold registers are used to set the lower trigger point for interrupt generation. If the ALS value crosses below or is equal to the lower threshold, an interrupt is asserted on the interrupt flag. An 8-bit RW Register ALS\_TH1(0x05) and a nibble ALS\_TH2(0x06[B3,B2,B1,B0]) provide the low and high bytes, respectively, of the lower interrupt threshold. The high and low bytes from each set of registers are combined to form a 12-bit threshold value. The interrupt threshold registers default to 0x00 on power up.

ALS\_TH2 & ALS\_TH3 Registers (Address: 0x06[B7,B6,B5,B4] & 0x07)

INTERRUPT THRESHOLD HIGH REGISTER BITS

Register name	Access	Address	Register bit								default
			B7	B6	B5	B4	B3	B2	B1	B0	
ALS_TH2_	RW	0x06	TH7	TH6	TH5	TH4					0xF0



LSB											
ALS_TH3_ MSB	RW	0x07	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0	0xFF

The upper interrupt threshold registers are used to set the upper trigger point for interrupt generation. If the ALS value crosses above or is equal to the upper threshold, an interrupt is asserted on the interrupt pin and the interrupt flag. A nibble RW Register ALS\_TH(0x06[B7,B6,B5,B4]) and an 8-bit RW ALS\_TH3(0x07) provide the low and high bytes, respectively, of the upper interrupt threshold. The high and low bytes from each set of registers are combined to form a 12-bit threshold value. The interrupt threshold registers default to 0xFF on power up.

Data Registers (Addresses: 0x08)

ADC REGISTER BITS

Register name	Access	Address	Register bit								default
			B7	B6	B5	B4	B3	B2	B1	B0	
DATA	RO	0x08	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0	0x00

The ORAP-29044 has 8-bit read-only registers to hold the ADC value. The upper byte is accessed at address 0x03 and the lower byte is accessed at address 0x02. The registers are refreshed after every conversion cycle. The default register value is 0x00 at power on.

Data Registers (Addresses: 0x09 & 0x0A)

ADC REGISTER BITS

Register name	Access	Address	Register bit								default
			B7	B6	B5	B4	B3	B2	B1	B0	
DATALSB	RW	0x09	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0	0x00
DATAMSB	RW	0x0A					Data11	Data10	Data9	Data8	0x00

The ORAP-29044 has one 8-bit read-only register to hold the lower, and one nibble (4-bit read only) to hold the upper of the ADC value. The nibble (4-bit read only) is accessed at address 0x0A and the lower byte is accessed at address 0x09. For 12-bit resolution, the data is from Data0 to Data11. The registers are refreshed after every conversion cycle. The default register value is 0x00 at power on.



## 7 Applications Information

### 7.1 Calculating Lux

The ORAP-29044's ADC output codes are directly proportional to lux when in ALS mode (see ALSIR\_MODE bit).

$$E_{\text{calc}} = \alpha_{\text{RANGE}} \times \text{OUT}_{\text{ADC}}$$

In the Equation ,  $E_{\text{calc}}$  is the calculated lux reading and OUT represents the ADC code. The constant  $\alpha$  to plug in is determined by the range bit ALS\_RANGE (register 0x1 bit 1) and is independent of the light source type.

ALS SWNSITIVITY DIFFERENT RANGES

ALS_RANGE	$\alpha_{\text{RANGES}}$ (Lux/Count)
0	0.0326
1	0.522

Which shows two different scale factors: one for the low range (ALS\_RANGE = 0) and the other for the high range (ALS\_RANGE = 1).

### 7.2 Noise Rejection

Charge balancing ADC's have excellent noise-rejection characteristics for periodic noise sources whose frequency is an integer multiple of the conversion rate. For instance, a 60Hz AC unwanted signal's sum from 0ms to  $k \cdot 16.66\text{ms}$  ( $k = 1, 2, \dots, k_i$ ) is zero. Similarly, setting the device's integration time to be an integer multiple of the periodic noise signal greatly improves the light sensor output signal in the presence of noise. Since wall sockets may output at 60Hz or 50Hz, our integration time is 100ms: the lowest common integer number of cycles for both frequencies.



## 7.3 Proximity Detection of Various Objects

Proximity sensing relies on the amount of IR reflected back from objects. A perfectly black object would absorb all light and reflect no photons. The ORAP-29044 is sensitive enough to detect black ESD foam, which reflects only 1% of IR. For biological objects, blonde hair reflects more than brown hair and customers may notice that skin tissue is much more reflective than hair. IR penetrates into the skin and is reflected or scattered back from within. As a result, the proximity count peaks at contact and monotonically decreases as skin moves away. The reflective characteristics of skin are very different from that of paper.

## 7.4 Suggested PCB Footprint

It is important that users check the “Surface Mount Assembly Guidelines for Optical Dual FlatPack No Lead (ODFN) Package” before starting ODFN product board mounting. You can refer to the assumption diagram what is offered to Orent, if you have some question , you can contact “hejun03230311@613.com “ for supporting.

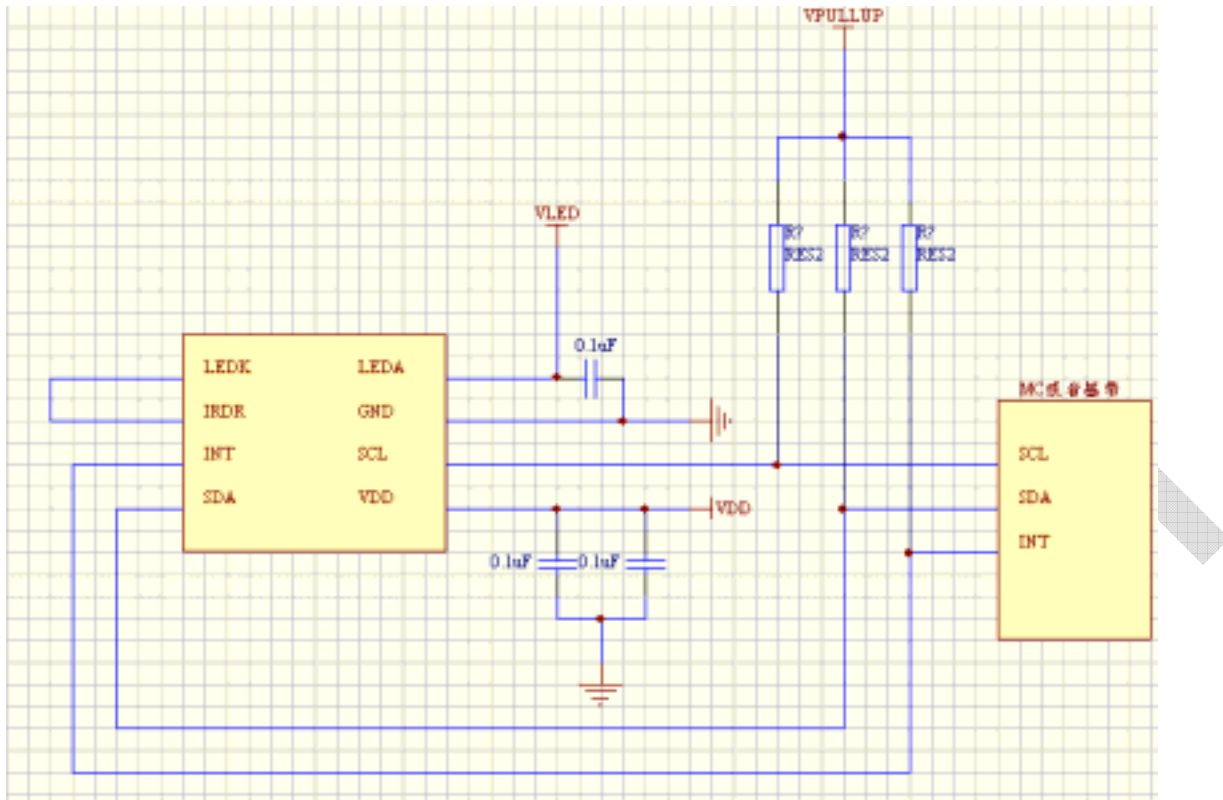
## 7.5 Layout Considerations

The ORAP-29044 is relatively insensitive to layout. Like other I<sup>2</sup>C devices, it is intended to provide excellent performance even in significantly noisy environments. There are only a few considerations that will ensure best performance.

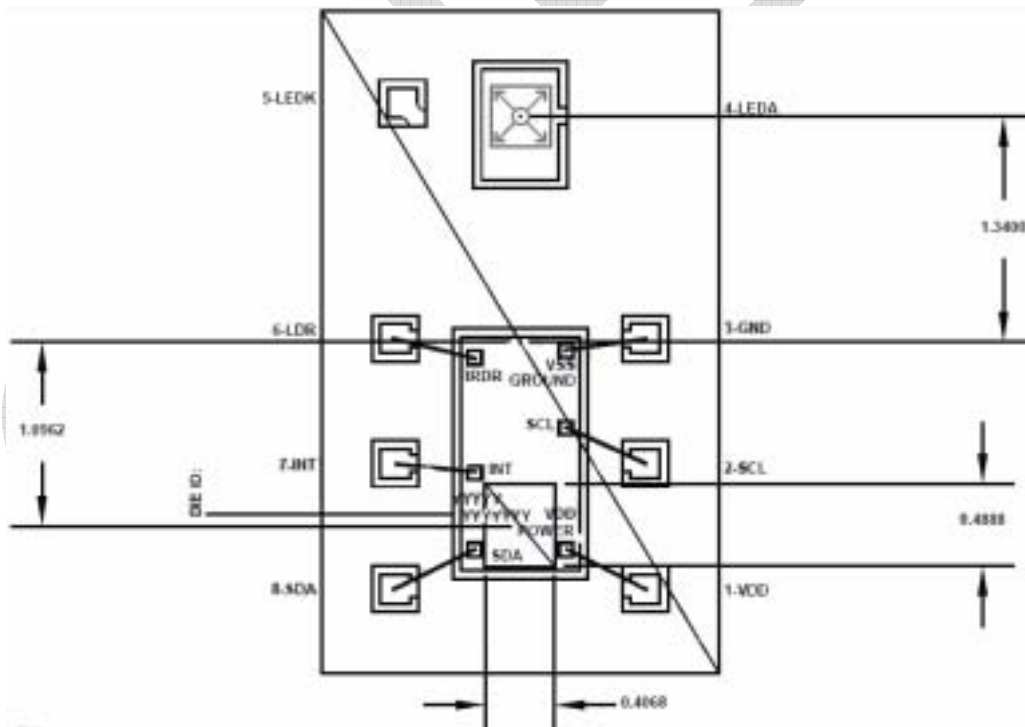
Route the supply and I<sup>2</sup>C traces as far as possible from all sources of noise. 0.1μF and 1μF power supply decoupling capacitors need to be placed close to the device.

## 7.6 Typical Circuit

A typical application for the ORAP-29044 is shown in next Figure . **The ORAP-29044's I<sup>2</sup>C address is internally hardwired as 0b1000100.** The device can be tied onto a system's I2C bus together with other I<sup>2</sup>C compliant devices.



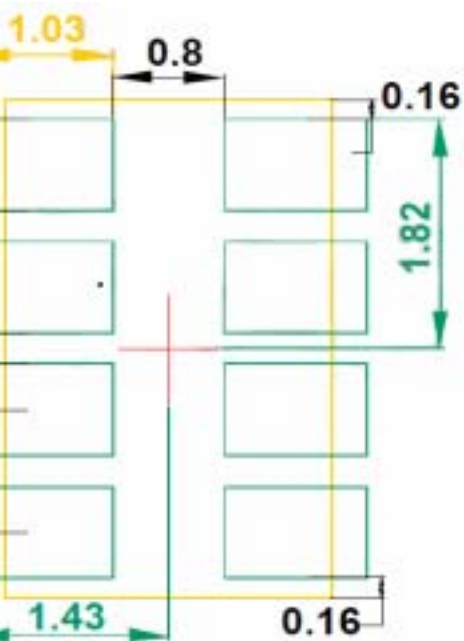
ORAP-29044 TYPICAL CIRCUIT



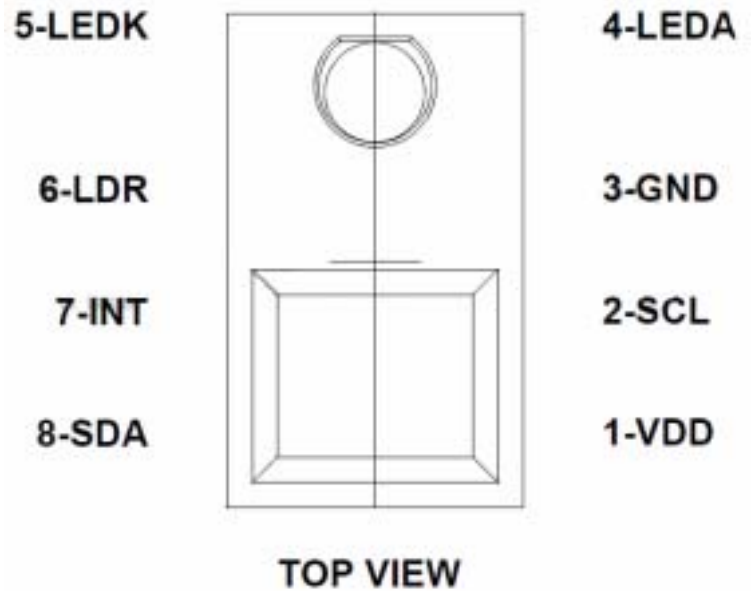
Optical sensor location







TYPICAL RECOMMENDED LAND PATTERN



## 9 Product

Orient includes Shenzhen Orient Technology, Orient Opto-Electronics, Orient Components and Jiangmen Orient Opto-Electronics Co., Ltd. The product line covers LED Epi-wafer, LED Chip, Packaging and applied products such as comprehensive series of LED Chips, SMD LED (0603, 0605, 0805), Dot matrix, Photocoupler, Digital Displays, Opto Interrupter and RGB full color Panel, etc.

Orient always sets the technical innovation as its core competitiveness, sustains tremendous investment in R&D and fosters a strong R&D team. We adhere to international manufacturing norms and quality standards to provide the most competitive products to our customers. The company has passed ISO9001 quality system certificate and products have passed the domestic and international security certificates such as UL, CE, VDE, SGS, CQC and RoHS .

Orient is not only a provider of low-carbon products, but also an advocate of low-carbon lifestyle. What's more, it is the leader of the sustainable development of the industry. People of Orient abide by the idea of Cooperation, Diligence, Pragmatism and Customer First and endeavor to create a new LED industry era.



## 企业荣誉

卓越品质，资质为证。

我们追求的不仅仅是荣誉，更要求客户的认可。

奥伦德视品质如生命，以创新为宗旨，尽心尽力，孜孜不倦，为民族光电事业贡献自己的光和热。

