

## 1. Description

The HS3205T is the N-Channel logic enhancement mode power field effect transistors , using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance.

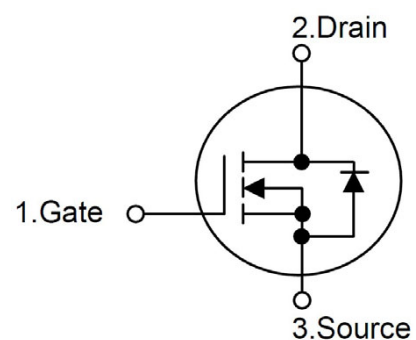
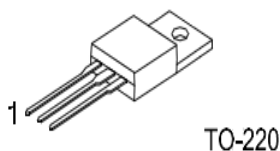
## 2. Feature

- $R_{DS(on)} \leq 8.0 \text{ m}\Omega @ V_{GS}=10\text{V}$
- Super high density cell design for extremely low  $R_{DS(on)}$
- Exceptional on-resistance and maximum DC current capability

$V_{DS}$	55	V
$R_{DS(on)}$	8.0	m $\Omega$
$I_D$	106.6	A

## 3. Pin configuration

Order Number	Package
HS3205T	TO-220



#### 4. Absolute maximum ratings (T<sub>c</sub>=25°C Unless Otherwise Noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V <sub>DSS</sub>	55	V
Gate-Source Voltage		V <sub>GSS</sub>	±20	V
Continuous Drain Current*	T <sub>c</sub> =25°C	I <sub>D</sub>	106.6	A
	T <sub>c</sub> =70°C		89.2	
Pulsed Drain Current		I <sub>DM</sub>	426	A
Maximum Power Dissipation	T <sub>c</sub> =25°C	P <sub>D</sub>	200	W
	T <sub>c</sub> =70°C		140	
Operating Junction Temperature		T <sub>J</sub>	-55 to 175	°C

#### 5. Thermal characteristics

Parameter	Symbol	Ratings	Units
Thermal resistance, case-to-sink typ.	R <sub>thCS</sub>	0.5	°C/W
Thermal resistance junction-case	R <sub>thJC</sub>	0.75	°C/W

## 6. Electrical characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μA	55			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA	3.0		5.0	V
I <sub>GSS</sub>	Gate Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =55V, V <sub>GS</sub> =0V			1	μA
R <sub>DS(ON)</sub>	Drain-Source On-Resistance <sup>a</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =62A		6.6	8.0	mΩ
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =62A, V <sub>GS</sub> =0V		0.9	1.2	V
<b>DYNAMIC</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =44V, V <sub>GS</sub> =10V, I <sub>D</sub> =62A		91		nC
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =44V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =62A		28		
Q <sub>gs</sub>	Gate-Source Charge			41		
Q <sub>gd</sub>	Gate-Drain Charge			18		
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz		6330		pF
C <sub>oss</sub>	Output Capacitance			495		
C <sub>rss</sub>	Reverse Transfer Capacitance			154		
R <sub>g</sub>	Gate-Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz		2.4		Ω
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DS</sub> =28V, R <sub>L</sub> =28Ω, V <sub>GS</sub> =10V, R <sub>G</sub> =6Ω		55		ns
t <sub>r</sub>	Turn-On Rise Time			12		
t <sub>d(off)</sub>	Turn-Off Delay Time			90		
t <sub>f</sub>	Turn-Off Fall Time			16		

Notes :a. pulse test:pulse width≤300 us,duty cycle≤2% ,Guaranteed by design,not subject to production testing.

b. HOMSEMI reserves the right to improve product design,functions and reliability without notice.