HS20P06DA

P channel MOSFET

1. Description

The HS20P06DA is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

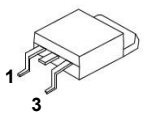
2. Feature

- $R_{DS(ON)} \leqq 78m\Omega @ V_{GS}=-10V$
- $R_{DS(ON)} \leqq 100m\Omega @ V_{GS}=-4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

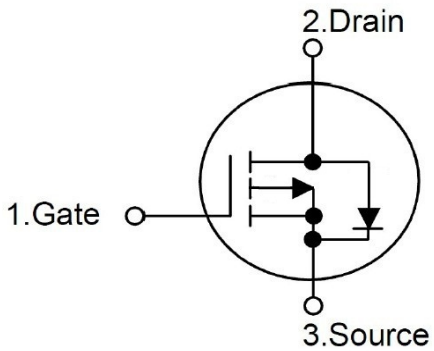
V_{DS}	-60	V
$R_{DS(on)}$	78	mΩ
I_D	-17.7	A

3. Pin configuration

Order Number	Package
HS20P06DA	TO-252



TO-252



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4. Absolute maximum ratings (TC= 25 ºC, unless otherwise specified)

Parameter		Symbol	Ratings	Units
Drain-source voltage		V_{DSS}	-60	V
Gate-source voltage		V_{GSS}	±20	V
Continuous Drain Current (Tj=150°C)	T_c =25°C	I_D	-17.7	A
	T_c =70°C		-14.1	A
Drain current pulsed		I_{DP}	-71	A
Maximum Power Dissipation	T_c=25°C	P_D	39.1	W
	T_c=70°C		25	W
Junction temperature		T_J	+150	°C
Storage temperature		T_{STG}	-50~+150	°C

5. Thermal characteristics

Parameter	Symbol	Ratings	Units
Thermal resistance, case to sink typ	R_{thCS}	0.5	°C/W
Thermal resistance junction to case	R_{thJC}	3.2	°C/W

6. Electrical characteristics (T_J=25°C,unless otherwise specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1		-3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-60V, V_{GS}=0V			1	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance[a]	V_{GS}=-10V, I_D= -20A		65	78	mΩ
		V_{GS}=-4.5V, I_D= -16A		80	100	
V_{SD}	Diode Forward Voltage	I_S=-20A, V_{GS}=0V		1	1.2	V
DYNAMIC						
Qg	Total Gate Charge(10V)	V_{DS}=-30V, V_{GS}=-10V, I_D=-20A		22		nC
Qg	Total Gate Charge(4.5V)	V_{DS}=-30V, V_{GS}=-4.5V, I_D=-20A		10		
Qgs	Gate-Source Charge			6.3		
Qgd	Gate-Drain Charge			5		
Ciss	Input capacitance	V_{DS}=-15V, V_{GS}=0V, F=1MHz		958		pF
Coss	Output Capacitance			100		
Crss	Reverse Transfer Capacitance			33		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-15V, R_L =15Ω I_D=-1A, V_{GEN}=-10V, R_G=3Ω		36		ns
t_r	Turn-On Rise Time			16		
$t_{d(off)}$	Turn-Off Delay Time			53		
t_f	Turn-On Fall Time			6		

Note :a. Pulse test: pulse width 300μs, duty cycle 2% , Guaranteed by design , not subject to production testing.

b. Homsemi reserves the right to improve product design , functions and reliability without notice.

