HOMSEMI
SEMICONDUCTOR

HS25N06DA

N channel MOSFET

1. Description

The HS25N06DA is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

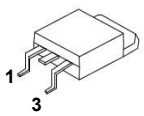
2. Feature

- $R_{DS(ON)} \leqq 62m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leqq 86m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

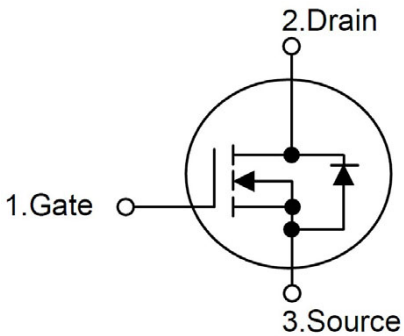
V_{DS}	60	V
$R_{DS(on)}$	62	mΩ
I_D	16	A

3. Pin configuration

Order Number	Package
HS25N06DA	TO-252



TO-252



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4. Absolute maximum ratings (TA=25℃ Unless Otherwise Noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		VDSS	60	V
Gate-Source Voltage		VGSS	±25	V
Continuous Drain Current(Tj=150℃)	Tc=25℃	ID	16	A
	Tc=70℃		13	
Pulsed Drain Current		IDM	65	A
Maximum Power Dissipation	Tc=25℃	PD	25	W
	Tc=70℃		16	
Operating Junction Temperature		TJ	-55 to 150	℃

5. Thermal characteristics

Parameter	Symbol	Ratings	Units
Thermal resistance, case-to-sink typ.	R_{thCS}	0.5	°C/W
Thermal resistance junction-case	R_{thJC}	5	°C/W

6. Electrical characteristics (TA=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	60			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1		3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V			1	μA
		V_{DS}=60V, V_{GS}=0V,T_J=55℃			10	
$R_{DS(ON)}$	Drain-Source On-Resistance [a]	V_{GS}=10V, I_D= 15A		52	62	mΩ
		V_{GS}=4.5V, I_D= 10A		70	86	
V_{SD}	Diode Forward Voltage	I_S=15A, V_{GS}=0V		1		V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=48V, V_{GS}=10V, I_D=16A		17		nC
Qgs	Gate-Source Charge			4.2		
Qgd	Gate-Drain Charge			5		
Rg	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		0.6		Ω
Ciss	Input Capacitance	V_{DS}=30V, V_{GS}=0V, f=1MHz		523		pF
Coss	Output Capacitance			47		
Crss	Reverse Transfer Capacitance			14		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=30V, R_L=15Ω I_D=1A, V_{GEN}=10V R_G=3Ω		11		ns
tr	Turn-On Rise Time			13		
$t_{d(off)}$	Turn-Off Delay Time			34		
tf	Turn-Off Fall Time			4		

Notes :a. pulse test:pulse width≦300 us,duty cycle≦2% ,Guaranteed by design,not subject to production testing.

b.Homsemi reserves the right to improve product design,functions and reliability without notice.

