

1. Description

The HS15N10DA is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

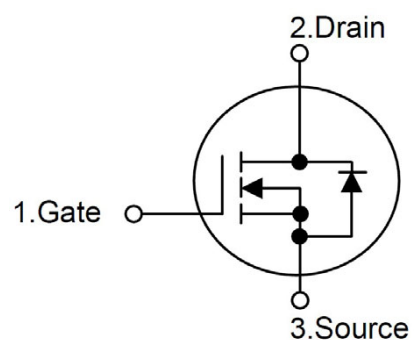
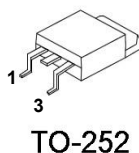
2. Feature

- $R_{DS(ON)} \leq 100m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

V_{DS}	100	V
$R_{DS(on)}$	100	m Ω
I_D	14.7	A

3. Pin configuration

Order Number	Package
HS15N10DA	TO-252



4. Absolute maximum ratings (T_A=25°C Unless Otherwise Noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V _{DSS}	100	V
Gate-Source Voltage		V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	T _C =25°C	I _D	14.7	A
	T _C =70°C		13.6	
Pulsed Drain Current		I _{DM}	59	A
Maximum Power Dissipation	T _C =25°C	P _D	34.7	W
	T _C =70°C		22.2	
Operating Junction Temperature		T _J	-55 to 150	°C

5. Thermal characteristics

Parameter	Symbol	Ratings	Units
Thermal resistance, case-to-sink typ.	R _{thCS}	3.6	°C/W
Thermal resistance junction-case	R _{thJC}	5	°C/W

6. Electrical characteristics (TA=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250 μA	100			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250 μA	1		3	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V			1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =10V, I _D = 8A		80	100	mΩ
V _{SD}	Diode Forward Voltage	I _S =8A, V _{GS} =0V		0.9	1.2	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =80V, V _{GS} =10V, I _D =10A		24		nC
Q _g	Total Gate Charge	V _{DS} =80V, V _{GS} =4.5V, I _D =10A		13		
Q _{gs}	Gate-Source Charge			4.6		
Q _{gd}	Gate-Drain Charge			7.6		
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz		890		pF
C _{oss}	Output Capacitance			58		
C _{rss}	Reverse Transfer Capacitance			23		
R _g	Gate-Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		0.9		Ω
t _{d(on)}	Turn-On Delay Time	V _{DS} =50V, R _L =5Ω, V _{GEN} =10V, R _G =1Ω		14		ns
t _r	Turn-On Rise Time			33		
t _{d(off)}	Turn-Off Delay Time			39		
t _f	Turn-Off Fall Time			5		

Notes :a. pulse test:pulse width ≤ 300 us,duty cycle ≤ 2% ,Guaranteed by design,not subject to production testing.

b.Homsemi reserves the right to improve product design,functions and reliability without notice.