2.4GHz FSK/MSK/ASK/OOK 收发模块

1.Description

CC2500+PA+LNA is a FSK/ASK/OOK/MSK Transceiver module.It provides extensive hardware support for packet handling ,data buffering ,burst transmissions ,clear channel assessment, link quality indication and wake on radio . It 's data stream can be manchester coded by the modulator and decoded by the demodulator .It has a high performance and easily to design your product .It can be used in 2400-2483.5MHz ISM/SRD band systems,Consumer Electronics, Wireless game controllers,Wireless audio and others wireless systems.

we support the frequency have 2400-2483.5MHz ISM Band modules now,

一般描述

CC2500+PA+LNA 是集 FSK/ASK/OOK/MSK.调制方式于一体的收发模块。它提供扩展硬件支持实现信息包处理、数据缓冲、群发射、空闲信道评估、链接质量指示和无线电波唤醒，可以采用曼彻斯特编码进行调制解调它的数据流。性能优越并且易于应用到你的产品设计中，它可以应用于 2400-2483.5MHz ISM/SRD 频段的系统，消费类电子产品、无线游戏控制器、无线音频传输和其他的无线系统中。

我们目前有支持 2400-2483.5MHz 范围的 ISM 频段的模块。

2. Features 基本特征

- Low current consumption. ●低电流损耗
- Easy for application. ●方便投入应用
- Efficient SPI interface ●高效的串行编程接口
- Operating temperature range ●工作温度范围：－ 40℃～＋85℃
- Operating voltage ●工作电压：1.8~ 3.6 Volts.
- Available frequency at ●有效频率：2.4-2.483GHz
- Programmable output power and hi sensitivity ●灵敏度高、输出功率可编程

3. BOM list for the modules:

N/A

4. Schematic Diagram

N/A

5. Pin Descriptions 管脚描述

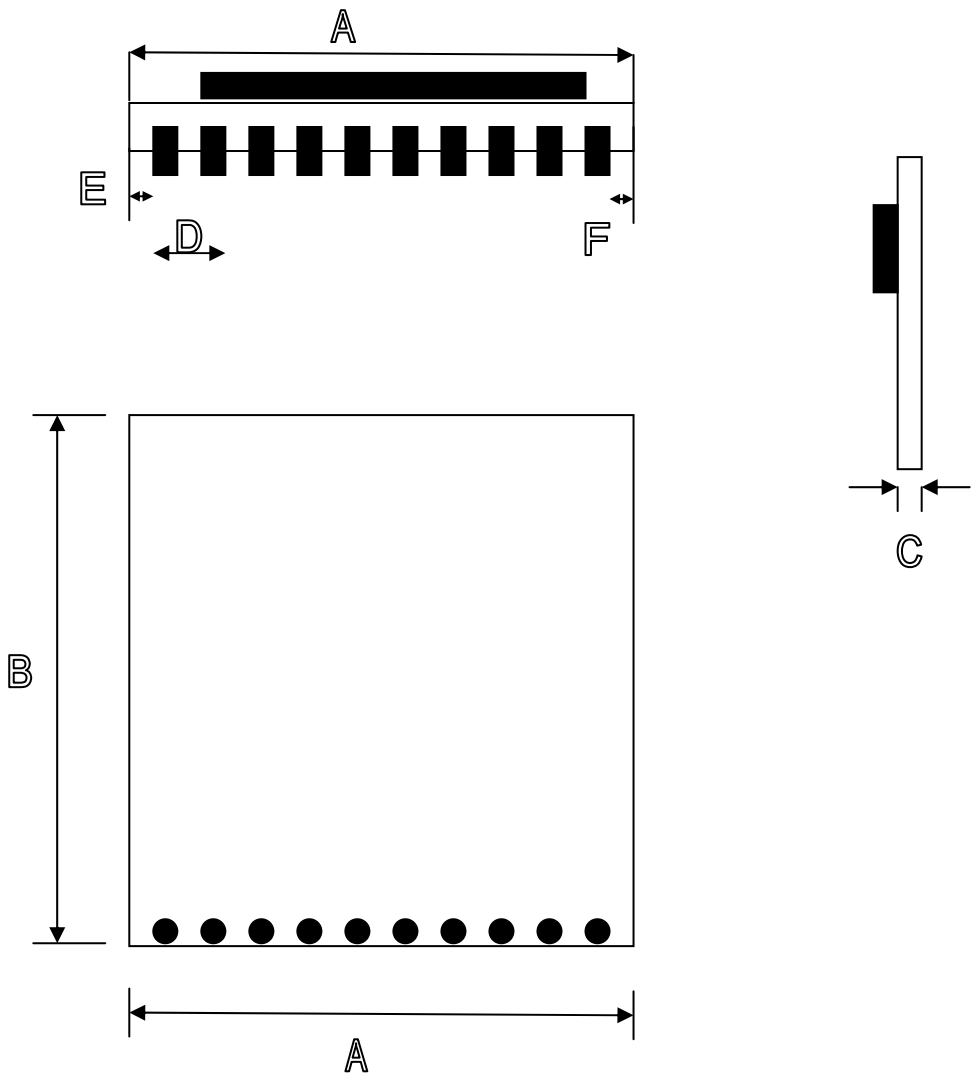
Pin No	Pin Name	Pin Type	Description 一般描述
1	VCC	Power	1.8V-3.6V power 1.8~3.6电源
2	SI	Digital Input	Serial configuration interface, data input 串行配置接口，数据输入
3	SCLK	Digital Input	Serial configuration interface, clock input 串行配置接口，时钟输入
4	SO	Digital Output	Serial configuration interface, data output. 串行配置接口，数据输出 Optional general output pin when CSn is high CSn高电平时，可选通用输出
5	GDO2	Digital Output	Digital output pin for general use: 通用数字信号输出： Test signals 测试信号 FIFO status signals 先进先出堆栈状态信号 Clear Channel Indicator 空闲信道指示 Clock output, down-divided from XOSC 时钟输出，从XOSC分频

			Serial output RX data 串行输出接收数据
6	GND	Ground	GND 地
7	GDOo	Digital 0/I	Digital output pin for general use: 通用数字信号输出： Test signals 测试信号 FIFO status signals 先进先出堆栈状态信号 Clear Channel Indicator 空闲信道指示 Clock output, down-divided from XOSC 时钟输出，从XOSC分频 Serial output RX data 串行输出接收数据 Serial intput RX data 串行输入接收数据
8	CSn	Digital Input	Serial configuration interface, chip select 串行配置接口，芯片选择
9	PA_EN	Digital Input	When TX status set ”1”, RX set”0” Tx发射状态时设置为“1”RX接收设置为“0”
10	LNA_EN	Digital Input	When RX status set ”1”, TX set”0” Rx接收状态时设置为“1”TX发射设置为“0”

Absolute Maximum Ratings 极限参数

Parameter（参数）	Rating（额定值）	Units（单位）
Supply Voltage（工作电压）	2-3.6	V DC
Operating Temperature（工作温度）	-40 to +85	℃

▪Package Description 外型说明



Name 名称	Dimension 尺寸	Name 名称	Dimension 尺寸

A	25.5mm+-0.2mm	**D**	2.0mm
B	34mm+-0.2mm	**E**	3.6mm
C	1mm	**F**	3.6mm+-0.2mm

6. Electrical Specifications 电气特性

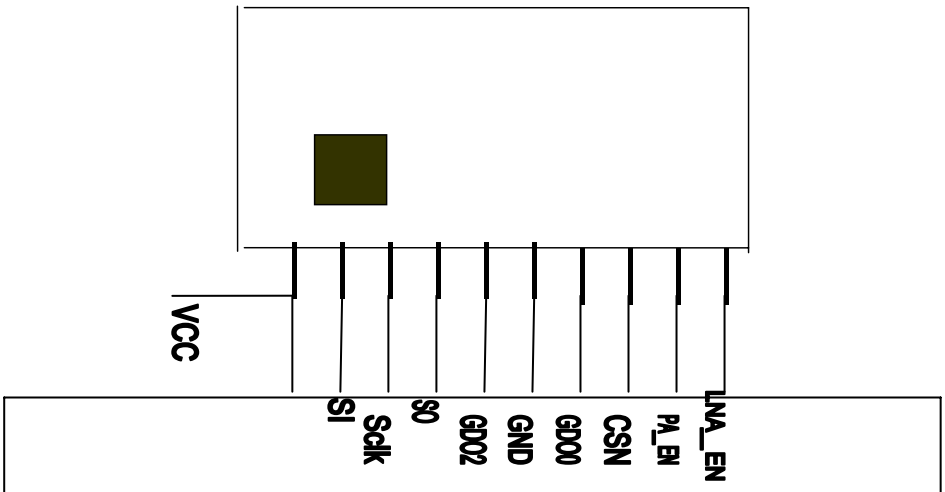
Tc = 25° C, VDD = 3.0V

Parameter	Min	Typ	Max	Unit	Condition
Current consumption, 消耗电流		150		mA	Transmit mode, +17dBm output power

General Characteristics 一般特性

Parameter	Min	Typ	Max	Unit	Condition/Note
Frequency range 频率范围	2400		2483	MHz	
Data rate	1.2		500	kbps	FSK
	1.2		500	kbps	GFSK and OOK
	2.6		500	kbps	(Shaped) MSK (also known as differential offset QPSK)
					Optional Manchester encoding (halves the data rate).

Application Circuit 典型应用电路



6.1 RF receiver section　RF 接收部分

Tc = 25° C, VDD = 3.0V

Parameter	Min	Typ	Max	Unit	Condition/Note
Receiver sensitivity 接收灵敏度		–112		dBm	2-FSK, 2.4kbps, 38kHz deviation, , 1% packet error rate, 20 bytes packet length, 203 kHz digital channel filter bandwidth
		–105		dBm	10 kbps data rate, FSK, 1% packet error rate, 20 bytes packet length, 232 kHz digital channel filter bandwidth
		-95		dBm	250kbps, MSK, 1% packet error rate, 20 bytes packet length, 540 kHz digital channel filter bandwidth
		-89		dBm	500Kbps, MSK, 1% packet error rate, 20 bytes packet length, 812 kHz digital channel filter bandwidth
Saturation输入饱和度		–13		dBm	
Digital channel filter bandwidth数字通道滤波器带宽	58		650	kHz	User programmable. The bandwidth limits are proportional to crystal frequency (given values assume a 26.0MHz crystal).

6.2 RF Transmit Section　RF 发射部分

Tc = 25° C, VDD = 3.0V

Parameter	Min	Typ	Max	Unit	Condition/Note
Differential load impedance差分负载阻抗		80 + j74		Ω	Differential impedance as seen from the RF-port (RF_P and RF_N) towards the antenna. Follow the CC2500EM reference design available from the TI and Chipcon websites.
Output power, highest setting最大输出功率		18.5	22	dBm	Output power is programmable, and full range is available in all frequency bands.

					Delivered to a 50Ωsingle-ended load via Chipcon reference RF matching network.

7. Measurement setup and testing procedures:

The interface for the localized CC2500+PA+LNA module cannot plug directly to SmartRF04EB board so there is an adaptor to convert it to standard EM interface as follows:

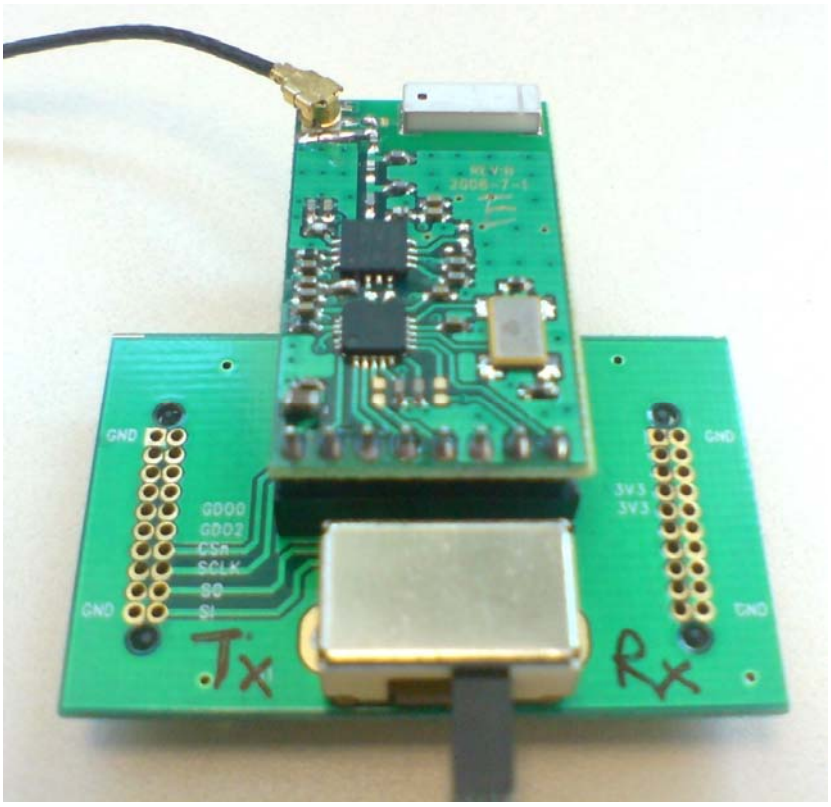


Figure 3.1 Connection for CC2500+PA+LNA module to SmartRF04EB.

Measurement setup:

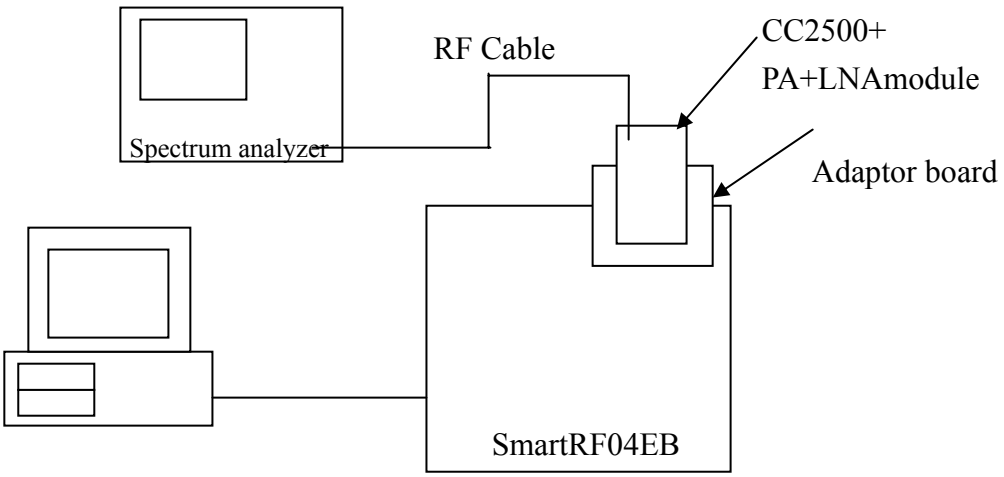
Module can then plugged into SmartRF04EB as below and further measurement.

Figure 3.2 Setup for CC2500+PA+LNA module on SmartRF04EB.

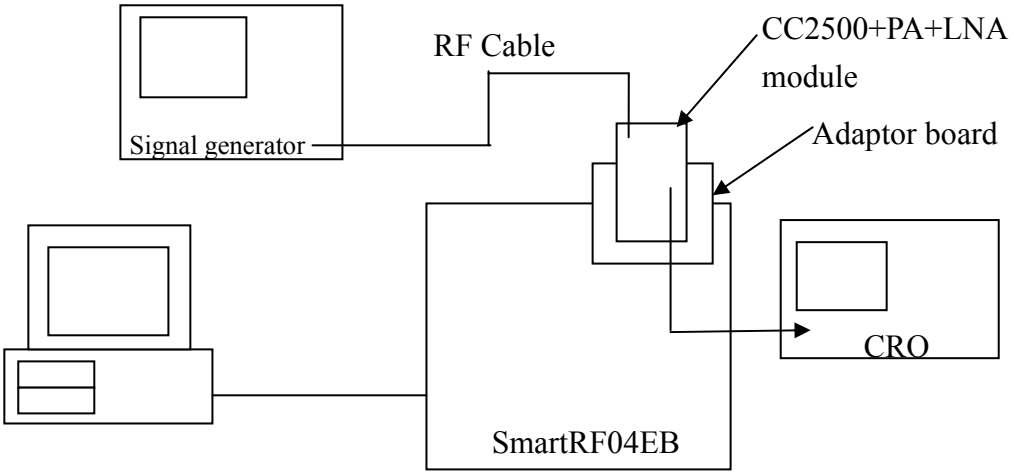
In addition, the module can be operated by SmartRF studio through SmartRF04EB. However, SmartRF studio software cannot control the Tx / Rx switch for PA+LNA; so it should be done it manual by switch the Tx / Rx on the adaptor board. Tx / Rx control is just simple switching the switch located at adaptor board (see Figure 2.1).

7.2 Parameters measurement:

For **transmitted power measurement**, it can connect the boards as follows and then set the SmartRF studio to Simple Tx with proper channels (say 2441MHz with 2.4kbps from preferred setting) and then read the Tx power, spectrum and spurious from spectrum analyzer.



7.3 For **sensitivity measurement**, it can connect those boards as follows:



Please set the signal generator to match the modulation setting at SmartRF studio and then set it to Simple Rx for reception.

Because the GDO pin of CC2500 does not layout to the SmartRF04EB, it should tie the signal from the following pin.

8. Program 模块编程

8.1. Configuration Software 配置软件

CC2500PA can be configured using the **SmartRF®** Studio software, available for download from http://www.chipcon.com. The SmartRF® Studio software is highly recommended for obtaining optimum register settings, and for evaluating performance and functionality.

可以利用**SmartRF®** Studio 软件对**cc2500PA**进行配置参数，该软件可以从网站 http://www.ti.com.下载。SmartRF® Studio是被高度推荐用来获得最合适的寄存器配置，和用来评估模块性能和功能。

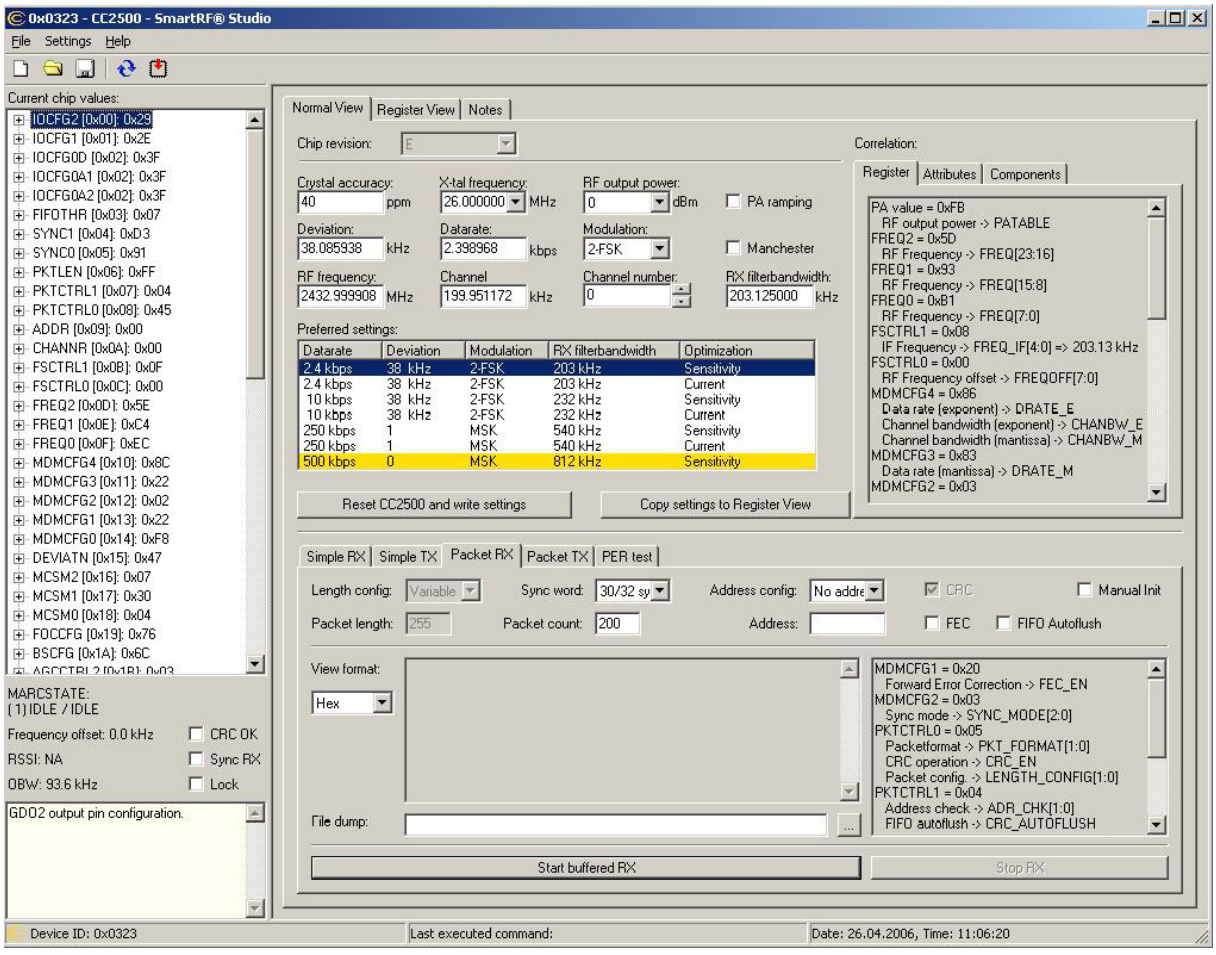


Figure 6: SmartRF® Studio user interface

8.2. 4-wire Serial Configuration and Data Interface

CC2500PA is configured via a simple 4-wire SPI compatible interface (SI, SO, SCLK and CSn) where **CC2500PA** is the slave. This interface is also used to read and write buffered data. All address and data transfer on the SPI interface is done most significant bit first.
CC2500PA是通过一个简单的4线SPI兼容接口（SI，SO，SCLK，CSn）来配置，这时CC2500PA工作于slave模式。该接口也用于读缓冲器的数据。所有的地址和数据在SPI口的传送都是从最高位开始的。

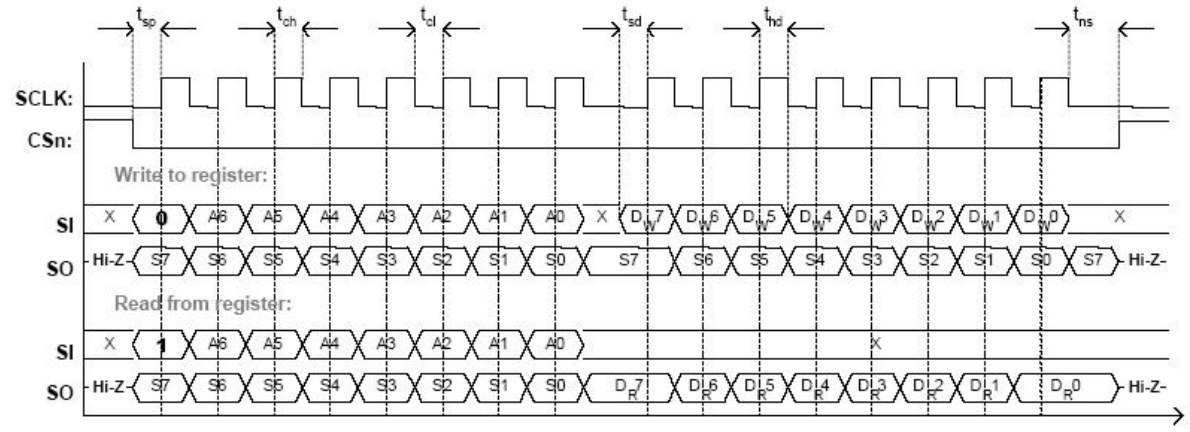


Figure 6: Configuration registers write and read operations

寄存器读写操作如下图：

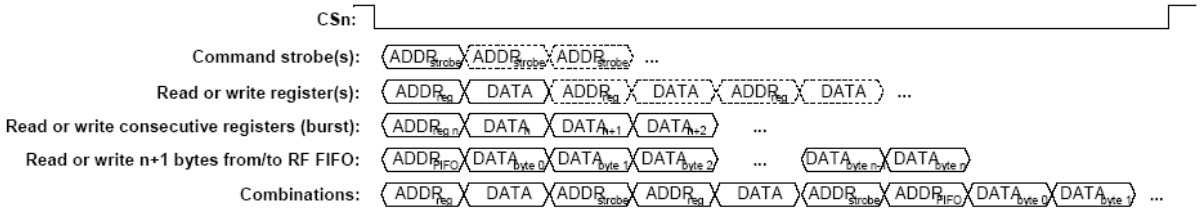


Figure 7: Register access types

8.3. 数据包格式：

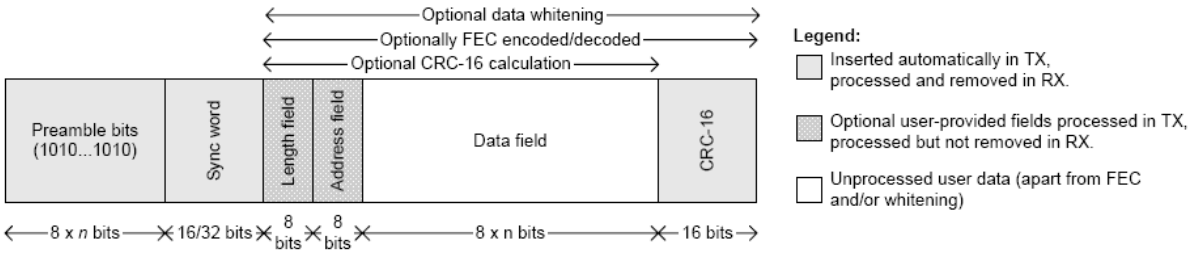


Figure 8: Packet Format

8.4. Power on start-up sequence

The power-up sequence is as follows (see Figure 11):

Set SCLK=1 and SI=0, to avoid potential problems with pin control mode .

Strobe CSn low / high.

Hold CSn high for at least 40µs.

Pull CSn low and wait for SO to go low (CHIP_RDYn).

Issue the SRES strobe.

When SO goes low again, reset is complete and the chip is in the IDLE state.

power-up 的操作顺序如下：

.设置 SCLK=1 和 SI=0，以消除 PIN 脚控制模式造成的可能发生的问题。

.设置 CSn 为低然后再拉高。

.保持 CSn 为高至少 40us。

.将 CSn 拉低等待 SO 变低（CHIP_RDYn）.

.发送 SRES 命令.

.当 SO 再次变低后,复位工作就完成了,IC 处于 IDLE 状态.

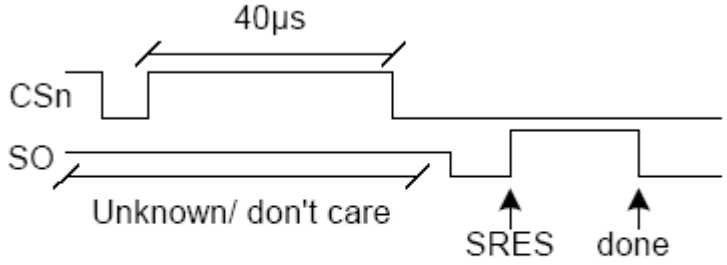


Figure 11: Power-up with SRES

8.5.WOR 模式

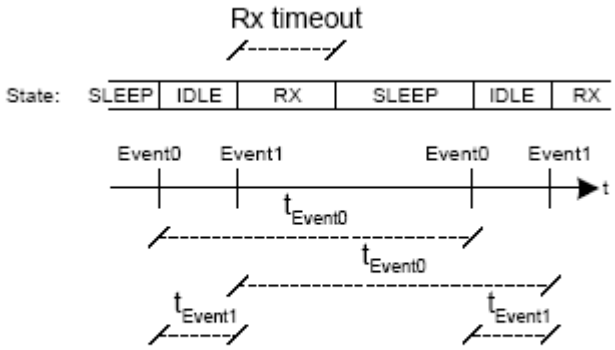


Figure 18: Event 0 and Event 1 relationship

8.6.TIMING

Description	XOSC periods	26 MHz crystal
IDLE to RX, no calibration	2298	88.4 µs
IDLE to RX, with calibration	~21037	809 µs
IDLE to TX/FSTXON, no calibration	2298	88.4 µs
IDLE to TX/FSTXON, with calibration	~21037	809 µs
TX to RX switch	560	21.5 µs
RX to TX switch	250	9.6 µs
RX or TX to IDLE, no calibration	2	0.1 µs
RX or TX to IDLE, with calibration	~18739	721 µs
Manual calibration	~18739	721 µs

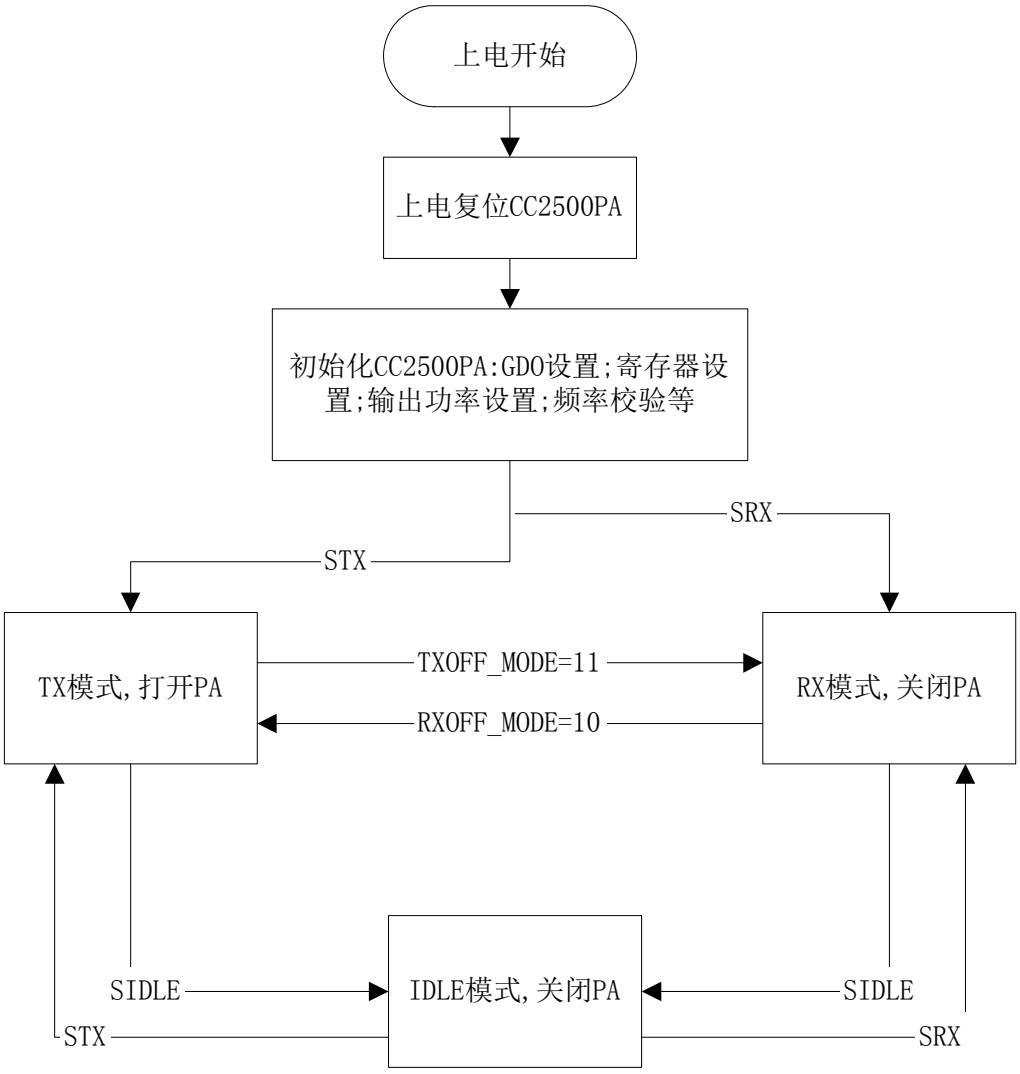
Table 28: State transition timing

9. OUTPUT POWER 输出功率表：

Output power [dBm]	Setting	Current consumption, typ. [mA]
(–55 or less)	0x00	8.9
–30	0x44	10.1
–28	0x41	10.0
–26	0x4C	11.7
–24	0x53	11.1
–22	0x83	10.9
–20	0x46	10.5
–18	0x4A	11.7
–16	0x86	11.0
–14	0x66	12.9
–12	0xC6	11.5
–10	0x69	14.1
–8	0x99	13.6
–6	0x7F	15.4
–4	0xAA	16.7
–2	0xBF	18.5
0	0xFB	21.6
1	0xFF	21.9

Table 22: Optimum PATABLE settings for various output power levels (subject to changes)

10．FLOW CHART 参考流程图：



Mark:

1. About Detail Specifications , Pls see CC2500 Data sheet .