LINEAR TECHNOLOGY

LT1964

200mA, Low Noise, Low Dropout Negative Micropower Regulator in ThinSOT

FEATURES

- **Low Profile (1mm) ThinSOT™ Package**
- **Low Noise: $30\mu V_{RMS}$ (10Hz to 100kHz)**
- **Low Quiescent Current: $30\mu A$**
- **Low Dropout Voltage: 340mV**
- **Output Current: 200mA**
- Fixed Output Voltage: −5V
- Adjustable Output from −1.22V to −20V
- Positive or Negative Shutdown Logic
- $3\mu A$ Quiescent Current in Shutdown
- Stable with $1\mu F$ Output Capacitor
- Stable with Aluminum, Tantalum, or Ceramic Capacitors
- Thermal Limiting

APPLICATIONS

- Battery-Powered Instruments
- Low Noise Regulator for Noise-Sensitive Instrumentation
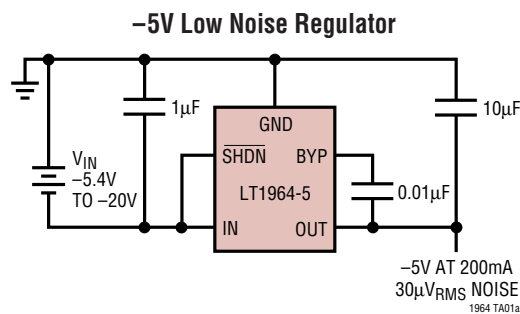- Negative Complement to LT1761 Family of Positive LDOs

DESCRIPTION

The LT®1964 is a micropower low noise, low dropout negative regulator. The device is capable of supplying 200mA of output current with a dropout voltage of 340mV. Low quiescent current ($30\mu A$ operating and $3\mu A$ shutdown) makes the LT1964 an excellent choice for battery-powered applications. Quiescent current is well controlled in dropout.

Other features of the LT1964 include low output noise. With the addition of an external $0.01\mu F$ bypass capacitor, output noise is reduced to $30\mu V_{RMS}$ over a 10Hz to 100kHz bandwidth. The LT1964 is capable of operating with small capacitors and is stable with output capacitors as low as $1\mu F$. Small ceramic capacitors can be used without the necessary addition of ESR as is common with other regulators. Internal protection circuitry includes reverse output protection, current limiting, and thermal limiting. The device is available with a fixed output voltage of −5V and as an adjustable device with a −1.22V reference voltage. The LT1964 regulators are available in a low profile (1mm) ThinSOT package.

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ThinSOT is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

−5V Low Noise Regulator

1964 TA01a

10Hz to 100kHz Output Noise

V_{OUT} 100μV/DIV

$30\mu V_{RMS}$

1ms/DIV

1964 TA01b
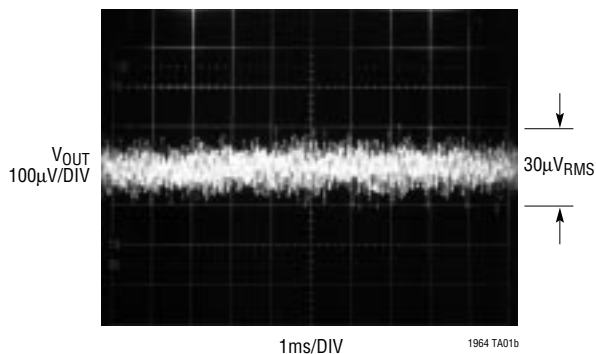
ABSOLUTE MAXIMUM RATINGS (Note 1)

IN Pin Voltage .... ±20V
OUT Pin Voltage (Note 11) .... ±20V
OUT to IN Differential Voltage (Note 11) .... −0.5V, 20V
ADJ Pin Voltage
    (with Respect to IN Pin) (Note 11) .... −0.5V, 20V
BYP Pin Voltage
    (with Respect to IN Pin) .... ±20V
$\overline{\text{SHDN}}$ Pin Voltage
    (with Respect to IN Pin) (Note 11) .... −0.5V, 35V

$\overline{\text{SHDN}}$ Pin Voltage
    (with Respect to GND Pin) .... −20V, 15V
Output Short-Circuit Duration .... Indefinite
Operating Junction Temperature
    Range (Note 10) .... − 40°C to 125°C
Storage Temperature Range .... − 65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

GND 1 | 5 OUT
IN 2 |
$\overline{\text{SHDN}}$ 3 | 4 ADJ

S5 PACKAGE
5-LEAD PLASTIC SOT-23

$T_{JMAX} = 150°C$, $\theta_{JA} \approx 125°C/W$ to $250°C/W$
(NOTE 13)
SEE THE APPLICATIONS INFORMATION SECTION

ORDER PART NUMBER
LT1964ES5-SD
S5 PART MARKING
LTVX

TOP VIEW

GND 1 | 5 OUT
IN 2 |
BYP 3 | 4 ADJ

S5 PACKAGE
5-LEAD PLASTIC SOT-23

$T_{JMAX} = 150°C$, $\theta_{JA} \approx 125°C/W$ to $250°C/W$
(NOTE 13)
SEE THE APPLICATIONS INFORMATION SECTION

ORDER PART NUMBER
LT1964ES5-BYP
S5 PART MARKING
LTVY

TOP VIEW

GND 1 | 5 OUT
IN 2 |
BYP 3 | 4 $\overline{\text{SHDN}}$

S5 PACKAGE
5-LEAD PLASTIC SOT-23

$T_{JMAX} = 150°C$, $\theta_{JA} \approx 125°C/W$ to $250°C/W$
(NOTE 13)
SEE THE APPLICATIONS INFORMATION SECTION

ORDER PART NUMBER
LT1964ES5-5
S5 PART MARKING
LTVZ

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Regulated Output Voltage (Notes 3, 9)	LT1964-5	$V_{IN} = −5.5V$, $I_{LOAD} = −1mA$		−4.925	−5	−5.075	V
		$−20V < V_{IN} < −6V$, $−200mA < I_{LOAD} < −1mA$	●	−4.850	−5	−5.150	V
ADJ Pin Voltage (Notes 2, 3, 9)	LT1964	$V_{IN} = −2V$, $I_{LOAD} = −1mA$		−1.202	−1.22	−1.238	V
		$−20V < V_{IN} < −2.8V$, $−200mA < I_{LOAD} < −1mA$	●	−1.184	−1.22	−1.256	V
Line Regulation	LT1964-5	$\Delta V_{IN} = −5.5V$ to $−20V$, $I_{LOAD} = −1mA$	●		15	50	mV
	LT1964 (Note 2)	$\Delta V_{IN} = −2.8V$ to $−20V$, $I_{LOAD} = −1mA$	●		1	12	mV
Load Regulation	LT1964-5	$V_{IN} = −6V$, $\Delta I_{LOAD} = −1mA$ to $−200mA$			15	35	mV
		$V_{IN} = −6V$, $\Delta I_{LOAD} = −1mA$ to $−200mA$	●			50	mV
	LT1964	$V_{IN} = −2.8V$, $\Delta I_{LOAD} = −1mA$ to $−200mA$			2	7	mV
		$V_{IN} = −2.8V$, $\Delta I_{LOAD} = −1mA$ to $−200mA$	●			15	mV

1964f

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Dropout Voltage $V_{IN} = V_{OUT(NOMINAL)}$ (Notes 4, 5)	$I_{LOAD} = -1mA$			0.1	0.15	V
	$I_{LOAD} = -1mA$	●			0.19	V
	$I_{LOAD} = -10mA$			0.15	0.20	V
	$I_{LOAD} = -10mA$	●			0.25	V
	$I_{LOAD} = -100mA$			0.26	0.33	V
	$I_{LOAD} = -100mA$	●			0.39	V
	$I_{LOAD} = -200mA$			0.34	0.42	V
	$I_{LOAD} = -200mA$	●			0.49	V
GND Pin Current $V_{IN} = V_{OUT(NOMINAL)}$ (Notes 4, 6)	$I_{LOAD} = 0mA$	●		30	70	µA
	$I_{LOAD} = -1mA$	●		85	180	µA
	$I_{LOAD} = -10mA$	●		300	600	µA
	$I_{LOAD} = -100mA$	●		1.3	3	mA
	$I_{LOAD} = -200mA$	●		2.5	6	mA
Output Voltage Noise	$C_{OUT} = 10µF$, $C_{BYP} = 0.01µF$, $I_{LOAD} = -200mA$, BW = 10Hz to 100kHz			30		$µV_{RMS}$
ADJ Pin Bias Current	(Notes 2, 7)			30	100	nA
Minimum Input Voltage (Note 12) $I_{LOAD} = -200mA$	LT1964-BYP	●		-1.9	-2.8	V
	LT1964-SD	●		-1.6	-2.2	V
Shutdown Threshold	V_{OUT} = Off to On (Positive)	●		1.6	2.1	V
	V_{OUT} = Off to On (Negative)	●		-1.9	-2.8	V
	V_{OUT} = On to Off (Positive)	●	0.25	0.8		V
	V_{OUT} = On to Off (Negative)	●	-0.25	-0.8		V
$\overline{SHDN}$ Pin Current (Note 8)	$V_{\overline{SHDN}} = 0V$		-1	±0.1	1	µA
	$V_{\overline{SHDN}} = 15V$			6	15	µA
	$V_{\overline{SHDN}} = -15V$			-3	-9	µA
Quiescent Current in Shutdown	$V_{IN} = -6V$, $V_{\overline{SHDN}} = 0V$	●		3	10	µA
Ripple Rejection	$V_{IN} - V_{OUT} = -1.5V(Avg)$, $V_{RIPPLE} = 0.5V_{P-P}$, $f_{RIPPLE} = 120Hz$, $I_{LOAD} = -200mA$		46	54		dB
Current Limit	$V_{IN} = -6V$, $V_{OUT} = 0V$			350		mA
	$V_{IN} = V_{OUT(NOMINAL)} -1.5V$, $\Delta V_{OUT} = 0.1V$	●	220			mA
Input Reverse Leakage Current	$V_{IN} = 20V$, V_{OUT}, V_{ADJ}, $V_{\overline{SHDN}}$ = Open Circuit	●			1	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LT1964 (adjustable version) is tested and specified for these conditions with the ADJ pin connected to the OUT pin.

Note 3: Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

Note 4: To satisfy requirements for minimum input voltage, the LT1964 (adjustable version) is tested and specified for these conditions with an external resistor divider (two 249k resistors) for an output voltage of −2.44V. The external resistor divider will add a 5µA DC load on the output.

Note 5: Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to: $(V_{IN} + V_{DROPOUT})$.

Note 6: GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)}$ and a current source load. This means the device is tested while operating in its dropout region. This is the worst-case GND pin current. The GND pin current will decrease slightly at higher input voltages.

Note 7: ADJ pin bias current flows out of the ADJ pin.

Note 8: Positive $\overline{SHDN}$ pin current flows into the $\overline{SHDN}$ pin. $\overline{SHDN}$ pin current is included in the GND pin current specification.

Note 9: For input-to-output differential voltages greater than 7V, a 50µA load is needed to maintain regulation.

Note 10: The LT1964E is guaranteed to meet performance specifications from 0°C to 125°C. Specifications over the −40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 11:** A parasitic diode exists internally on the LT1964 between the OUT, ADJ and $\overline{SHDN}$ pins and the IN pin. The OUT, ADJ and $\overline{SHDN}$ pins cannot be pulled more than 0.5V more negative than the IN pin during fault conditions, and must remain at a voltage more positive than the IN pin during operation.

Note 12: For the LT1964-BYP, this specification accounts for the operating threshold of the $\overline{SHDN}$ pin, which is tied to the IN pin internally. For the LT1964-SD, the $\overline{SHDN}$ threshold must be met to ensure device operation.

Note 13: Actual thermal resistance (θ_{JA}) junction to ambient will be a function of board layout. Junction-to-case thermal resistance (θ_{JC}) measured at Pin 2 is 60°C/W. See the Thermal Considerations section in the Applications Information.
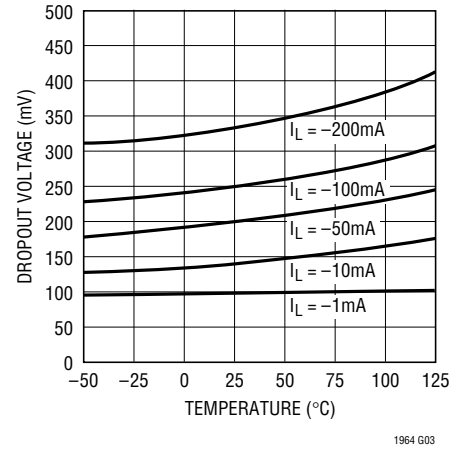
LT1964

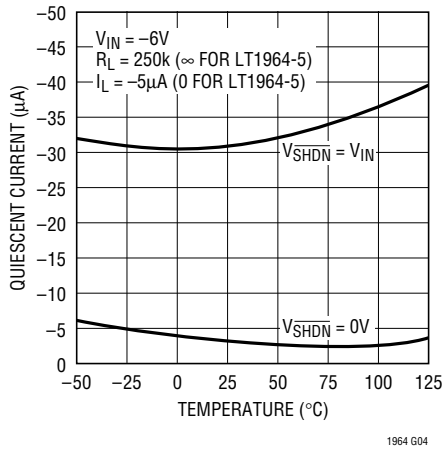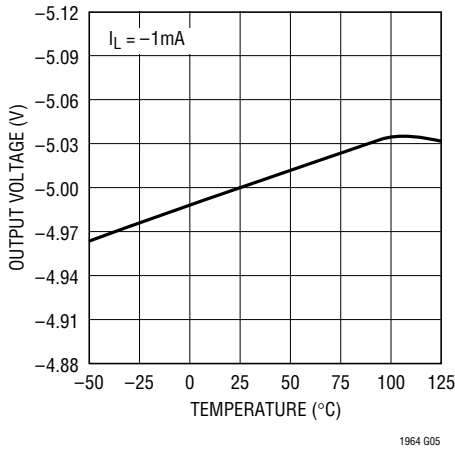# TYPICAL PERFORMANCE CHARACTERISTICS

Typical Dropout Voltage

1964 G01
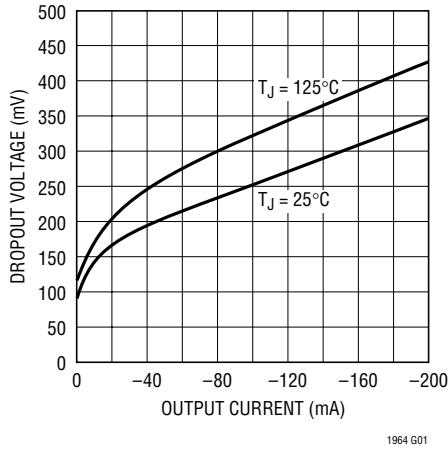
Guaranteed Dropout Voltage

1964 G02

Dropout Voltage

1964 G03

Quiescent Current

1964 G04
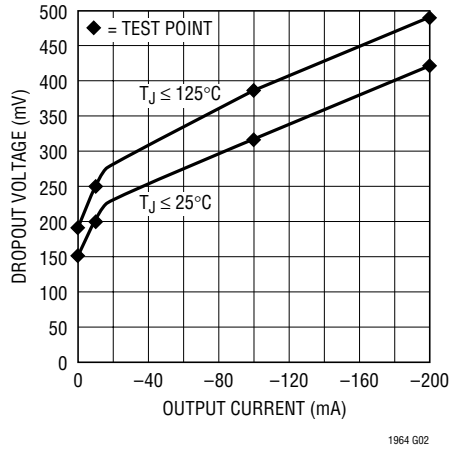
LT1964-5 Output Voltage

1964 G05

**LT1964-BYP, LT1964-SD
ADJ Pin Voltage**

1964 G06
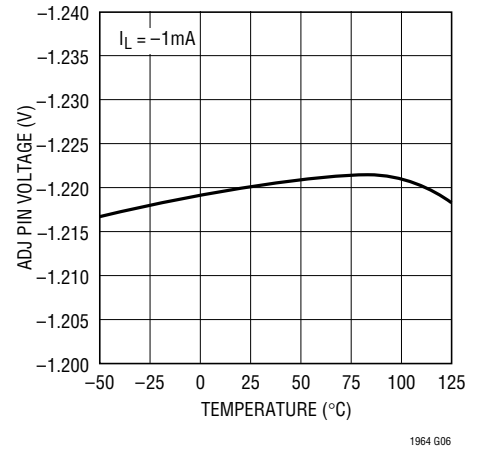
**LT1964-5
Quiescent Current**

1964 G07
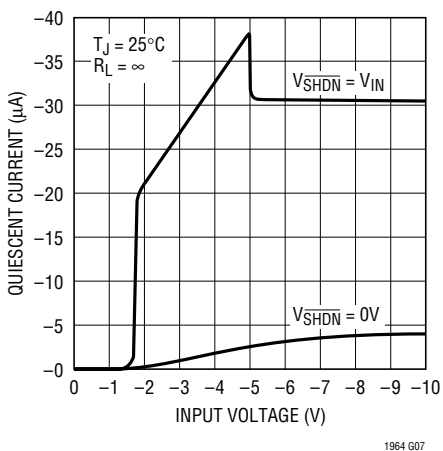
**LT1964-BYP, LT1964-SD
Quiescent Current**

1964 G08
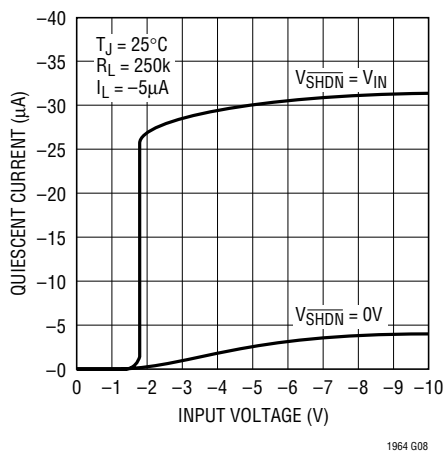
**LT1964-5
GND Pin Current**

1964 G09
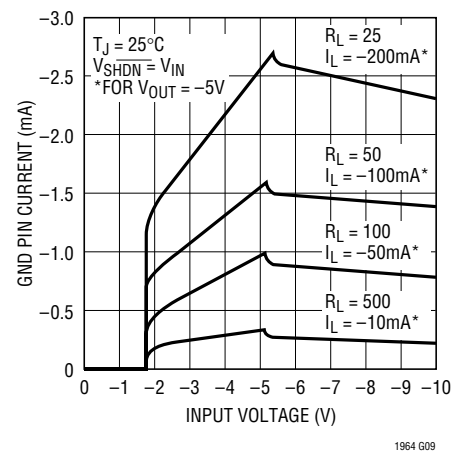
TYPICAL PERFORMANCE CHARACTERISTICS

LT1964-BYP, LT1964-SD
GND Pin Current
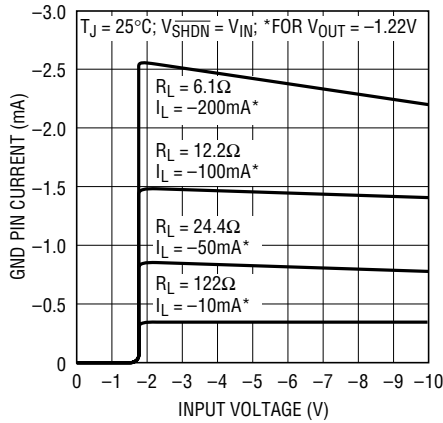
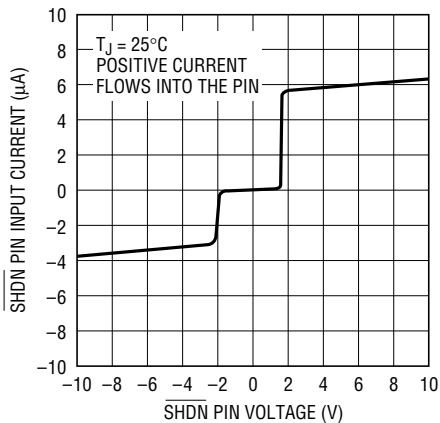1964 G10

GND Pin Current vs I_LOAD
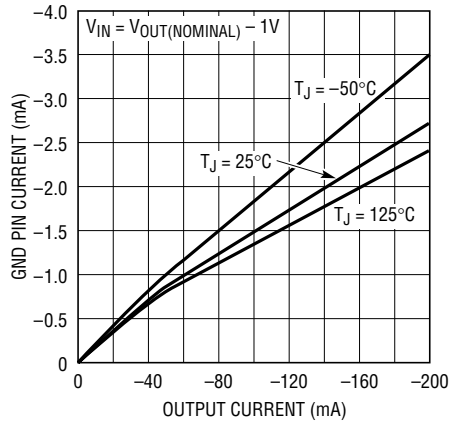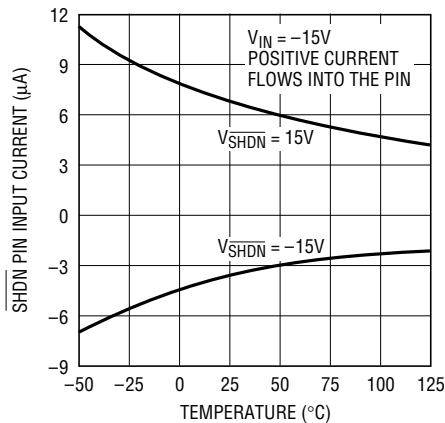

1964 G11

SHDN Pin Thresholds
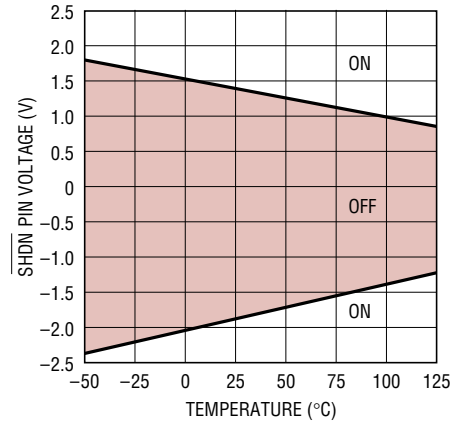
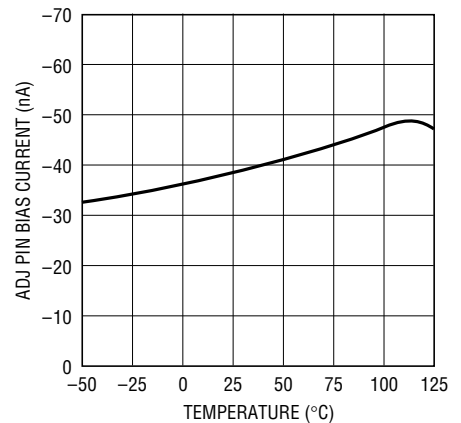1964 G12

SHDN Pin Input Current
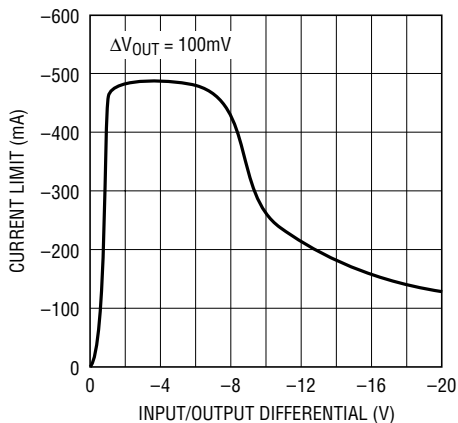

1964 G13

SHDN Pin Input Current
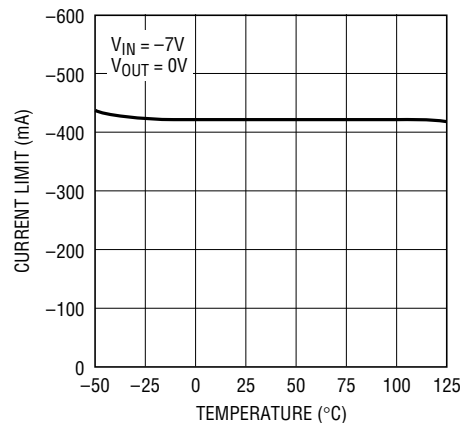

1964 G14

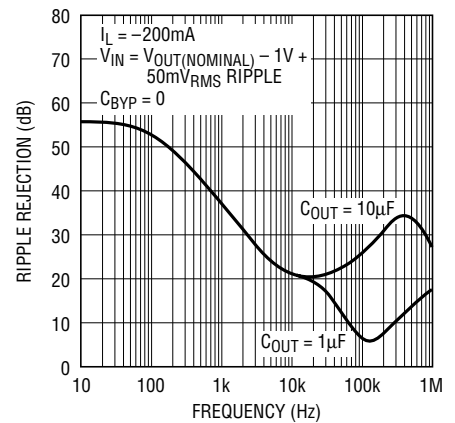**ADJ Pin Bias Current**

1964 G15

Current Limit

1964 G16

Current Limit

1964 G17

Input Ripple Rejection

1964 G18

TYPICAL PERFORMANCE CHARACTERISTICS
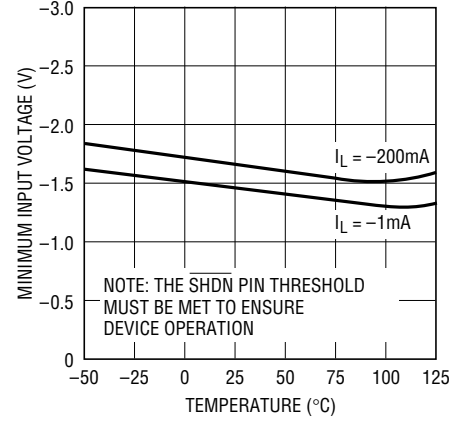
Input Ripple Rejection

$V_{IN} = V_{OUT(NOMINAL)} - 1V +$
$0.5V_{P-P}$ RIPPLE AT f = 120Hz
$I_L = -200mA$
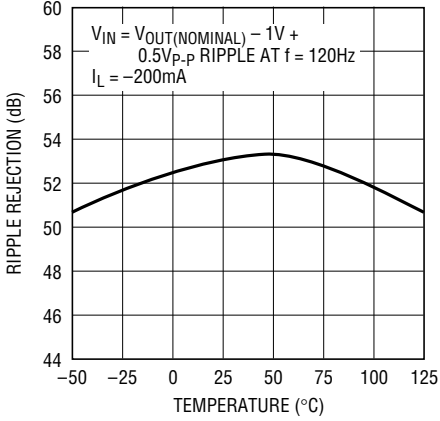
1964 G19

**LT1964-BYP
Minimum Input Voltage**

$I_L = -200mA$

$I_L = -1mA$

NOTE: THE MINIMUM INPUT VOLTAGE
ACCOUNTS FOR THE OPERATING
THRESHOLD OF THE SHDN PIN WHICH
IS TIED TO THE IN PIN INTERNALLY
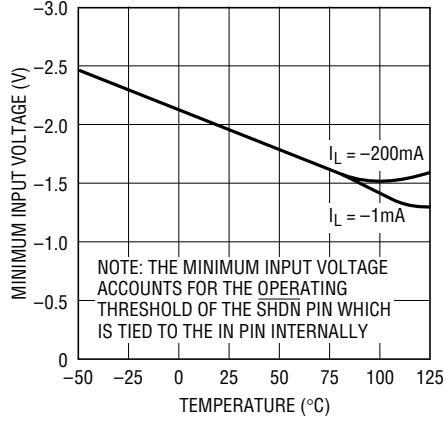
1964 G20

**LT1964-SD
Minimum Input Voltage**

$I_L = -200mA$

$I_L = -1mA$

NOTE: THE SHDN PIN THRESHOLD
MUST BE MET TO ENSURE
DEVICE OPERATION

1964 G21

Load Regulation

$I_L = -1mA$ TO $-200mA$

LT1964-5

LT1964-BYP, LT1964-SD
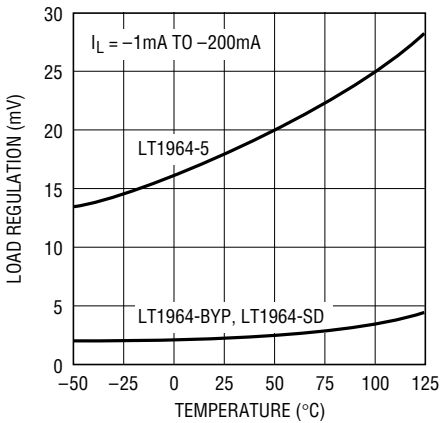
1964 G22

Output Noise Spectral Density

$C_{BYP} = 1000pF$ $C_{BYP} = 100pF$

$C_{BYP} = 0$

$C_{BYP} = 0.01\mu F$

$C_{OUT} = 10\mu F$
$I_L = 200mA$
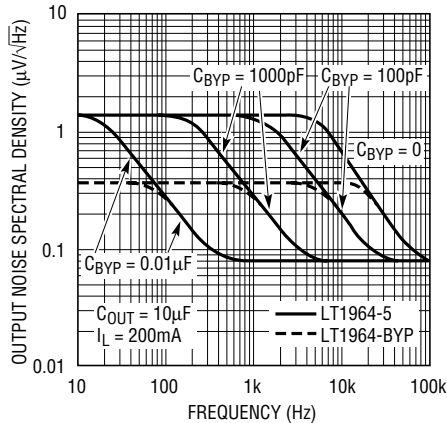
LT1964-5
LT1964-BYP

1964 G23

**RMS Output Noise vs Bypass
Capacitor**

$C_{OUT} = 10\mu F$
$I_L = -200mA$
f = 10Hz TO 100kHz

LT1964-5

LT1964-BYP
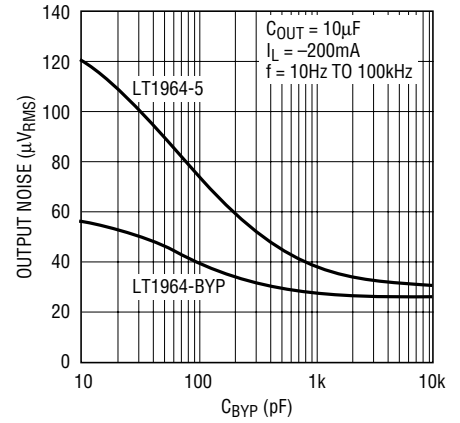
1964 G24

**RMS Output Noise vs Load
Current**

$C_{OUT} = 10\mu F$

LT1964-5

$C_{BYP} = 0$

LT1964-BYP,
LT1964-SD

LT1964-5

LT1964-BYP

$C_{BYP} = 0.01\mu F$
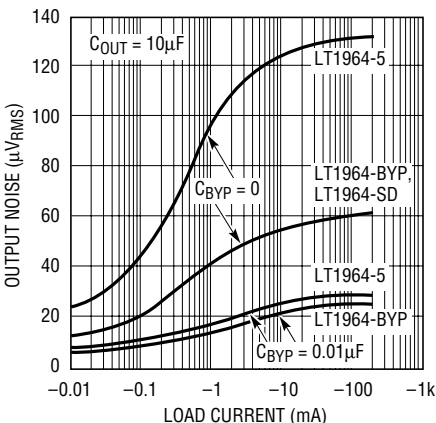
1964 G25

**LT1964-5, 10Hz to 100kHz Output
Noise, $C_{BYP} = 0$**

$C_{OUT} = 10\mu F$ 1ms/DIV
$I_{LOAD} = -200mA$
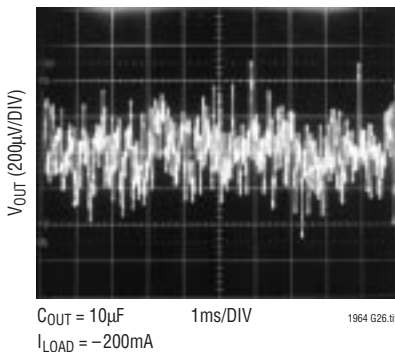
1964 G26.tif

**LT1964-5, 10Hz to 100kHz Output
Noise, $C_{BYP} = 100pF$**

$C_{OUT} = 10\mu F$ 1ms/DIV
$I_{LOAD} = -200mA$

1964 G27.tif

1964f

LINEAR
TECHNOLOGY
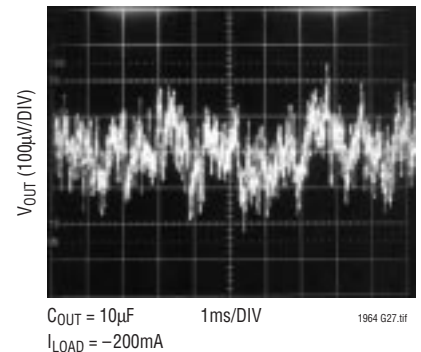
TYPICAL PERFORMANCE CHARACTERISTICS

LT1964-5, 10Hz to 100kHz Output Noise, C_{BYP} = 1000pF
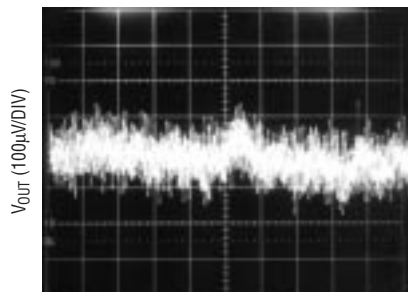
C_{OUT} = 10μF   1ms/DIV   1964 G28.tif
I_{LOAD} = –200mA

LT1964-5, 10Hz to 100kHz Output Noise, C_{BYP} = 0.01μF

C_{OUT} = 10μF   1ms/DIV   1964 G29.tif
I_{LOAD} = –200mA

LT1964-5, Transient Response, C_{BYP} = 0

1964 G30

LT1964-5, Transient Response, C_{BYP} = 0.01μF

1964 G31

PIN FUNCTIONS

GND (Pin 1): Ground.

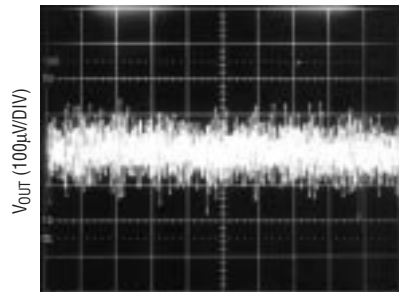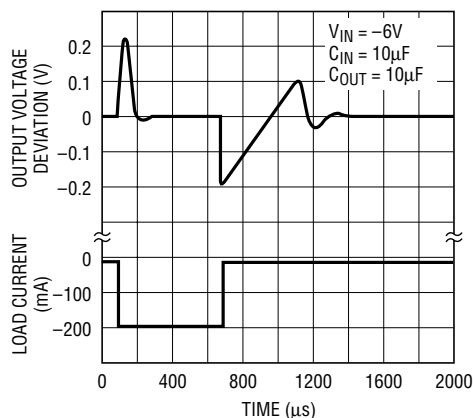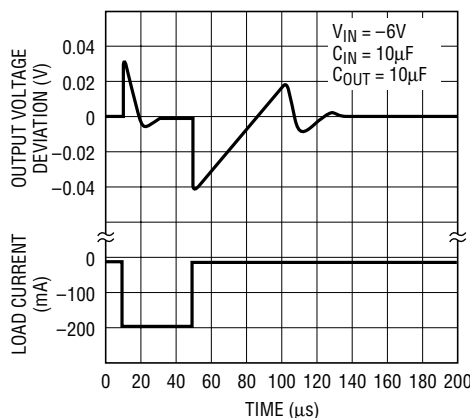**IN (Pin 2):** Power is Supplied to the Device Through the Input Pin. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of 1μF to 10μF is sufficient.

BYP (Pin 3, Fixed/–BYP devices): The BYP Pin is used to Bypass the Reference of the LT1964 to Achieve Low Noise Performance from the Regulator. A small capacitor from the output to this pin will bypass the reference to lower the output voltage noise. A maximum value of 0.01μF can be used for reducing output voltage noise to a typical $30μV_{RMS}$ over a 10Hz to 100kHz bandwidth. If not used, this pin must be left unconnected.

$\overline{SHDN}$ (Pin 3/4, –$\overline{SHDN}$/Fixed Devices): The $\overline{SHDN}$ Pin is used to put the LT1964 into a Low Power Shutdown State. The $\overline{SHDN}$ pin is referenced to the GND pin for regulator control, allowing the LT1964 to be driven by either positive or negative logic. The output of the LT1964 will be off when the $\overline{SHDN}$ pin is pulled within ±0.8V of GND. Pulling the $\overline{SHDN}$ pin more than –1.9V or +1.6V will turn the LT1964 on. The $\overline{SHDN}$ pin can be driven by 5V logic or open

PIN FUNCTIONS

collector logic with a pull-up resistor. The pull-up resistor is required to supply the pull-up current of the open collector gate, normally several microamperes, and the SHDN pin current, typically 3μA out of the pin (for negative logic) or 6μA into the pin (for positive logic). If unused, the SHDN pin must be connected to V_{IN}. The device will be shut down if the SHDN pin is open circuit. For the LT1964-BYP, the SHDN pin is internally connected to V_{IN}. A parasitic diode exists between the SHDN pin and the input of the LT1964. The SHDN pin cannot be pulled more negative than the input during normal operation, or more than 0.5V below the input during a fault condition.

ADJ (Pin 4, Adjustable Devices only): For the Adjustable LT1964, this is the Input to the Error Amplifier. The ADJ pin has a bias current of 30nA that flows out of the pin. The ADJ pin voltage is –1.22V referenced to ground, and the output voltage range is –1.22V to –20V. A parasitic diode exists between the ADJ pin and the input of the LT1964. The ADJ pin cannot be pulled more negative than the input during normal operation, or more than 0.5V more negative than the input during a fault condition.

OUT (Pin 5): The Output Supplies Power to the Load. A minimum output capacitor of 1μF is required to prevent oscillations. Larger output capacitors will be required for applications with large transient loads to limit peak voltage transients. A parasitic diode exists between the output and the input. The output cannot be pulled more negative than the input during normal operation, or more than 0.5V below the input during a fault condition. See the Applications Information section for more information on output capacitance and reverse output characteristics.

APPLICATIONS INFORMATION

The LT1964 is a 200mA negative low dropout regulator with micropower quiescent current and shutdown. The device is capable of supplying 200mA at a dropout voltage of 340mV. Output voltage noise can be lowered to 30μV$_{RMS}$ over a 10Hz to 100kHz bandwidth with the addition of a 0.01μF reference bypass capacitor. Additionally, the reference bypass capacitor will improve transient response of the regulator, lowering the settling time for transient load conditions. The low operating quiescent current (30μA) drops to 3μA in shutdown. In addition to the low quiescent current, the LT1964 incorporates several protection features which make it ideal for use in battery-powered systems. In dual supply applications where the regulator load is returned to a positive supply, the output can be pulled above ground by as much as 20V and still allow the device to start and operate.

Adjustable Operation

The adjustable version of the LT1964 has an output voltage range of –1.22V to –20V. The output voltage is set by the ratio of two external resistors as shown in Figure 1. The device servos the output to maintain the voltage at the ADJ pin at –1.22V referenced to ground. The current in R1 is then equal to –1.22V/R1 and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 30nA at 25°C, flows through R2 out of the ADJ pin. The output voltage can be calculated using the formula in Figure 1. The value of R1 should be less than 250kΩ to minimize errors in the output voltage caused by the ADJ pin bias current. Note that in shutdown the output is turned off and the divider current will be zero. Curves of ADJ Pin Voltage vs Temperature and ADJ Pin Bias Current vs Temperature appear in the Typical Performance Characteristics section.

The adjustable device is tested and specified with the ADJ pin tied to the OUT pin and a 5μA DC load (unless otherwise specified) for an output voltage of –1.22V. Specifications for output voltages greater than –1.22V will be proportional to the ratio of the desired output voltage to –1.22V; (V_{OUT}/–1.22V). For example, load regulation for an output current change of 1mA to 200mA is 2mV typical at V_{OUT} = –1.22V. At V_{OUT} = –12V, load regulation is:

$$(-12V/-1.22V) \bullet (2mV) = 19.6mV$$

APPLICATIONS INFORMATION
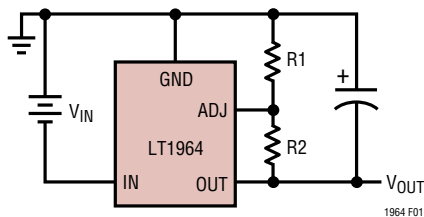
$$V_{OUT} = -1.22V(1 + \frac{R2}{R1}) - (I_{ADJ})(R2)$$

$$V_{ADJ} = -1.22V$$

$$I_{ADJ} = 30nA\ AT\ 25°C$$

OUTPUT RANGE = –1.22V TO –20V

Figure 1. Adjustable Operation

Bypass Capacitance and Low Noise Performance

The LT1964 may be used with the addition of a bypass capacitor from V_{OUT} to the BYP pin to lower output voltage noise. A good quality low leakage capacitor is recommended. This capacitor will bypass the reference of the LT1964, providing a low frequency noise pole. The noise pole provided by this bypass capacitor will lower the output voltage noise to as low as $30\mu V_{RMS}$ with the addition of a 0.01µF bypass capacitor. Using a bypass capacitor has the added benefit of improving transient response. With no bypass capacitor and a 10µF output capacitor, a –10mA to –200mA load step will settle to within 1% of its final value in less than 100µs. With the addition of a 0.01µF bypass capacitor, the output will stay within 1% for the same –10mA to –200mA load step (see LT1964-5 Transient Response in the Typical Characteristics section). However, regulator start-up time is inversely proportional to the size of the bypass capacitor.

Higher values of output voltage noise may be measured if care is not exercised with regard to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the output of the LT1964-X.

Output Capacitance and Transient Response

The LT1964 is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 1µF with an ESR of 3Ω or less is recommended to prevent oscillations. The LT1964 is a micropower device and output transient response will be a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT1964, will increase the effective output capacitor value.

Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R, and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients as shown in Figures 2 and 3. When used with a –5V regulator, a 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor the stress can be induced by vibrations in the system or thermal transients. The resulting voltages produced can cause appreciable amounts of noise, especially when a ceramic capacitor is used for noise bypassing. A ceramic capacitor produced Figure 4's trace in response to light tapping from a pencil. Similar vibration induced behavior can masquerade as increased output voltage noise.
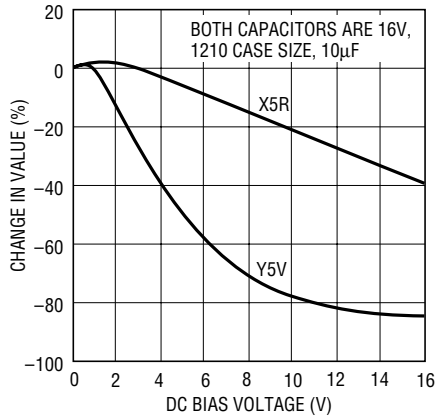
APPLICATIONS INFORMATION
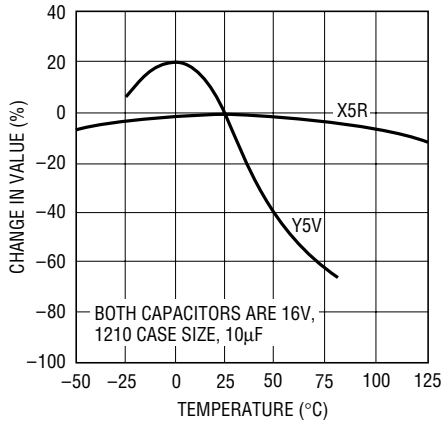

Figure 2. Ceramic Capacitor DC Bias Characteristics
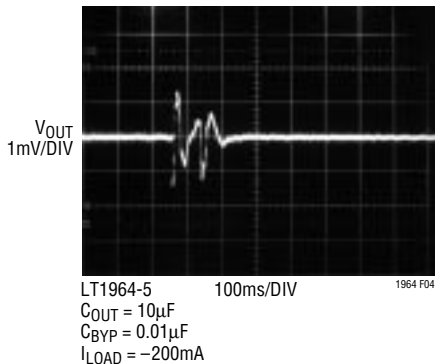

Figure 3. Ceramic Capacitor Temperature Characteristics

Figure 4. Noise Resulting from Tapping on a Ceramic Capacitor

Thermal Considerations

The power handling capability of the device will be limited by the maximum rated junction temperature (125°C). The power dissipated by the device will be made up of two components:

1. Output current multiplied by the input/output voltage differential: $I_{OUT} \cdot (V_{IN} - V_{OUT})$, and

2. Ground pin current multiplied by the input voltage: $I_{GND} \cdot V_{IN}$.

The GND pin current can be found by examining the GND Pin Current curves in the Typical Performance Characteristics. Power dissipation will be equal to the sum of the two components listed above.

The LT1964 series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

The following table lists thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on 3/32" FR-4 board with one ounce copper.

Table 1. Measured Thermal Resistance

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
TOPSIDE*	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	125°C/W
1000mm^2	2500mm^2	2500mm^2	125°C/W
225mm^2	2500mm^2	2500mm^2	130°C/W
100mm^2	2500mm^2	2500mm^2	135°C/W
50mm^2	2500mm^2	2500mm^2	150°C/W

*Device is mounted on topside.

The thermal resistance junction-to-case (θ_{JC}), measured at Pin 2, is 60°C/W.

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APPLICATIONS INFORMATION

Calculating Junction Temperature

Example: Given an output voltage of –5V, an input voltage range of –6V to –8V, an output current range of 0mA to –100mA, and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

The power dissipated by the device will be equal to:

$$I_{OUT(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) + (I_{GND} \bullet V_{IN(MAX)})$$

where,

$I_{OUT(MAX)} = -100mA$

$V_{IN(MAX)} = -8V$

I_{GND} at ($I_{OUT} = -100mA$, $V_{IN} = -8V$) = $-2mA$

so,

$$P = -100mA \bullet (-8V + 5V) + (-2mA \bullet -8V) = 0.32W$$

The thermal resistance (junction to ambient) will be in the range of 125°C/W to 150°C/W depending on the copper area. So the junction temperature rise above ambient will be approximately equal to:

$$0.32W \bullet 140°C/W = 44.2°C$$

The maximum junction temperature will then be equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$$T_{JMAX} = 50°C + 44.2°C = 94.2°C$$

Protection Features

The LT1964 incorporates several protection features which make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse input voltages and reverse output voltages.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The output of the LT1964 can be pulled above ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled above ground by 20V. For fixed voltage versions, the output will act like a large resistor, typically 500kΩ or higher, limiting current

flow to less than 40µA. For adjustable versions, the output will act like an open circuit, no current will flow into the pin. If the input is powered by a voltage source, the output will sink the short-circuit current of the device and will protect itself by thermal limiting. In this case, grounding the SHDN pin will turn off the device and stop the output from sinking the short-circuit current.
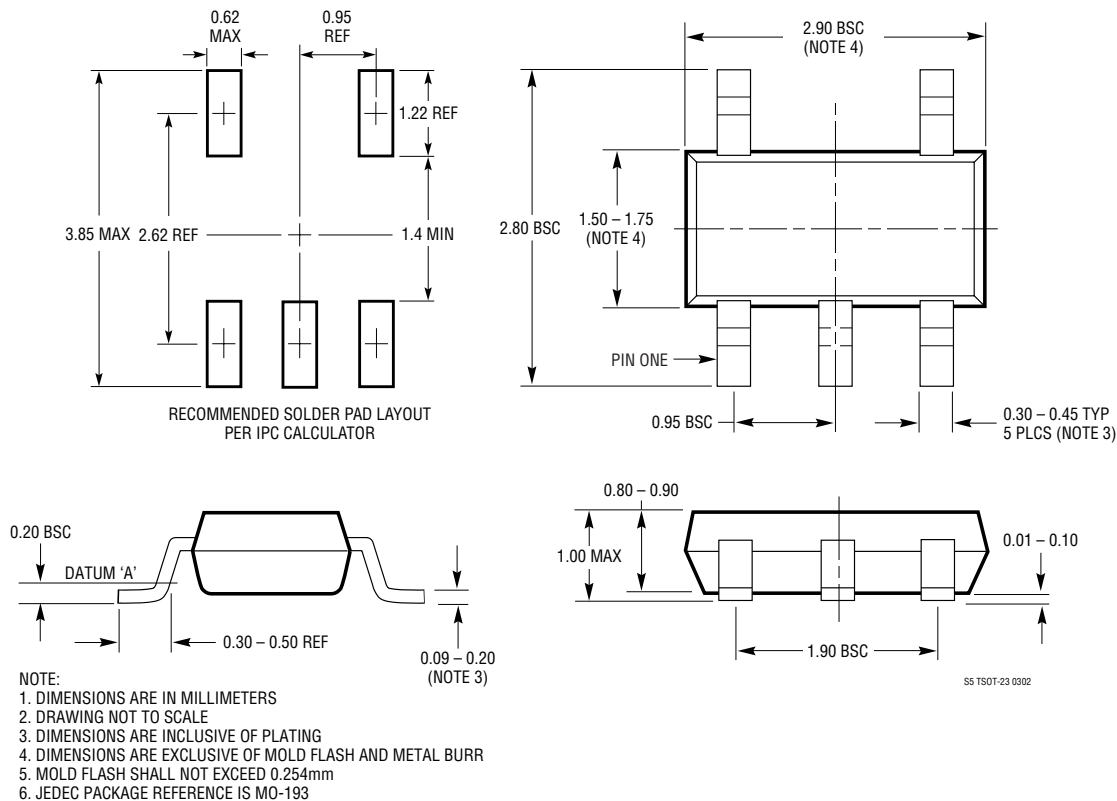
Like many IC power regulators, the LT1964 series have safe operating area protection. The safe area protection activates at input-to-output differential voltages greater than –7V. The safe area protection decreases the current limit as the input-to-output differential voltage increases and keeps the power transistor inside a safe operating region for all values of forward input to-output voltage. The protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown. A 50µA load is required at input-to-output differential voltages greater than –7V.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During start-up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein removal of an output short will not allow the output voltage to fully recover. Other regulators, such as the LT1175, also exhibit this phenomenon, so it is not unique to the LT1964 series.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations are immediately after the removal of a short-circuit or when the SHDN pin is pulled high after the input voltage has already been turned on. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable operating points for the regulator. With this double intersection, the input supply may need to be cycled down to zero and brought up again to make the output recover.

PACKAGE DESCRIPTION

S5 Package
5-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1635)

RECOMMENDED SOLDER PAD LAYOUT
PER IPC CALCULATOR

0.62 MAX
0.95 REF
1.22 REF
3.85 MAX
2.62 REF
1.4 MIN

2.90 BSC (NOTE 4)
2.80 BSC
1.50 – 1.75 (NOTE 4)
PIN ONE
0.95 BSC
0.30 – 0.45 TYP 5 PLCS (NOTE 3)

0.20 BSC
DATUM 'A'
0.30 – 0.50 REF
0.09 – 0.20 (NOTE 3)

0.80 – 0.90
1.00 MAX
0.01 – 0.10
1.90 BSC

S5 TSOT-23 0302

NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1120	125mA Micropower Low Dropout Regulator with Comparator and Shutdown	Includes 2.5V Reference and Comparator, V_{IN} = 3.5V to 36V, I_Q = 40μA, N8 Package
LT1121	150mA Micropower Low Dropout Regulator	V_{IN} = 4.2V to 30V, I_Q = 30μA; ThinSOT, S8 and MS8 Packages
LT1129	700mA Micropower Low Dropout Regulator	V_{IN} = 4.5V to 30V, I_Q = 50μA; DD and S8 Packages
LT1175	800mA Negative Low Dropout Micropower Regulator	V_{IN} = 4.5V to 20V, I_Q = 45μA, 0.26V Dropout Voltage, S8 and ThinSOT Packages
LT1611	Inverting 1.4MHz Switching Regulator	−5V at 150mA from 5V Input, ThinSOT Package
LT1761 Series	100mA, Low Noise, Low Dropout Micropower Regulators	V_{IN} = 1.5V to 20V, I_Q =20μA, 20μV_{RMS} Noise, ThinSOT Package
LT1762 Series	150mA, Low Noise, LDO Micropower Regulators	V_{IN} = 1.5V to 20V, I_Q =25μA, 20μV_{RMS} Noise, MS8 Package
LT1763 Series	500mA, Low Noise, LDO Micropower Regulators	V_{IN} = 1.5V to 20V, I_Q =30μA, 20μV_{RMS} Noise, S8 Package
LT1764A	3A, Low Noise, Fast Transient Response LDO	V_{IN} = 1.5V to 20V, 40μV_{RMS} Noise; DD and T5 Packages
LT1931/LT1931A	Inverting 1.2MHz/2.2MHz Switching Regulators	−5V at 350mA from 5V Input, ThinSOT Package
LT1962	300mA, Low Noise, LDO Micropower Regulator	V_{IN} = 1.5V to 20V, I_Q =30μA, 20μV_{RMS} Noise, MS8 Package
LT1963A	1.5A, Low Noise, Fast Transient Response LDO	V_{IN} = 1.5V to 20V, 40μV_{RMS} Noise; DD, T5, S8 and ThinSOT Packages

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