

Panasonic

AN32257A

**INTEGRATED WIRELESS POWER SUPPLY RECEIVER,
Qi (WIRELESS POWER CONSORTIUM) COMPLIANT**

FEATURES

- Integrated Wireless Power Receiver Solution
- Synchronous Full Bridge Rectifier control
- Input Voltage Range : VCC: 5 V ~ 19 V
- Over Temperature, Voltage, Current protection
- Under voltage lockout function
- Thermal Shut Down
- LED Indicator
- I²C Interface
- Package WLCSP

DESCRIPTION

AN32257A is a Wireless Power System Controller IC which is designed for Qi compliance defined by Version 1.1 of the System Description Wireless Power Transfer, Volume 1 for Low Power from Wireless Power Consortium. AN32257A is a controller IC to be used as the power receiver on a wireless power mobile device. A Qi compliance wireless power mobile device with AN32257A built-in could work with any wireless power base station which is Qi compliance.

APPLICATIONS

- WPC Compliant Receivers
- Cell Phones, Smart Phones
- Headsets
- Digital Cameras
- Tablets
- Portable Media Players etc.

The product specifications described in this book are subject to change without notice for the product which is currently under development. At the final stage of your design, purchasing, or use of the product, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Notes
Supply voltage	V_{RECT}	20	V	*1
	V_{EXT}	6.9	V	*1
	V_{VIO}	6	V	*1
Output Current	I_{RECT}	—	A	*1
Operating free-air temperature	T_{opr}	– 30 to + 85	°C	*2
Storage temperature	T_{stg}	– 50 to + 125	°C	*2
ESD	HBM (Human Body Model)	TBD	kV	—

Notes) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guarantee able as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for $T_a = 25\text{ °C}$.

POWER DISSIPATION RATING

PACKAGE	θ_{JA}	PD ($T_a = 25\text{ °C}$)	PD ($T_a = 85\text{ °C}$)	Notes
WLCSP Typ	TBD °C / W	TBD W	TBD W	*1

Note). For the actual usage, please refer to the PD- T_a characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

**CAUTION**

Although this has limited built-in ESD protection circuit, but permanent damage may occur on it. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Min.	Typ.	Max.	Unit	Notes
Supply voltage range	V_{RECT}	4.4	8	19	V	*1
	V_{EXT}	4.4	5	6		
	V_{VIO}	3.2(TBD)	3.3	5.5		

Note) Do not apply external currents and voltages to any pin not specifically mentioned.

Voltage values, unless otherwise specified, are with respect to GND.

*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

ELECTRICAL CHARACTERISTICS

C_{out} = 4.7 μF, V_{RECT} = 8 V, T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current Consumption							
Quiescent current	I _{STBY}			TBD		mA	—
UVLO							
Undervoltage lock-out	V _{UVLO}	V _{RECT} : 0V -> 5V	3.99	4.2	4.41	V	
Hysteresis on UVLO	V _{UVLOHY}	V _{RECT} : 5V -> 3V	—	0.4	—	V	
OVP							
Input overvoltage threshold	V _{OVP}	V _{RECT} : 5V -> 19V	17	18	19	V	
Hysteresis on OVP	V _{OVP0HY}	V _{RECT} : 19V -> 5V	—	3	—	V	
V_{RECT} (5W, LDO 5V mode)							
V _{RECT} Threshold1	V _{RECTTH1}	I _{LOAD} <125mA(TBD)		8		V	
V _{RECT} Threshold2	V _{RECTTH2}	125mA<I _{LOAD} <420mA (TBD)		5.4		V	
V _{RECT} Threshold3	V _{RECTTH3}	420mA<I _{LOAD} (TBD)		5.1		V	
V_{RECT} (5W, LDO 7V mode)							
V _{RECT} Threshold4	V _{RECTTH4}			TBD		V	
V _{RECT} Threshold5	V _{RECTTH5}			TBD		V	
V _{RECT} Threshold6	V _{RECTTH6}			TBD		V	
OUTPUT							
V _{OUT} (5W, LDO 5V mode)	V _{OUT1}	V _{RECT} =8V , I _{LOAD} =10mA	4.85	5	5.15	V	
	V _{OUT2}	V _{RECT} =5.1V , I _{LOAD} =1000mA	4.76	—	—	V	
V _{OUT} (5W, LDO 6V mode)	V _{OUT3}	V _{RECT} =9V , I _{LOAD} =10mA C _{OUT} = 10μF		6		V	
V _{OUT} (5W, LDO 7V mode)	V _{OUT4}	V _{RECT} =10V , I _{LOAD} =10mA C _{OUT} = 10μF		7		V	

ELECTRICAL CHARACTERISTICS (Continue)C_{out} = 4.7 μF, V_{RECT} = 8 V, T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Temperature Detector [Thermistor : ERTJ0EV104F]							
Over-temperature Detection Voltage	V _{TH}	60 °C detection VT _{HR} : TBD kohm (±1%)		TBD		V	—
Over-current protection							
Over-current threshold voltage	V _{OC_P}	Difference Voltage between V _{RECT} and I _{SENSE}		TBD		V	—
Thermal protection							
Thermal shutdown temperature	T _j	—	—	TBD	—		—
Thermal shutdown hysteresis	T _{j_{hys}}	—	—	TBD	—		—
Ext detector							
V _{EXT} Rising threshold voltage	V _{EXT_{TH}}	—	3.99	4.2	4.41		—
V _{EXT} hysteresis	V _{EXT_{HY}}	—	—	0.4	—		—
Termination (FULLCH)							
High input threshold (Termination)	V _{I_{H1}}	—	2.0	—	—	V	—
Low input threshold	V _{I_{L1}}	—	-0.2	—	0.2	V	—
Termination (SELVER)							
High input threshold (Termination)	V _{I_{H1}}	—	2.0	—	—	V	—
Low input threshold	V _{I_{L1}}	—	-0.2	—	0.2	V	—
Termination (SELHP)							
High input threshold (Termination)	V _{I_{H1}}	—	2.0	—	—	V	—
Low input threshold	V _{I_{L1}}	—	-0.2	—	0.2	V	—
Termination (SELOS_R)							
High input threshold (Termination)	V _{I_{H1}}	—	2.0	—	—	V	—
Low input threshold	V _{I_{L1}}	—	-0.2	—	0.2	V	—
Termination (NFC)							
High input threshold (Termination)	V _{I_{H1}}	—	2.0	—	—	V	—
Low input threshold	V _{I_{L1}}	—	-0.2	—	0.2	V	—
Termination (SELHV)							
High input threshold (Termination)	V _{I_{H1}}	—	2.9	—	—	V	—
Low input threshold	V _{I_{L1}}	—	-0.2	—	0.5	V	—

ELECTRICAL CHARACTERISTICS (Continue)C_{out} = 4.7 μF, V_{RECT} = 8 V, T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Termination (EXTCLK)							
High input threshold (Termination)	V _{IH1}	V _{IO} = 3.3V	V _{IO} × 0.7	—	—	V	—
Low input threshold	V _{IL1}	V _{IO} = 3.3V	-0.2	—	V _{IO} × 0.3	V	—
Termination (OUTH P)							
Output High level	V _{OH}	V _{IO} = 3.3V I _{OUTH P} = -2mA	V _{IO} × 0.8	—	—	V	—
Output Low level	V _{OL}	V _{IO} = 3.3V I _{OUTH P} = +2mA	-0.2	—	V _{IO} × 0.2	V	—
Termination (ENI2C)							
Output High level	V _{OH}	V _{IO} = 3.3V I _{ENI2C} = -2mA	V _{IO} × 0.8	—	—	V	—
Output Low level	V _{OL}	V _{IO} = 3.3V I _{ENI2C} = +2mA	-0.2	—	V _{IO} × 0.2	V	—
LEDCNT							
LET Sat	LED _{SAT}	I _{LED} = 20mA	—	—	0.5	V	—
LED Leak	LED _{LEAK}	LED = 7.5V	—	—	10	uA	—

ELECTRICAL CHARACTERISTICS (Continue)

C_{out} = 4.7 μF, V_{RECT} = 8 V, T_a = 25 °C ± 2 °C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C bus (Internal I/O stage characteristics)							
Low-level input voltage	V _{IL1}	Voltage which is recognized as SDA and SCL Low Level	-0.5	—	0.3 × V _{IO}	V	*1
High-level input voltage	V _{IH1}	Voltage which is recognized as SDA and SCL High Level	0.7 × V _{IO}	—	V _{IOmax} + 0.5	V	*1
SDA Low-level output voltage 1	V _{OL1}	V _{IO} > 3 V SDA(sink current) = 3 mA	0	—	0.4	V	—
SDA Low-level output voltage 2	V _{OL2}	V _{IO} < 3 V SDA(sink current) = 3 mA	0	—	0.2 × V _{IO}	V	—
Input current each I/O pin	I _L	SCL, SDA = 0.1 × V _{IO} to 0.9 × V _{IO}	-10	—	10	mA	—
SCL clock frequency	F _{OSC}	—	0	—	400	kHz	—

Note) *1 : The input threshold voltage of I²C bus (V_{th}) is linked to V_{IO} (I²C bus I/O stage supply voltage).

In case the pull-up voltage is not V_{IO}, the threshold voltage (V_{th}) is fixed to ((V_{IO} / 2) ± (Schmitt width) / 2) and High-level, Low-level of input voltage are not specified.

In this case, pay attention to Low-level (max.) value (V_{ILmax}).

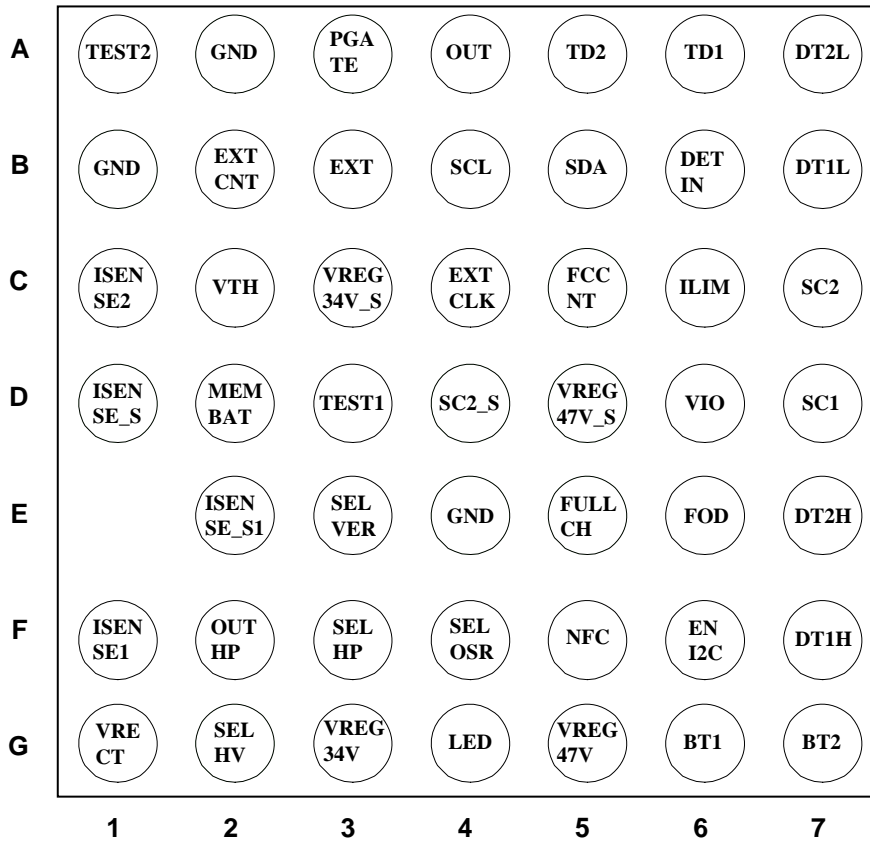
It is recommended that the pull-up voltage of I²C bus is set to the I²C bus I/O stage supply voltage (V_{IO}).

Slave address

A7	A6	A5	A4	A3	A2	A1
0	0	1	0	0	1	0

Pin Layout

Top View



Note). Refer to a "Detail Description" and the "Application Information" for detailed information.

Pin Function

Pin No.	Pin name	Type	Description
A1	TEST2	I	TEST Pin
A2,B1, E4	GND	GND	GND Pin
A3	PGATE	O	LDO Control Switch Pin
A4	OUT	I	LDO Feed back Pin
A5	TD2	O	Driving Load Capacity for Transmit Pin
A6	TD1	O	Driving Load Capacity for Transmit Pin
A7	DT2L	O	Rectification Low side Switch Gate Control Pin
B2	EXTCNT	O	External Switch control Pin
B3	EXT	Power Supply	External Input Pin for Detection
B4	SCL	I	I2C clock input Pin
B5	SDA	I/O	I2C data input/output Pin
B6	DETIN	I	Wave shaping Pin
B7	DT1L	O	Rectification Low side Switch Gate Control Pin
C1	ISENSE2	I	Current Sense Pin2
C2	VTH	I	Thermistor Connection Pin for abnormal temperature detection
C3	VREG34V _S	O	Internal Regulator Output Pin
C4	EXTCLK	I	External CLK Input Pin
C5	FCCNT	I	Full-Charge Control Pin
C6	ILIM	I	Programming Pin for the over current limit.
C7	SC2	I	Rectification Detection Pin
D1	ISENSE1_S	I	Current Sense Pin1
D2	MEMBAT	O	Random Number Memory Time Adjustment Pin
D3	TEST1	O	TEST Pin
D4	SC2_S	I	Rectification Detection Pin
D5	VREG47V _S	O	Internal Regulator Output Pin
D6	VIO	Power Supply	I2C Interface Power Supply Pin
D7	SC1	I	Rectification Detection Pin

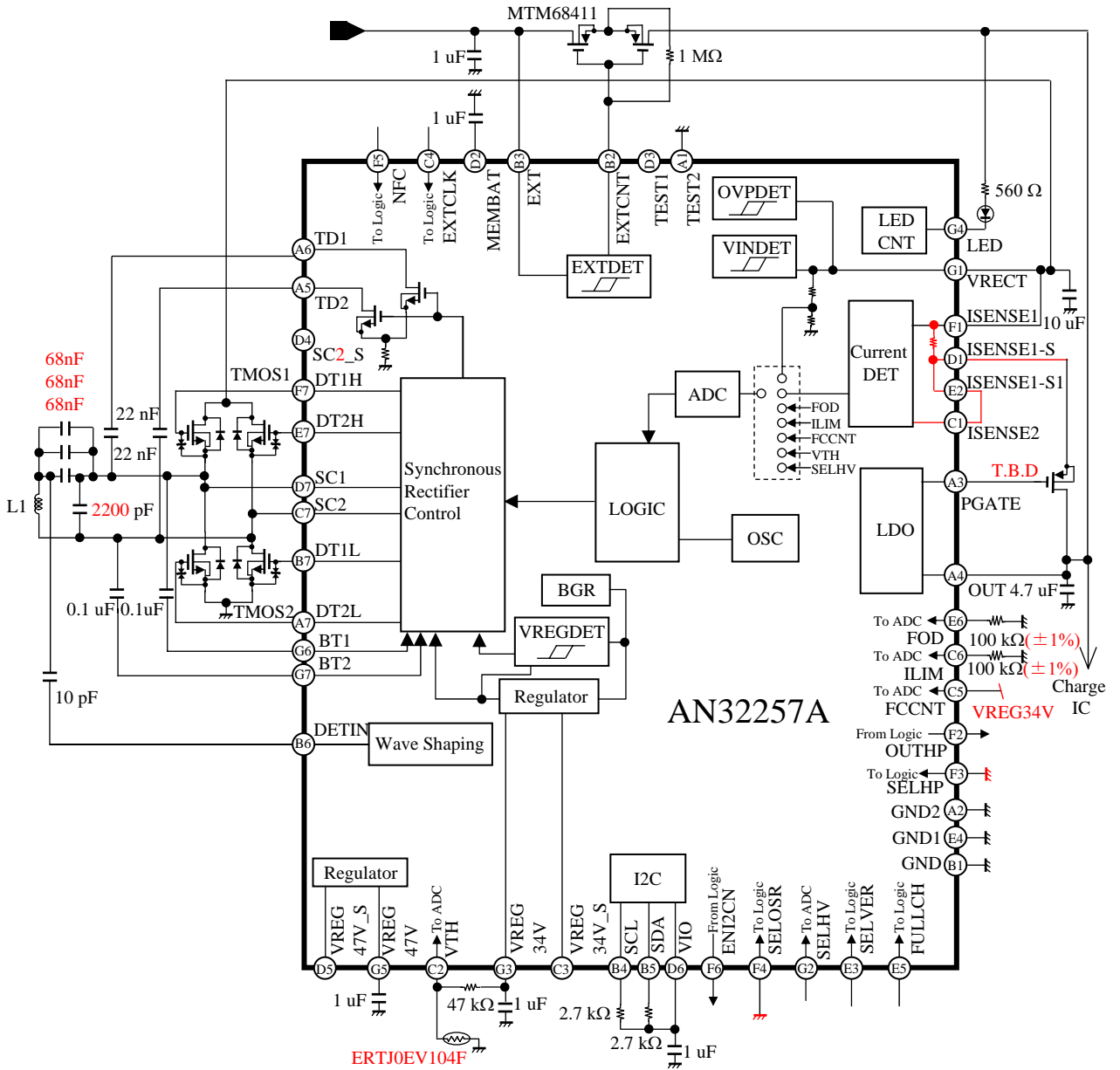
Note). Refer to a "Detail Description" and the "Application Information" for detailed information.

Pin Function

Pin No.	Pin name	Type	Description
E2	ISENSE1_S1	I	Current Sense Pin
E3	SELVER	I	Select WPC Version
E5	FULLCH	I	Full-Charge Signal Pin
E6	FOD	O	FOD Correction Pin
E7	DT2H	O	Rectification High side Switch Gate Control Pin
F1	ISENSE1	I	Current Sense Pin
F2	OUTHV	O	Output Enable 10W mode Pin
F3	SELHP	I	Select Power 5W or 10W mode Pin
F4	SELOSR	I	Select Outside Sense Resistor
F5	NFC	I	NFC Pin
F6	ENI2C	O	Enable to read or write I2C Pin
F7	DT1H	O	Rectification High side Switch Gate Control Pin
G1	VRECT	Power Supply	Supply Voltage Pin (from Rectifier Circuit)
G2	SELHV	I	Select Output Voltage(5V,6V or 7V) Pin
G3	VREG34V	O	Internal Regulator Output Pin
G4	LED	O	LED Driver Pin
G5	VREG47V	O	Internal Regulator Output Pin
G6	BT1	O	Boot Strap Pin
G7	BT2	O	Boot Strap Pin

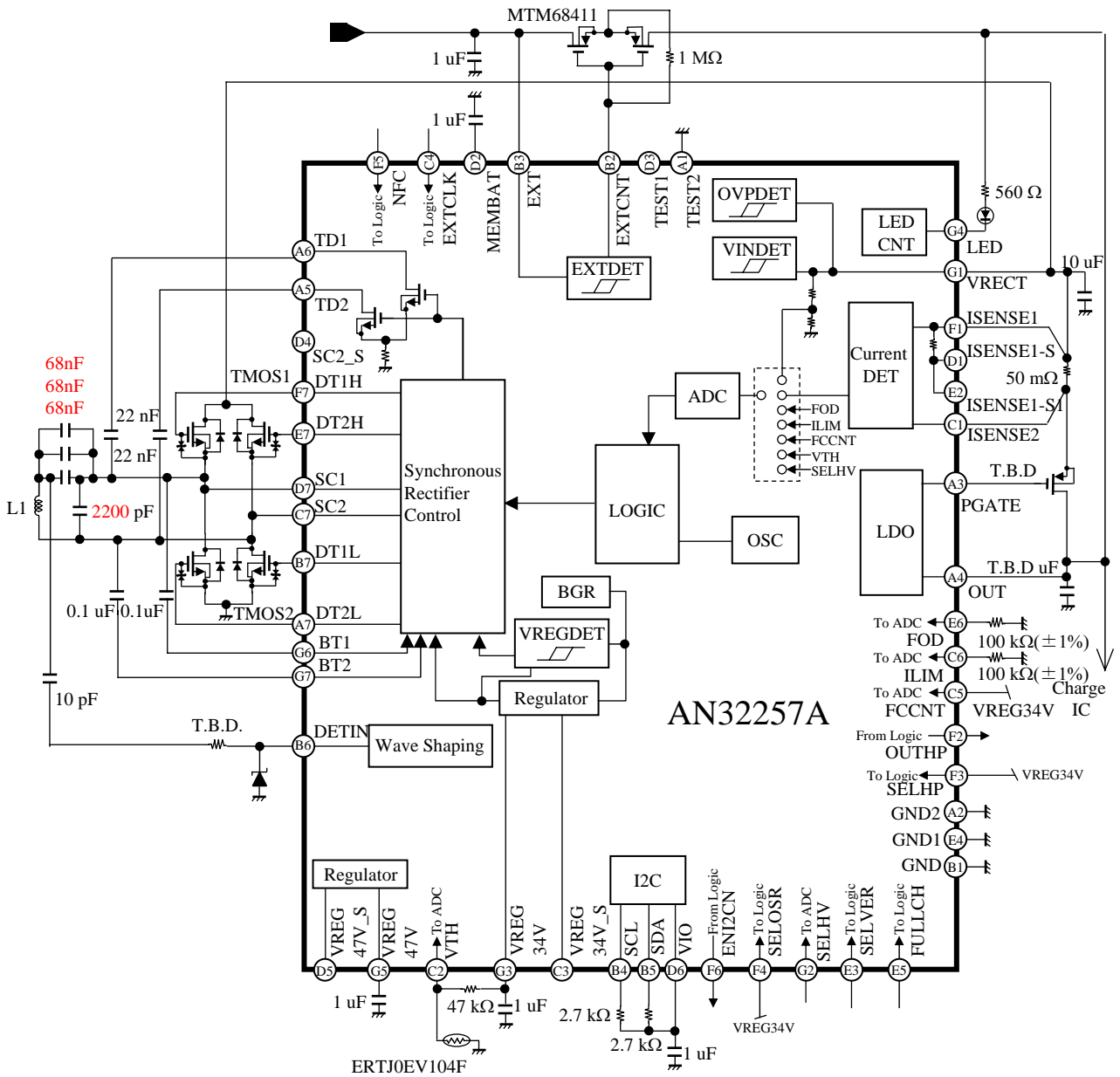
Note). Refer to a "Detail Description" and the "Application Information" for detailed information.

FUNCTIONAL BLOCK DIAGRAM : Composition corresponding to 5W



AN32257A

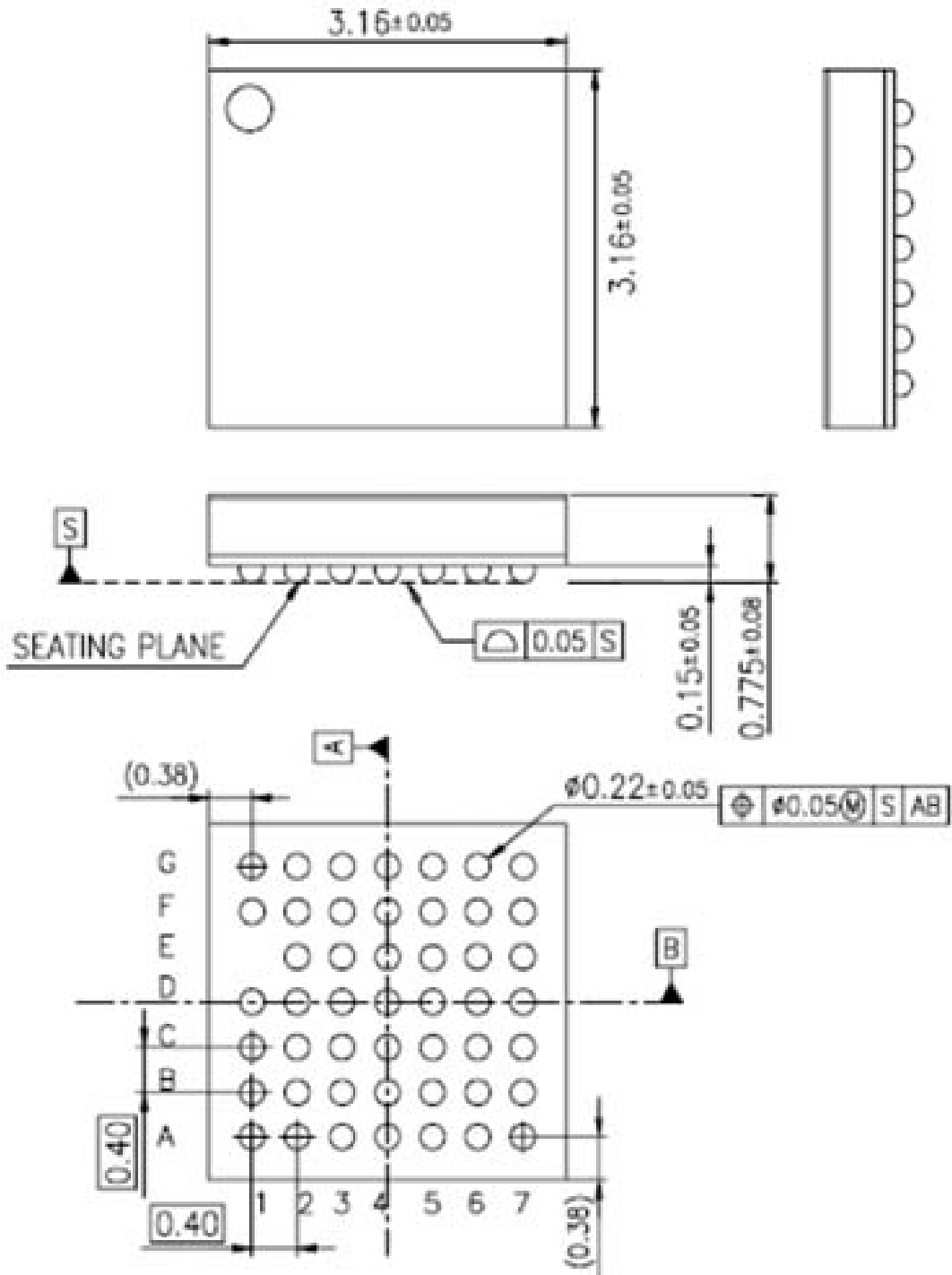
FUNCTIONAL BLOCK DIAGRAM : Composition corresponding to 10W



PACKAGE INFORMATION (Reference Data)

Package Code : XBGA048-W-3232AEL

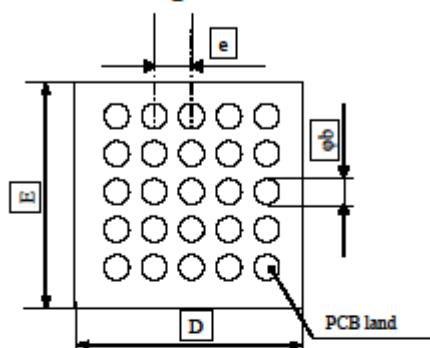
Unit : mm



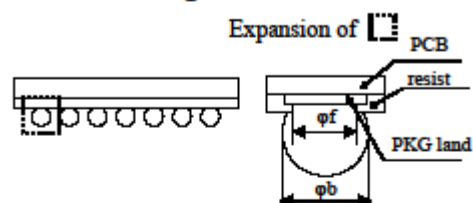
The reference spec. of PCB & Mask for WLCSP ver.1.0

Semiconductor Business Group
Industrial Devices Company
Panasonic Co.,Ltd.

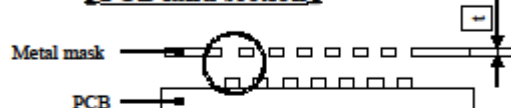
【PCB land figure】



【PKG section figure】

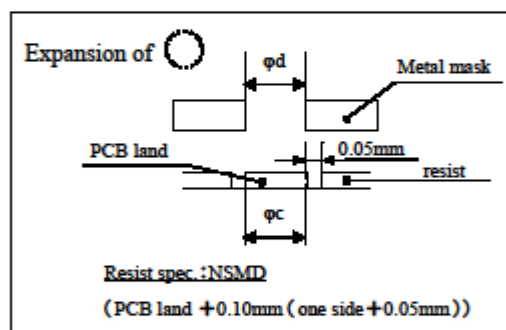


【PCB land section】



【Name of the collation letter】

Collation letter	Name
D	PKG length
E	PKG width



【Reference spec.】

unit:mm

Name	Symbol	Reference spec.			
Terminal pitch	e	0.50	0.50	0.40	0.30
PKG land	ϕf	0.23	0.25	0.20	0.15
Terminal diameter	ϕb	0.23	0.25/0.31	0.20/0.22	0.15
PCB land diameter	ϕc	0.27	0.30	0.23	0.15~0.18
Metal mask opening	ϕd	0.27	0.30	0.23	0.20~0.23
Metal mask thickness	t	0.08~0.11	0.08~0.11	0.08~0.11	0.08~0.11

*The above size is calculated based on the experiment results by Panasonic Corporation, and is not intended as a guarantee of mounting reliability. Mounting reliability can vary depending on factors such as the equipment specifications and conditions, material specifications and properties, and environmental conditions. To ensure satisfactory results, your company should evaluate and confirm actual mounting performance.

Functional explanation

1. All the functions

- Programmable Full Charge control setting
- Programmable Over Current Limit
- Selectable WPC Version
- Selectable Full Charge control through External Pin
- Adjustable Foreign Object Detection Threshold
- Selectable Power Range 5W or 10W mode
- Selectable between Internal/External Sense Resistor
- Option to send NFC request
- Selectable Output Voltage
- Report the frequency of the primary side

2. Programmable Full Charge Control Setting

When the charging current is less than the value set at FCCNT Pin (Pin No. C5).

Full Charge will be asserted and the output will be shut-off.

Example: By connecting 100k ohms between FCCNT pin and GND, An End Power Transfer Packet indicating Full Charge will be transmitted to the primary side when the charging current is less than or equal to 80mA (approximately) 5secs after charging begin.

Note: If this function is not required, it can be disable by connecting FCCNT pin to VREG34V.

3. Programmable Over Current Limit

If the output current goes beyond the value set at ILIM pin (Pin No. C6), output will be turned off due to Over-current.

Example: By connecting 100k ohms between ILIM pin and GND, End Power Transfer Packet indicating Over Current will be transmitted to the primary side when the output current is more than or equal to 1000mA.

Note: If this function is not required, it can be disable by connecting ILIM pin to VREG34V.

Under this condition, the default setting, 1500mA and 2500mA for 5W mode and 10W mode respectively for over-current will be set.

4. Selectable WPC Version

The WPC version can be selected between version 1.1 to 1.0 by connecting SELVER (Pin No. E3) to GND (Default) or VREG34V respectively.

5. Selectable Full Charge control through External Pin

If the FULLCH Pin (No. E5) is supplied an external voltage of level VREG34V, End Power Transfer Packet indication Full Charge will be transmitted to the primary side. Note that this external pin takes priority over the setting at FCCNT Pin.

6. Adjustable Foreign Object Detection Threshold

The Received Power value that will be sent to the primary side for Foreign Object Detection can be adjusted through the FOD Pin (Pin No. E6).

Example: By connecting 100k ohms between FOD pin and GND, the Received Power that will be transmitted to the primary side will be offset by +0W.

Note: If this function is not required, it can be disable by connecting FOD pin to VREG34V.

7. Selectable Power Range 5W or 10W mode

The Desired Power can be selected through SELHP (Pin No. F3). By connecting SELHP pin to GND, 5W (Default) will be selected. When SELHP pin is connected to VREG34V, 10W mode will be selected.

Note: 10W mode will only operate will the primary side is NN32251A. If the primary side is not NN32251A, it will operate in 5W mode even though SELHP may be set for 10W mode.

Functional explanation (Continue)

8. Selectable between Internal/External Sense Resistor

The current sensing resistors can be selected through SELOSR (Pin No. F4). When SELOSR is tied to GND, Internal sensing resistors (Default) will be used, otherwise, if SELOSR is tied to VREG34V, the sensing resistors shall be external discrete resistor.

Note: When set to 10W mode, please tied SELOSR pin to VREG34V so that external sensing resistors can be used.

This is reduce the heat generated when using 10W mode.

9. Option to send NFC request

User has the option to send NFC to the primary side by setting NFC pin (Pin No. F5) to VREG34V level. NFC request will be indicated to the primary side only when the primary side is NN32251A. And, in the event that the primary side support NFC transfer, power will be cut-off to facilitate NFC transfer.

10. Selectable Output Voltage

Output Voltage can be selected through SELHV (Pin No. G2). The setting is as follows:

OPEN:5V

GND:7V

VREG34V:6V

11. Report the frequency of the primary side

When an external clock of frequency 4MHz to 19MHz is input through EXTCLK (Pin No. C4), the transmit frequency during charging will be computed and recorded in the internal registers. User can check this value through Serial Bus (I2C).

Application information

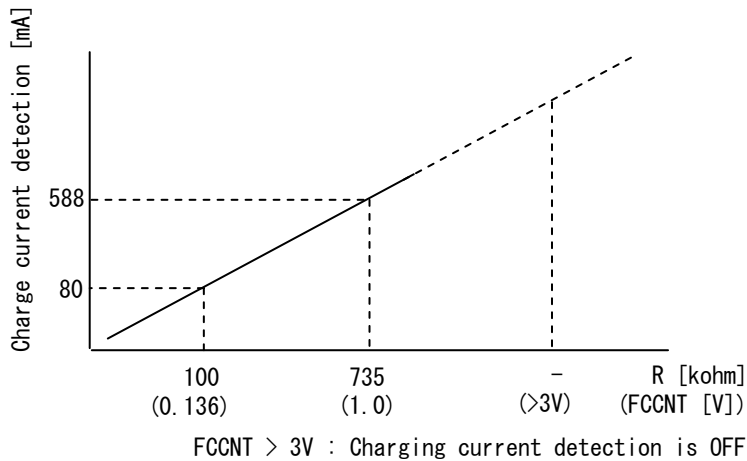
1. Full charge detection : FCCNT (Pin No. C5)

The threshold for full charge current can be preset through FCCNT pin. When the charging current falls below this threshold, full charge will be indicated to the primary side through End Power Transfer Packet. At the same time, the output will be turned off. Note that this happens only 5 seconds after charging begins.

This setting for the full charge current can be done through connecting resistor between FCCNT terminal and GND.

As an example, when 100kohm is connected between FCCNT terminal and GND, the threshold current is 80mA (Refer to the graph below).

When this function is not required, please connect FCCNT terminal directly to VREG34V.



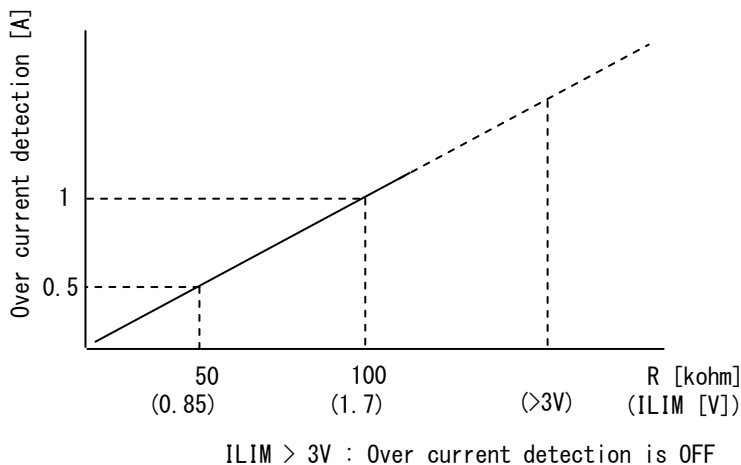
2. Over current detection : ILIM (Pin No. C6)

The threshold for Over Current Detection can be set through ILIM terminal.

As an example, when 100kohm is connected between ILIM terminal and GND, the threshold current will be about 1A. If the current goes beyond 1A under this setting, End Power Transfer Packet will be transmitted to a primary side indicating Over Current. At the same time, the output will be turned off.

When this function is not required, please connect ILIM terminal directly to VREG34V.

In this case, Over Current threshold will be 1.5A and 2.5A for 5W and 10W mode respectively.



Application information (Continue)

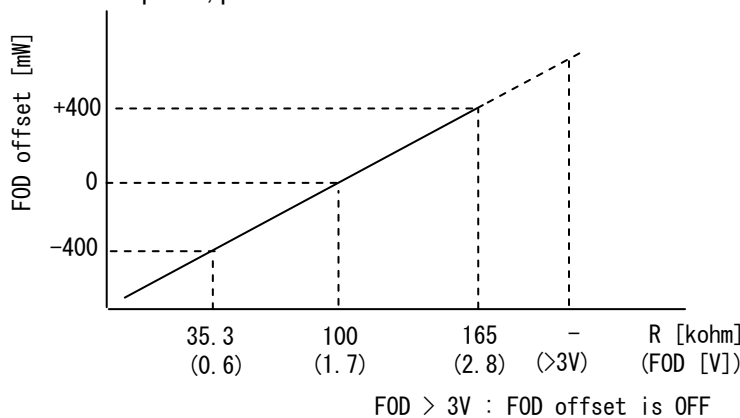
3. Foreign Object Detection offset setting : FOD (Pin No. E3)

The Foreign Object Detection function was added from WPC Ver.1.1.

In WPC ver 1.1, Foreign Object is judged by the Received Power (sent and calculated by secondary side) compared to the Transmitted Power by the primary side. In order to facilitate different structures/housing for the secondary side, AN32257A can add/subtract an offset for the received power through the FOD terminal.

As an example, when 100kohm is placed in between FOD terminal and GND, the offset value will be 0 (Refer to the chart below).

If this function is not required, please tied the FOD to VREG34V to disable it.



4. Frequency of a secondary coil : EXTCLK (Pin No. C4)

The frequency of the secondary coil is computed when EXTCLK terminal is provided with a clock frequency of 4MHz ~ 19MHz. The level of the input should be V_{in} . Subsequent, this computation will begin when register 0Ah is written 01h. The computation takes approximately 3ms.

User should read register 09h for the computed value. After which, frequency of the secondary coil can be calculated as follows:

$$\text{Frequency of a secondary coil} = \text{Fextclk} / \text{FREQCNT}[7:0]$$

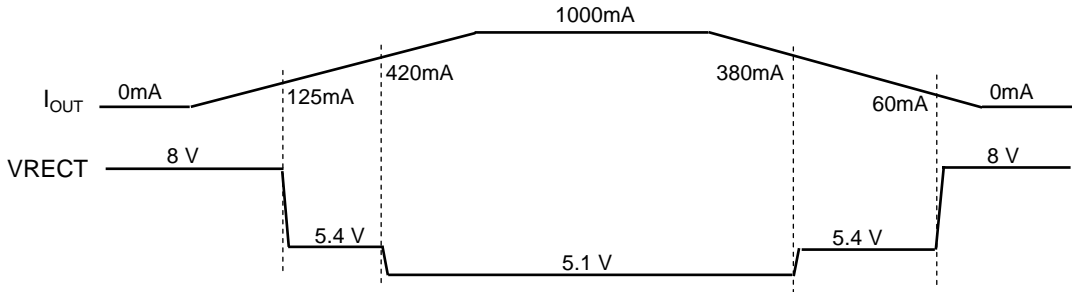
(Refer to page 28 for more details)

Application information (Continue)

5. Target control of VRECT voltage.

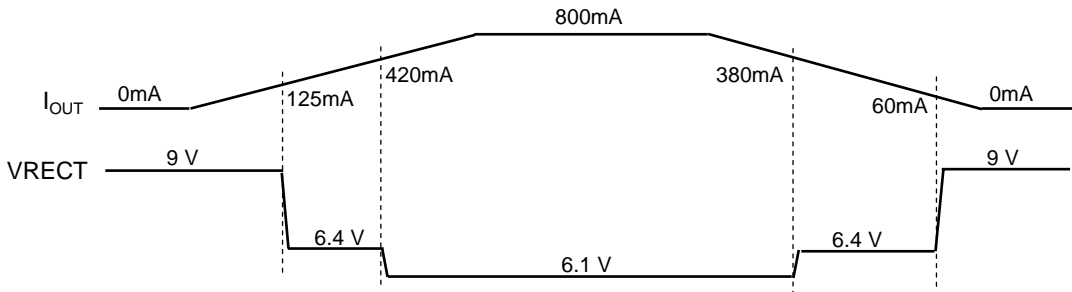
5W mode

OUT=5V setup : SELHV = OPEN



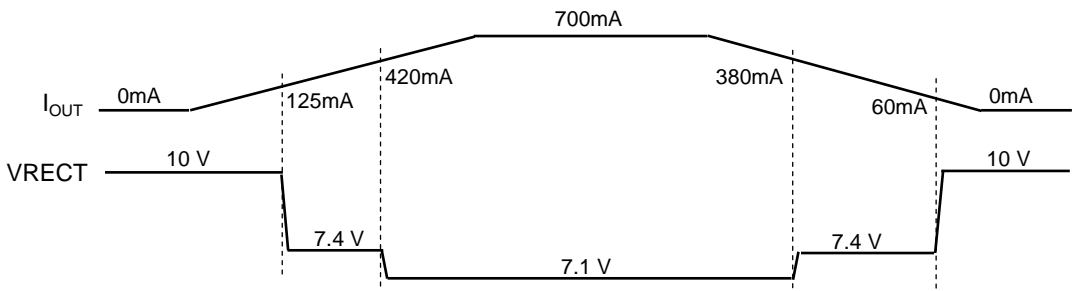
Note) The above is a value of reference.

OUT=6V setup : SELHV = VREG34V



Note) The above is a value of reference.

OUT=7V setup : SELHV = GND



Note) The above is a value of reference.

Application information (Continue)

6. LED Indication

Status	Indication
	LED
Standby	OFF
Charge	ON
Full Battery Detection	OFF
External Input Detection	OFF
Over-current Detection	OFF
Over-temperature Detection	OFF



Application information (Continue)

7. Register MAP

Normal register

Address	R/W	RESET要因	attribute	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
01h	R	NRESET	SIGNALSTR	SSV[7:0]							
Initial				0	0	0	0	0	0	0	0
02h	R	NRESET	EPTP	EPTP[7:0]							
Initial				0	0	0	0	0	0	0	0
03h	R	NRESET	CONTROL ERROR	CERR[7:0]							
Initial				0	0	0	0	0	0	0	0
04h	R	NRESET	RECEIVED POWER	RPWR[7:0]							
Initial				0	0	0	0	0	0	0	0
20h	R/W	NRESET	CONTROL POINT A	CTLPOINTA[7:0]							
Initial				0	1	1	0	0	1	1	0
21h	R/W	NRESET	CONTROL POINT B	CTLPOINTB[7:0]							
Initial				0	1	0	0	0	1	0	1
22h	R/W	NRESET	CONTROL POINT C	CTLPOINTC[7:0]							
Initial				0	1	0	0	0	0	0	1
23h	R/W	NRESET	CURRENT THRESH 1A	THRESH1A[7:0]							
Initial				0	0	0	1	0	0	0	0
24h	R/W	NRESET	CURRENT THRESH 1B	THRESH1B[7:0]							
Initial				0	0	0	0	1	0	0	0
25h	R/W	NRESET	CURRENT THRESH 2A	THRESH2A[7:0]							
Initial				0	0	1	1	0	1	1	0
26h	R/W	NRESET	CURRENT THRESH 2B	THRESH2B[7:0]							
Initial				0	0	1	1	0	0	0	0
27h	W	NRESET	TXEPTP	TXEPTP							
Initial				0	0	0	0	0	0	0	0
40h	R/W	NRESET	USER MODE SELECT	PRIVILEGE							
Initial				0	0	0	0	0	0	0	0
71h	R	NRESET	ID1	MAJOR VER[3:0]				MINOR VER[3:0]			
Initial				0	0	0	1	0	0	0	1
72h	R	NRESET	ID2	MANUFACTURE CODE[15:8]							
Initial				0	0	0	0	0	0	0	0
73h	R	NRESET	ID3	MANUFACTURE CODE[7:0]							
Initial				0	0	1	0	0	1	0	1
74h	R	NRESET	ID4	EXTID	BASIC DEVICE ID[30:24]						
Initial				0	0	0	0	0	0	0	0
75h	R	NRESET	ID5	BASIC DEVICE ID[23:9]							
Initial				0	0	0	0	0	0	0	0
76h	R	NRESET	ID6	BASIC DEVICE ID[15:8]							
Initial				0	0	0	0	0	0	0	0
77h	R	NRESET	ID7	BASIC DEVICE ID[7:0]							
Initial				0	0	0	0	0	0	0	0
80h	R	NRESET	CHARGE MODE	10W MODE							
Initial				0	0	0	0	0	0	0	0



Application information (Continue)

7. Register MAP (Continue)

Privilege register

Address	R/W	RESET要因	attribute	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
03h	R/W	PRIVILEGE	CONTROL ERROR	CERR7	CERR6	CERR5	CERR4	CERR3	CERR2	CERR1	CERR0
Initial				0	0	0	0	0	0	0	0
04h	R/W	PRIVILEGE	RECEIVED POWER	RPWR7	RPWR6	RPWR5	RPWR4	RPWR3	RPWR2	RPWR1	RPWR0
Initial				0	0	0	0	0	0	0	0
05h	R/W	PRIVILEGE	CHARGE STATUS	CHGSTATUS[7:0]							
Initial				1	1	1	1	1	1	1	1
07h	R	PRIVILEGE	VADC	VADC7	VADC6	VADC5	VADC4	VADC3	VADC2	VADC1	VADC0
Initial				0	0	0	0	0	0	0	0
08h	R	PRIVILEGE	IADC	IADC7	IADC6	IADC5	IADC4	IADC3	IADC2	IADC1	IADC0
Initial				0	0	0	0	0	0	0	0
09h	R	PRIVILEGE	FREQCNT	FREQCNT[7:0]							
Initial				0	0	0	0	0	0	0	0
0Ah	R/W	PRIVILEGE	EXTCLK ENABLE	—	—	—	—	—	—	—	EXTCLKEN
Initial				0	0	0	0	0	0	0	0
30h	R/W	PRIVILEGE	CTLP 10W VRECA	10WCTLPOINTA[7:0]							
Initial				0	1	1	0	0	1	1	0
31h	R/W	PRIVILEGE	CTLP 10W VRECB	10WCTLPOINTB[7:0]							
Initial				0	1	1	0	0	1	1	0
32h	R/W	PRIVILEGE	CTLP 10W VRECC	10WCTLPOINTC[7:0]							
Initial				0	1	0	0	0	0	0	1
33h	R/W	PRIVILEGE	CTLP KEY	—	—	—	—	—	—	—	CTLPKEY
Initial				0	0	0	0	0	0	0	0
41h	R/W	PRIVILEGE	FUNCTION SET	—	—	—	—	—	—	SETRPWR	SETCE
Initial				0	0	0	0	0	0	0	0
42h	R/W	NRESET	POWER PARAMETER 1	KA[7:0]							
Initial				0	0	0	0	1	1	0	0
43h	R/W	NRESET	POWER PARAMETER 2	KB[7:0]							
Initial				0	0	0	0	0	0	0	1
44h	R/W	NRESET	POWER PARAMETER 3	KC[7:0]							
Initial				0	0	0	0	1	1	1	1
45h	R/W	NRESET	POWER OFFSET	OFFSET[7:0]							
Initial				0	0	0	0	0	0	0	0
51h	R	PRIVILEGE	CONFIG1	PWR CLASS1	PWR CLASS0	MAXPWR5	MAXPWR4	MAXPWR3	MAXPWR2	MAXPWR1	MAXPWR0
Initial				0	0	0	0	1	0	1	0
53h	R/W	PRIVILEGE	CONFIG3	—	—	—	—	—	COUNT2	COUNT1	COUNT0
Initial				0	0	0	0	0	0	0	0
54h	R/W	PRIVILEGE	CONFIG4	WINDOW SIZE				WINDOW OFFSET			
Initial				1	0	0	0	0	1	0	0
60h	W	AUTORST	OPTREQ	—	—	—	—	—	—	—	OPTREQ
Initial				0	0	0	0	0	0	0	0
61h	R/W	PRIVILEGE	OPTCNT	—	—	—	OPTCNT4	OPTCNT3	OPTCNT2	OPTCNT1	OPTCNT0
Initial				0	0	0	0	0	0	1	1
62h	R/W	PRIVILEGE	OPTADR	OPTADR[7:0]							
Initial				0	0	0	0	0	1	1	0
63h	R/W	PRIVILEGE	OPTDATA1	OPTDATA1[7:0]							
Initial				0	0	0	0	0	0	0	0
64h	R/W	PRIVILEGE	OPTDATA2	OPTDATA2[7:0]							
Initial				0	0	0	0	0	0	0	0
65h	R/W	PRIVILEGE	OPTDATA3	OPTDATA3[7:0]							
Initial				0	0	0	0	0	0	0	0
66h	R/W	PRIVILEGE	OPTDATA4	OPTDATA4[7:0]							
Initial				0	0	0	0	0	0	0	0
67h	R	PRIVILEGE	OPTDATTX	—	—	—	—	OPT4TXWAIT	OPT3TXWAIT	OPT2TXWAIT	OPT1TXWAIT
Initial				0	0	0	0	0	0	0	0
71h	R/W	PRIVILEGE	ID1	MAJOR VER3	MAJOR VER2	MAJOR VER1	MAJOR VER0	MINOR VER	MINOR VER	MINOR VER	MINOR VER
Initial				0	0	0	1	0	0	0	1

Application information (Continue)

7. Register MAP (Continue)

Explanation

Register Name		SIGNALSTR							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
01h	R	SSV7	SSV6	SSV5	SSV4	SSV3	SSV2	SSV1	SSV0
Default	00h	0	0	0	0	0	0	0	0

D7-D0 : Signal Strength Value (0-255)

Signal Strength Value = VRECT Voltage / 20 × 255

Register Name		RPTP							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
02h	R	EPTP7	EPTP6	EPTP5	EPTP4	EPTP3	EPTP2	EPTP1	EPTP0
Default	00h	0	0	0	0	0	0	0	0

D7-D0 : End Power Transfer Packet

The message contained in a "End Power Transfer packet" is shown.

0x00 : EXT input detection

0x01 : Full charge

0x02 : Internal Fault ** This can be set by writing 01h to register 27h.

0x03 : Over temperature detection

0x04 : Over voltage detection

0x05 : Over current detection

Register Name		CONTROLERROR							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
03h	R	CERR7	CERR6	CERR5	CERR4	CERR3	CERR2	CERR1	CERR0
Default	00h	0	0	0	0	0	0	0	0

D7-D0 : Control Error Value (-128 - +127)

Application information (Continue)

7. Register MAP (Continue)

Explanation (Continue)

Register Name		RECEIVEDPOWER							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
04h	R	RPWR7	RPWR6	RPWR5	RPWR4	RPWR3	RPWR2	RPWR1	RPWR0
Default	00h	0	0	0	0	0	0	0	0

D7-D0 : Received Power Value(0-255)

The time range defined as the Configuration packet shows the average of the Power total amount which the secondary side received.

It is an integer of 0 to 255 without a mark.

Receiving Power's total amount is calculated below.

$$\text{Received Power} = (\text{RPWR}[7:0] / 128) \times (\text{Maximum Power} / 2) \times 10^{\text{Power Class W}}$$

* The Configuration packet defines Maximum Power and Power Class.

Register Name		CONTROLPOINT A							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
20h	R/W	CTLPOINT A7	CTLPOINT A6	CTLPOINT A5	CTLPOINT A4	CTLPOINT A3	CTLPOINT A2	CTLPOINT A1	CTLPOINT A0
Default	66h	0	1	1	0	0	1	1	0

D7-D0 : Control Point A(0-255)

The target value of VRECT voltage when current is less than 125mA is shown.

VRECT voltage is calculated below.

$$\text{VRECT voltage} = \text{CTLPOINTA}[7:0] / 255 \times 20 \text{ V}$$

*Initial value : 8.0 V

Register Name		CONTROLPOINT B							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
21h	R/W	CTLPOINT B7	CTLPOINT B6	CTLPOINT B5	CTLPOINT B4	CTLPOINT B3	CTLPOINT B2	CTLPOINT B1	CTLPOINT B0
Default	45h	0	1	0	0	0	1	0	1

D7-D0 : Control Point B(0-255)

The target value of VRECT voltage in case current is settled in the range of 125mA to 420mA is shown.

VRECT voltage is calculated below.

$$\text{VRECT voltage} = \text{CTLPOINTB}[7:0] / 255 \times 20 \text{ V}$$

* Initial value : 5.4 V

Application information (Continue)

7. Register MAP (Continue)

Explanation (Continue)

Register Name		CONTROLPOINT C							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
22h	R/W	CTLPOINT C7	CTLPOINT C6	CTLPOINT C5	CTLPOINT C4	CTLPOINT C3	CTLPOINT C2	CTLPOINT C1	CTLPOINT C0
Default	41h	0	1	0	0	0	0	0	1

D7-D0 : Control Point C(0-255)

The target value of VRECT voltage in case current is more than 420mA is shown.

VRECT voltage is calculated below.

$$\text{VRECT voltage} = \text{CTLPOINTC}[7:0] / 255 \times 20 \text{ V}$$

*Initial value : 5.1 V

Register Name		CURRENTTHRESH 1A							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
23h	R/W	THRESH1A 7	THRESH1A 6	THRESH1A 5	THRESH1A 4	THRESH1A 3	THRESH1A 2	THRESH1A 1	THRESH1A 0
Default	10h	0	0	0	1	0	0	0	0

D7-D0 : Current thresh 1A(0-255)

It is a setting register of a Control Point A/B change current threshold value (higher).

A current threshold value is calculated below.

$$\text{Current threshold} = \text{THRESH1A}[7:0] / 255 \times 2 \text{ A}$$

* Initial value : 125mA

Register Name		CURRENTTHRESH 1B							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
24h	R/W	THRESH1A 7	THRESH1A 6	THRESH1A 5	THRESH1A 4	THRESH1A 3	THRESH1A 2	THRESH1A 1	THRESH1A 0
Default	08h	0	0	0	0	1	0	0	0

D7-D0 : Current thresh 1B(0-255)

It is a setting register of a Control Point A/B change current threshold value (lower).

A current threshold value is calculated below.

$$\text{Current threshold} = \text{THRESH1B}[7:0] / 255 \times 2 \text{ A}$$

* Initial value : 60mA

Application information (Continue)

7. Register MAP (Continue)

Explanation (Continue)

Register Name		CURRENTTHRESH 2A							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
25h	R/W	THRESH2A 7	THRESH2A 6	THRESH2A 5	THRESH2A 4	THRESH2A 3	THRESH2A 2	THRESH2A 1	THRESH2A 0
Default	36h	0	0	1	1	0	1	1	0

D7-D0 : Current thresh 2A(0-255)

It is a setting register of a Control Point B/C change current threshold value (higher).

A current threshold value is calculated below.

$$\text{Current threshold} = \text{THRESH2A}[7:0] / 255 \times 2 \text{ A}$$

* Initial value : 420mA

Register Name		CURRENTTHRESH 2B							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
26h	R/W	THRESH2A 7	THRESH2A 6	THRESH2A 5	THRESH2A 4	THRESH2A 3	THRESH2A 2	THRESH2A 1	THRESH2A 0
Default	30h	0	0	1	1	0	0	0	0

D7-D0 : Current thresh 2B(0-255)

It is a setting register of a Control Point B/C change current threshold value (lower).

A current threshold value is calculated below.

$$\text{Current threshold} = \text{THRESH2B}[7:0] / 255 \times 2 \text{ A}$$

* Initial value : 380mA

Register Name		TXEPTP							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
27h	W	-	-	-	-	-	-	-	TXEPTP
Default	00h	0	0	0	0	0	0	0	0

D0 : TXEPTP

It is a compulsive transmitting register of an End Power Transfer packet.

0 : Normal operation (default)

1 : End Power Transfer packet transmission

* This register will automatically clear after sending the End Power Transfer packet.

Application information (Continue)

7. Register MAP (Continue)

Explanation (Continue)

Register Name		USER MORE SELECT							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
40h	R/W	-	-	-	-	-	-	-	PRIVILEGE
Default	00h	0	0	0	0	0	0	0	0

D0 : PRIVILEGE

This register controls the access to privilege register.

0 : Normal register map access only. (default)

1 : Access to privilege register and normal register.

Register Name		ID1							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
71h	R	MAJOR VER[3:0]				MINOR VER[3:0]			
Default	00h	0	0	0	1	0	0	0	1

D7-D4 : MAJOR VER[3:0]

Major Version of the WPC standard to which this LSI corresponds is shown.

0001 : Major Version (default)

D3-D0 : MINOR VER[3:0]

Minor Version of the WPC standard to which this LSI corresponds is shown.

0001 : Minor Version (default)

Register Name		ID2							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
72h	R	MANUFACTURE CODE[15:8]							
Default	00h	0	0	0	0	0	0	0	0

Register Name		ID3							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
73h	R	MANUFACTURE CODE[7:0]							
Default	25h	0	0	1	0	0	1	0	1

REGISTER 72h-73h[7:0] : MANUFACTURE CODE

Manufacture Code of Panasonic is shown.

0025 : Manufacture Code of Panasonic (default)

Application information (Continue)

7. Register MAP (Continue)

Explanation (Continue)

Register Name		ID 4							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
74h	R	EXTID	BASIC DEVICE ID[30:24]						
Default	00h	0	0	0	0	0	0	0	0

Register Name		ID 5							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
75h	R	BASIC DEVICE ID[23:16]							
Default	0Xh	0	0	0	0	X	X	X	X

Register Name		ID6							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
76h	R	BASIC DEVICE ID[15:8]							
Default	XXh	X	X	X	X	X	X	X	X

Register Name		ID7							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
77h	R	BASIC DEVICE ID[7:0]							
Default	XXh	X	X	X	X	X	X	X	X

REGISTER 74h[7] : Extended ID

The identification bit sequence of this LSI is chosen.

0 : Manufacturer Code || Basic Device ID (default)

1 : Manufacturer Code || Basic Device ID || Extended Device Identifier

REGISTER 74h-77h Basic Device ID[30:0]

Basic Device ID of this LSI is shown.

A random number is set to BASIC DEVICE ID [19:0].

Register Name		CHRG MODE							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
80h	R	-	-	-	-	-	-	-	10WMODE
Default	00h	0	0	0	0	0	0	0	0

D0 : 10W MODE

It is a register which shows the 10W mode.

By setup of SELHP=H, when the primary side corresponds (NN32251A), it becomes "H".

0 : 5W mode (default)

1 : 10W mode

Application information (Continue)

7. Register MAP (Continue)

Explanation (Continue)

Privilege register

Register Name		CONTROLERROR							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
03h	R/W	CERR7	CERR6	CERR5	CERR4	CERR3	CERR2	CERR1	CERR0
Default	00h	0	0	0	0	0	0	0	0

D7-D0 : Control Error Value (-128 - +127)

The contents of the Control Error packet are shown.

It is a signed integer of -128 to +127 in the complement form of 2.

By set up SETCE (Address41h, bit0) =“H”, the Control Error value written in this address is transmit.

Register Name		RECEIVEDPOWER							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
04h	R/W	RPWR7	RPWR6	RPWR5	RPWR4	RPWR3	RPWR2	RPWR1	RPWR0
Default	00h	0	0	0	0	0	0	0	0

D7-D0 : Received Power Value(0-255)

The time range defined as the Configuration packet shows the average of the power total amount which the secondary side received.

It is an integer of 0 to 255 without a mark.

The total amount of receiving power is calculated below.

$$\text{Received Power} = (\text{RPWR}[7:0] / 128) \times (\text{Maximum Power} / 2) \times 10^{\text{Power Class W}}$$

By set up SETRPWR (Address41h, bit1) =“H”, the Received Power value written in this address is transmit.

* The Configuration packet defines Maximum Power and Power Class.

Application information (Continue)

7. Register MAP (Continue)

Explanation (Continue)

Privilege register

Register Name		CHARGE STATUS							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
05h	R/W	CHGSTAT US7	CHGSTAT US6	CHGSTAT US5	CHGSTAT US4	CHGSTAT US3	CHGSTAT US2	CHGSTAT US1	CHGSTAT US0
Default	FFh	1	1	1	1	1	1	1	1

D7-D0 : Charge Status Value(0-100, 255)

The rate to a full charge level is shown.

00000000 : Empty

:

01100100 : Full charge

11111111 : Charge information cannot be given. (default)

Register Name		CONTROLERROR							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
07h	R	VADC7	VADC6	VADC5	VADC4	VADC3	VADC2	VADC1	VADC0
Default	00h	0	0	0	0	0	0	0	0

D7-D0 : VRECT Value (0 - +255)

The voltage level of VRECT is shown.

It is set to VADC[7:0] = FFh at the time of VRECT = 20V.

Register Name		RECEIVEDPOWER							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
08h	R	IADC7	IADC6	IADC5	IADC4	IADC3	IADC2	IADC1	IADC0
Default	00h	0	0	0	0	0	0	0	0

D7-D0 : ISENSE Value (0 - +255)

The current level of ISENSE is shown.

It is set to IADC[7:0] = FFh at the time of ISENSE current = 2A.

Application information (Continue)

7. Register MAP (Continue)

Explanation (Continue)

Privilege register

Register Name		FREQCNT							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
09h	R	FREQCNT7	FREQCNT6	FREQCNT5	FREQCNT4	FREQCNT3	FREQCNT2	FREQCNT1	FREQCNT0
Default	00h	0	0	0	0	0	0	0	0

D7-D0 : Coil Frequency (0-100, 255)

The counted value (average of 256 cycles) which counted the coil frequency Fcoil with the EXTCLK_IN clock is shown.

If frequency of EXTCLK_IN is made into Fext Hz, the coil frequency Fcoil will be calculate below.

$$F_{coil} = F_{ext} / FREQCNT[7:0] \text{ Hz}$$

Register Name		EXTCLK ENABLE							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0Ah	R	-	-	-	-	-	-	-	EXTCLKEN
Default	00h	0	0	0	0	0	0	0	0

D0 : EXTCLKEN

It is the clock input enabling register from EXTCLK_IN.

0 : EXTCLK_IN is invalid (default)

1 : EXTCLK_IN is effective

Application information (Continue)

7. Register MAP (Continue)

Explanation (Continue)

Privilege register

Register Name		CTLP 10W VREC A							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
30h	R/W	10WCTLPO INTA7	10WCTLPO INTA6	10WCTLPO INTA5	10WCTLPO INTA4	10WCTLPO INTA3	10WCTLPO INTA2	10WCTLPO INTA1	10WCTLPO INTA0
Default	66h	0	1	1	0	0	1	1	0

D7-D0 : 10W Control Point A(0-255)

In 10W mode, the target value of VRECT voltage of conditions with less current than 125mA is shown.

VRECT voltage is calculate below.

$$\text{VRECT voltage} = 10\text{WCTLPOINTA}[7:0] / 255 \times 20 \text{ V}$$

*Initial value : 8.0 V

Register Name		CTLP 10W VREC C							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
31h	R/W	10WCTLPO INTB7	10WCTLPO INTB6	10WCTLPO INTB5	10WCTLPO INTB4	10WCTLPO INTB3	10WCTLPO INTB2	10WCTLPO INTB1	10WCTLPO INTB0
Default	66h	0	1	1	0	0	1	1	0

D7-D0 : 10W Control Point B(0-255)

In 10W mode, the target value of VRECT voltage of conditions with current for 125mA to 420mA is shown.

VRECT voltage is calculate below.

$$\text{VRECT voltage} = 10\text{WCTLPOINTB}[7:0] / 255 \times 20 \text{ V}$$

*Initial value : 5.4 V

Register Name		CTLP 10W VREC C							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
32h	R/W	10WCTLPO INTC7	10WCTLPO INTC6	10WCTLPO INTC5	10WCTLPO INTC4	10WCTLPO INTC3	10WCTLPO INTC2	10WCTLPO INTC1	10WCTLPO INTC0
Default	41h	0	1	0	0	0	0	0	1

D7-D0 : 10W Control Point C(0-255)

In 10W mode, the target value of VRECT voltage of conditions with more current than 420mA is shown.

VRECT voltage is calculate below.

$$\text{VRECT voltage} = 10\text{WCTLPOINTC}[7:0] / 255 \times 20 \text{ V}$$

*Initial value : 5.1 V

Application information (Continue)

7. Register MAP (Continue)

Explanation (Continue)

Privilege register

Register Name		CTLP KEY							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
33h	R/W	-	-	-	-	-	-	-	CTLPKEY
Default	00h	0	0	0	0	0	0	0	0

D0 : CTLPKEY

A setup of Control Error in the 10W mode is chosen in a default or a register (Address 30h, 31h, 32h).

0 : Resistor invalid (default)

1 : Resistor effective

Register Name		FUNCTION SET							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
41h	R/W	-	-	-	-	-	-	SETRPWR	SETCE
Default	00h	0	0	0	0	0	0	0	0

D1 : SETRPWR

It is a register which transmits the Received Power value set as RPWR [7:0] (Address 04h).

0 : Normal operation (default)

1 : The Received Power value set as RPWR [7:0] is transmit.

* This register is not an auto clearance.

D0 : SETCE

It is a register which transmits the Control Error value set as CERR [7:0] (Address 03h).

0 : Normal operation (default)

1 : The Control Error value set as CERR [7:0] is transmit.

* This register is not an auto clearance.

Application information (Continue)

7. Register MAP (Continue)

Explanation (Continue)

Privilege register

Register Name		POWER PARAMETER 1							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
42h	R/W	KA[7:0]							
Default	0Ch	0	0	0	0	1	1	0	0
Register Name		POWER PARAMETER 2							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
43h	R/W	KB[7:0]							
Default	01h	0	0	0	0	0	0	0	1
Register Name		POWER PARAMETER 3							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
44h	R/W	KC [7:0]							
Default	0Fh	0	0	0	0	1	1	1	1
Register Name		POWER OFFSET							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
45h	R/W	OFFSET[7:0]							
Default	00h	0	0	0	0	0	0	0	0

REGISTER 42h, 43h, 44h, 45h : Power Parameter

Received Power is rectified by the following formulas and the above-mentioned register expresses each coefficient with this LSI.

$$\text{Received Power} = (\text{VRECT Value} + 4 \times \text{KA}) \times \text{ISENSE Value} / 1024 + \text{ISENSE Value}^2 / 1024 \times \text{KB} / 256 + \text{OFFSET} + \text{KC}$$

Application information (Continue)

7. Register MAP (Continue)

Explanation (Continue)

Privilege register

Register Name		CONFIG1							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
51h	R	PWRCLAS S1	PWRCLAS S0	MAXPWR5	MAXPWR4	MAXPWR3	MAXPWR2	MAXPWR1	MAXPWR0
Default	0Ah	0	0	0	0	1	0	1	0

D7-D6 : Power Class

It is a register which shows Power Class.

In WPC Version 1.1, it is set as "0".

D5-D0 : Maximum Power

It is a register which shows the maximum power supplied to the output of the rectifier which a secondary side expects.

The maximum power is calculated as follows.

$$\text{Maximum Power} = (\text{MAXPWR}[5:0] / 2) \times 10^{\text{PWRCLASS}[1:0]} \text{ W}$$

By this LSI, MAXPWR [5:0] is one of the two following values.

001010 : Maximum Power = 5W (default)

010100 : Maximum Power = 10W (10W mode)

Register Name		CONFIG 3							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
53h	R/W	-	-	-	-	-	COUNT2	COUNT1	COUNT0
Default	00h	0	0	0	0	0	0	0	0

D2-D0 : Count

It is a register which shows the number of the Optional (Power Control Hold-off time) packets which transmit by a Identification & configuration phase.

Before Identification packet transmission, when numerical values other than "000" are set to this register, the Power Control Hold-off time packet of the number of times of setting up is transmit.

000 : Optional packet does not transmit. (default)

001 : Power Control Hold-off time packet is transmitted once.

010 : Power Control Hold-off time packet is transmitted twice.

: :

111 : Power Control Hold-off time packet is transmitted 7 times.

*The Power Control Hold-off time value transmitted is 05h fixation.

Application information (Continue)

7. Register MAP (Continue)

Explanation (Continue)

Privilege register

Register Name		CONFIG 4							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
54h	R/W	WINDOWSIZE[4:0]					WINDOWOFFSET[2:0]		
Default	84h	1	0	0	0	0	1	0	0

D7-D3 : Window Size

It is a register showing the section which takes the average of Received Power.

- 00000 : 0ms
- 00001 : 4ms
- 00010 : 8ms
- : :
- 10000 : 64ms (default)
- : :
- 11110 : 120ms
- 11111 : 124ms

D2-D0 : Window Offset

It is a register showing the interval of the section and the Received Power packet which take the average of Received Power.

- 000 : 0ms
- 001 : 4ms
- 010 : 8ms
- : :
- 100 : 16ms (default)
- : :
- 110 : 24ms
- 111 : 28ms

Application information (Continue)

7. Register MAP (Continue)

Explanation (Continue)

Privilege register

Register Name		OPTREQ							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
60h	W	-	-	-	-	-	-	-	OPTREQ
Default	00h	0	0	0	0	0	0	0	0

D0 : OPTREQ

It is a Request to Send of the Optional (it sets up by Address 61h, 62 h, 63 h, 64 h, 65 h, and 66 h) packet which transmits by a Power Transfer phase.

0 : Optional packet does not transmit. (default)

1 : Optional packet is transmit.

*This register is an auto clearance.

Register Name		OPTCNT							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
61h	R/W	-	-	-	OPTCNT4	OPTCNT3	OPTCNT2	OPTCNT1	OPTCNT0
Default	84h	0	0	0	0	0	0	1	1

D4-D0 : OPTCNT

It is a register showing the size of the Optional packet which transmits by a Power Transfer phase.

Please set up message size +2 of a packet.

00000 : Don't set up.

00001 : Don't set up.

00010 : Don't set up.

00011 : Message size = 1 (default)

00100 : Message size = 2

: :

11110 : Message size = 28

11111 : Message size = 29

Application information (Continue)

7. Register MAP (Continue)

Explanation (Continue)

Privilege register

Register Name		OPTADR							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
62h	R/W	OPTADR[7:0]							
Default	06h	0	0	0	0	0	1	1	0

D7-D0 : OPTADR

It is a register showing the header of the Optional packet which transmits by a Power Transfer phase.

Register Name		OPTDATA1							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
63h	R/W	OPTDATA1[7:0]							
Default	00h	0	0	0	0	0	0	0	0

Register Name		OPTDATA2							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
64h	R/W	OPTDATA2[7:0]							
Default	00h	0	0	0	0	0	0	0	0

Register Name		OPTDATA3							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
65h	R/W	OPTDATA3[7:0]							
Default	00h	0	0	0	0	0	0	0	0

Register Name		OPTDATA4							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
66h	R/W	OPTDATA4[7:0]							
Default	00h	0	0	0	0	0	0	0	0

REGISTER 63h, 64h, 65h, 66h : OPTDATA

It is a register showing the message of the Optional packet which transmits by a Power Transfer phase.

Application information (Continue)

7. Register MAP (Continue)

Explanation (Continue)

Privilege register

Register Name		OPTDATTX							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
51h	R	-	-	-	-	OPT4TXW AIT	OPT3TXW AIT	OPT2TXW AIT	OPT1TXW AIT
Default	0Ah	0	0	0	0	0	0	0	0

D3-D0 : OPTDATTX

It is a register showing the transmitting state of the message of the Optional packet which transmits by a Power Transfer phase.

0 : Transmission is completed. (default)

1 : Transmission is not completed.

*Please do not write data in OPTDATA1 [7:0] at the time of OPT1TXWAIT = 1.

*Please do not write data in OPTDATA2 [7:0] at the time of OPT2TXWAIT = 1.

*Please do not write data in OPTDATA3 [7:0] at the time of OPT3TXWAIT = 1.

*Please do not write data in OPTDATA4 [7:0] at the time of OPT4TXWAIT = 1.

Register Name		OPTREQ							
Sub Address	R/W	D7	D6	D5	D4	D3	D2	D1	D0
71h	R/W	MAJORVE R3	MAJORVE R2	MAJORVE R1	MAJORVE R0	MINORVE R3	MINORVE R2	MINORVE R1	MINORVE R0
Default	00h	0	0	0	1	0	0	0	1

D7-D4 : MAJOR VER[3:0]

Major Version of the WPC standard to which this LSI corresponds is shown.

0001 : Major Version (default)

D3-D0 : MINOR VER[3:0]

Minor Version of the WPC standard to which this LSI corresponds is shown.

0001 : Minor Version (default)

IMPORTANT NOTICE

1. The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.
2. When using the LSI for new models, verify the safety including the long-term reliability for each product.
3. When the application system is designed by using this LSI, be sure to confirm notes in this book.
Be sure to read the notes to descriptions and the usage notes in the book.
4. The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information de-scribed in this book.
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Any applications other than the standard applications intended.
 - (1) Space appliance (such as artificial satellite, and rocket)
 - (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
 - (3) Medical equipment for life support
 - (4) Submarine transponder
 - (5) Control equipment for power plant
 - (6) Disaster prevention and security device
 - (7) Weapon
 - (8) Others : Applications of which reliability equivalent to (1) to (7) is requiredIt is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the IC described in this book for any special application, unless our company agrees to your using the IC in this book for any special application.
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9. Please use this product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive.
Our company shall not be held responsible for any damage incurred as a result of your using the IC not complying with the applicable laws and regulations.

1. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.

Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.
2. Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.
3. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.
4. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
5. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
6. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .

And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.
7. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.

Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.
8. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
9. The product which has specified ASO (Area of Safe Operation) should be operated in ASO
10. Verify the risks which might be caused by the malfunctions of external components.
11. Connect the metallic plates on the back side of the IC with their respective potentials (AGND, PVIN, LX). The thermal resistance and the electrical characteristics are guaranteed only when the metallic plates are connected with their respective potentials.

Revision History

Control No.	Revised Date	Page	Items	Before changes	After changes	Reason
AN32257A-1209E-0	2012.09.24	1-7	all	—	initial	
AN32257A-1211E-1	2012.11.22	4	Temperature Detector	VT _{THR} : 100 kohm (±1%) Typ spec: 0.457	VT _{THR} : TBD kohm (±1%) Typ spec: TBD	
		5	Resistor	—	Add Resistor connected to EXT CNT terminal	
		2	Supply voltage range V _{IO}	Min :1.65 Typ: 1.85	Min:TBD Typ: 3.3V	
		3	Termination (Full charge)	Tterm	Delete	
		-	Pin layout Functional	Add		
AN32257A-1212E-2	2012.12.27	2	Symbol Name	V _{ADP}	V _{EXP}	
		3~6	ELECTRICAL CHARACTERISTICS		Add & update	
		10, 11	Functional Block Diagram	I _{SENSE1-S} Open	I _{SENSE1-S} Connect 10W mode add	
		13	PACKAGE INFORMATION	—	Update	
		16~38	Add	—	Add Application information	
AN32257A-1301E3	2013.1.25	10, 11	Functional Block Diagram	Capacitor 47nF+4.7nF 680pF+2200pF	Capacitor 47nF+4.7nF+68nF+68nF 2200pF	
AN32257A-1302E-4	2013.2.5	10, 11	Functional Block Diagram	Capacitor 47nF+4.7nF+68nF+68nF	Capacitor 68nF+68nF+68nF	