

# BMA023

## Digital, triaxial acceleration sensor

### Data sheet

Bosch Sensortec



**BOSCH**

Invented for life

芯扬国际（香港）有限公司



#### BMA023 Data sheet

Order code 0 273 141 065


Package type 12-pin LGA

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## BMA023

### Digital, triaxial $\pm 2g/\pm 4g/\pm 8g$ acceleration sensor

#### Key features

- Three-axis accelerometer
- Small package      LGA package  
Footprint 3mm x 3mm, height 0.90mm
- Digital interface      SPI (4-wire, 3-wire), I<sup>2</sup>C, interrupt pin
- Programmable functionality      g-range  $\pm 2g/\pm 4g/\pm 8g$ , bandwidth 25-1500Hz, internal acceleration evaluation for interrupt trigger, self-test
- Ultra-low power ASIC      Low current consumption, short wake-up time, advanced features for system power management
- RoHS compliant
- Halogen-free

#### Typical applications

- Menu scrolling
- Tap sensing functionality
- Gaming
- Pedometer, step-counting
- Drop detection for warranty logging
- Display profile switching
- Advanced system power management for mobile applications
- Shock detection


#### General description

The BMA023 is a triaxial, low-g acceleration sensor IC with digital output for consumer market applications. It allows measurements of acceleration in three perpendicular axes.

An evaluation circuitry converts the output of a three-channel micromechanical acceleration-sensing structure that works according to the differential capacitance principle.


Package and interface have been defined to match a multitude of hardware requirements. Since the sensor IC has small footprint and flat package it is attractive for mobile applications. The sensor IC can be programmed to optimize functionality, performance and power consumption in customer specific applications.

The BMA023 senses tilt, motion and shock vibration in cell phones, handhelds, computer peripherals, man-machine interfaces, virtual reality features and game controllers.

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## 1. Specification

If not stated otherwise, the given values are maximum values over lifetime and full performance temperature/voltage range in the normal operation mode, and min./max. values represent 3-sigma limits.

**Table 1: Operating range, output signal and mechanical specifications of BMA023**

| Parameter                         | Symbol      | Condition                                | Min  | Typ        | Max       | Units        |
|-----------------------------------|-------------|--|------|------------|-----------|--------------|
| OPERATING RANGE                   |             |  |      |            |           |              |
| Acceleration range                | $g_{FS2g}$  | Switchable via serial digital interface  | -2   |            | 2         | g            |
|                                   | $g_{FS4g}$  |  | -4   |            | 4         | g            |
|                                   | $g_{FS8g}$  |  | -8   |            | 8         | g            |
| Supply voltage analogue           | $V_{DD}$    |  | 2.0  |            | 3.6       | V            |
| Supply voltage for digital I/O    | $V_{DDIO}$  | $V_{DDIO} \leq V_{DD}$                   | 1.62 |            | 3.6       | V            |
| Supply current in normal mode     | $I_{DD}$    | Digital and analog                       |      | 200        | 290       | $\mu$ A      |
| Supply current in stand-by mode * | $I_{DDsbm}$ | Digital and analog                       |      | 1          | 2         | $\mu$ A      |
| Operating temperature             | $T_A$       |  | -40  |            | +85       | $^{\circ}$ C |
| ACCELERATION OUTPUT SIGNAL        |             |  |      |            |           |              |
| Acceleration output resolution    |             | Format:<br>2's complement                |      |            | 10        | Bit          |
| Sensitivity                       | $S_{2g}$    | g-range $\pm 2g$ ,<br>$T_A=25^{\circ}$ C | 238  | 256        | 274       | LSB/g        |
|                                   | $S_{4g}$    | g-range $\pm 4g$ ,<br>$T_A=25^{\circ}$ C | 115  | 128        | 141       | LSB/g        |
|                                   | $S_{8g}$    | g-range $\pm 8g$ ,<br>$T_A=25^{\circ}$ C | 57   | 64         | 71        | LSB/g        |
| Sensitivity temperature drift     | TCS         | Over $T_A$                               |      | $\pm 0.03$ | $\pm 0.1$ | %/K          |
| Zero-g offset                     | Off         | $T_A=25^{\circ}$ C, calibrated           | -75  |            | +75       | mg           |
| Zero-g offset                     | Off         | $T_A=25^{\circ}$ C, over lifetime        | -180 |            | +180      | mg           |
| Zero-g offset temperature drift   | TCO         | Over $T_A$                               | -6   | 1          | +6        | mg/K         |
| Power supply rejection ratio      | PSRR        | Over $V_{DD}$                            |      |            | 0.2       | LSB/V        |


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| Parameter                                 | Symbol           | Condition                            | Min  | Typ.                       | Max  | Units                  |
|---|------------------|--------------------------------------|------|----------------------------|------|------------------------|
| Bandwidth                                 | bw               | 2 <sup>nd</sup> order analog filter  |      | 1500                       |      | Hz                     |
|   |                  | Digital filter **                    |      | 25, 50, 100, 190, 375, 750 |      | Hz                     |
| Acceleration data refresh rate (all axes) | f_rate           |                                      | 2700 | 3000                       | 3300 | Hz                     |
| Nonlinearity                              | NL               | Best fit straight line               | -0.5 |                            | 0.5  | %FS                    |
| Output noise                              | n <sub>rms</sub> | Rms                                  |      | 0.5                        |      | mg/ $\sqrt{\text{Hz}}$ |
| MECHANICAL CHARACTERISTICS                |                  |                                      |      |                            |      |                        |
| Cross axis sensitivity                    | $\bar{S}$        | Relative contribution between 3 axes |      |                            | 2    | %                      |
| POWERING UP CHARACTERISTICS               |                  |                                      |      |                            |      |                        |
| Wake-up time                              | t <sub>wu</sub>  | From standby                         |      | 1                          | 1.5  | ms                     |
| Start-up time                             | t <sub>su</sub>  | From power-off                       |      | 3                          |      | ms                     |

Notes:

\* For more details on the current consumption of the BMA023 during wake-up mode, please refer to chapter 7.3

\*\* Please refer to chapter 3.1.3 for more detailed explanations

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## 2. Maximum ratings


**Table 2:** Maximum ratings specified for the BMA023

| Parameter                 | Condition                      | Min  | Max    | Units |
|---------------------------|--------------------------------|------|--------|-------|
| Supply voltage            | $V_{DD}$ and $V_{DDIO}$        | -0.3 | 4.25   | V     |
| Storage temperature range |                                | -50  | +150   | °C    |
| Mechanical shock          | Duration $\leq 100\mu\text{s}$ |      | 10,000 | g     |
|                           | Duration $\leq 1.0\text{ms}$   |      | 2,000  | g     |
|                           | Free fall onto hard surfaces   |      | 1.5    | m     |
| ESD                       | HBM, at any pin                |      | 2      | kV    |
|                           | CDM                            |      | 500    | V     |

**Note:**

Stress above these limits may cause damage to the device. Exceeding the specified electrical limits may affect the device reliability or cause malfunction.

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### 3. Global memory map

All operational registers are accessible through serial interface with a standard protocol:

| Type of Register  | Function of Register   | Command      | Volatile / non-volatile               |
|-------------------|--|--------------|---------------------------------------|
| Data Registers    | <ul style="list-style-type: none"> <li>– Chip identification, chip version</li> <li>– Acceleration data</li> </ul> | Read<br>Read | non-volatile (hard coded)<br>volatile |
| Control Registers | <ul style="list-style-type: none"> <li>– Activating self test, soft reset, switch to sleep mode etc.</li> </ul>    | Read / Write | volatile                              |
| Status Registers  | <ul style="list-style-type: none"> <li>– Interrupt status and self test status</li> </ul>                          | Read         | Volatile                              |
|                   | <ul style="list-style-type: none"> <li>– Customer usable status bytes</li> </ul>                                   | Read / Write | volatile                              |
| Setting Register  | <ul style="list-style-type: none"> <li>– Functional settings (range, bandwidth)</li> </ul>                         | Read / Write | volatile                              |
|                   | <ul style="list-style-type: none"> <li>– Interrupt settings</li> </ul>   | Read / Write | volatile                              |
| EEPROM            | <ul style="list-style-type: none"> <li>– Default settings of functional and interrupt settings</li> </ul>          | Write        | non-volatile                          |
|                   | <ul style="list-style-type: none"> <li>– Trimming values</li> </ul>  | Protected    | non-volatile                          |
|                   | <ul style="list-style-type: none"> <li>– Bosch Sensortec reserved memory</li> </ul>                                | Protected    | non-volatile                          |

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Figure 1: Global memory map of BMA023

| Memory Region    | Register Address (hexadecimal) | bit7                      | bit6       | bit5           | bit4         | bit3        | bit2            | bit1          | bit0      | type       | Default setting |                 |    |
|------------------|--------------------------------|---------------------------|------------|----------------|--------------|-------------|-----------------|---------------|-----------|------------|-----------------|-----------------|----|
| Default Settings | 16h to 7Fh                     | reserved                  |            |                |              |             |                 |               |           | reserved   | NA              |                 |    |
|                  | Operational Registers          | 15h                       | SPI4       | enable_adv_INT | new_data_INT | latch_INT   | shadow_dis      | wake_up_pause | wake_up   |            | control         | 1 0 0 0 0 0 0 b |    |
|                  | 14h                            | reserved                  |            |                | range<1:0>   |             | bandwidth<2:0>  |               |           |            | control         | XXX 00 000 b    |    |
|                  | 13h                            | customer_reserved 2 <7:0> |            |                |              |             |                 |               |           |            |                 | status          | NA |
|                  | 12h                            | customer_reserved 1 <7:0> |            |                |              |             |                 |               |           |            |                 | status          | NA |
|                  | 11h                            | any_motion_dur            |            |                | HG_hyst<2:0> |             |                 | LG_hyst<2:0>  |           |            | settings        | NA              |    |
|                  | 10h                            | any_motion_thres<7:0>     |            |                |              |             |                 |               |           |            |                 | settings        | NA |
|                  | 0Fh                            | HG_dur<7:0>               |            |                |              |             |                 |               |           |            |                 | settings        | NA |
|                  | 0Eh                            | HG_thres<7:0>             |            |                |              |             |                 |               |           |            |                 | settings        | NA |
|                  | 0Dh                            | LG_dur<7:0>               |            |                |              |             |                 |               |           |            |                 | settings        | NA |
|                  | 0Ch                            | LG_thres<7:0>             |            |                |              |             |                 |               |           |            |                 | settings        | NA |
|                  | 0Bh                            | alert                     | any motion | counter_HG     |              |             | counter_LG      |               | enable HG | enable LG  | control         | 0               |    |
|                  | 0Ah                            | reserved                  | reset_INT  | reserved       | reserved     | self_test_1 | self_test_0     | soft_reset    | sleep     | control    | 0               |                 |    |
|                  | 09h                            | st_result                 | reserved   |                | alert_phase  | LG_latched  | HG_latched      | status_LG     | status_HG | status     | NA              |                 |    |
|                  | 08h                            | unused                    |            |                |              |             |                 |               |           |            |                 | data            | NA |
|                  | 07h                            | acc_z<9:2> (msb)          |            |                |              |             |                 |               |           |            |                 | data            | NA |
|                  | 06h                            | acc_z<1:0> (lsb)          |            |                | unused       |             |                 |               |           | new_data_z | data            | NA              |    |
|                  | 05h                            | acc_y<9:2> (msb)          |            |                |              |             |                 |               |           |            |                 | data            | NA |
|                  | 04h                            | acc_y<1:0> (lsb)          |            |                | unused       |             |                 |               |           | new_data_y | data            | NA              |    |
|                  | 03h                            | acc_x<9:2> (msb)          |            |                |              |             |                 |               |           |            |                 | data            | NA |
|                  | 02h                            | acc_x<1:0> (lsb)          |            |                | unused       |             |                 |               |           | new_data_x | data            | NA              |    |
|                  | 01h                            | al_version<3:0>           |            |                |              |             | ml_version<3:0> |               |           |            |                 | data            | NA |
|                  | 00h                            | unused                    |            |                |              |             |                 | chip_id<2:0>  |           |            | data            | ---- 010 b      |    |


**Important notes:**

1) Bits 5, 6 and 7 of register addresses 14h do contain critical sensor individual calibration data which must not be changed or deleted by any means.

In order to properly modify addresses 14h for range and/or bandwidth selection using bits 0, 1, 2, 3 and 4, it is highly recommended to read-out the complete byte, perform bit-slicing and write back the complete byte with unchanged bits 5, 6 and 7.

Otherwise the reported acceleration data may show incorrect results.

2) Bit 7, bit 5 and bit 4 of register 0Ah should be left at a value of "0".

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### 3.1 Operational registers

#### 3.1.1 SPI4

The SPI4 bit (address 15h, bit 7) is used to select the correct SPI protocol (three-wire or four-wire, SPI-mode 3). The default value is SPI4=1 (four-wire SPI is default value). After power on reset or soft reset it is recommended to set the SPI4-bit to the correct value.

This first writing is possible because only CSB, SCK and SDI are required for a write sequence and the 3 bit timing diagrams are identical in three-wire and four-wire configuration.

Recommended procedure: Set SPI4 to the correct value (SPI4=0 for SPI three-wire, SPI4=1 for SPI four-wire (=default)) every time after power on reset or soft reset.

#### 3.1.2 Range


These two bits (address 14h, bits 4 and 3) are used to select the full scale acceleration range. Directly after changing the full scale range it takes  $1/(2 \cdot \text{bandwidth})$  to overwrite the data registers with filtered data according to the selected bandwidth.

**Table 3:** Settings of full scale range register

| range<1:0> | Full scale acceleration range |
|------------|-------------------------------|
| 00         | +/- 2g                        |
| 01         | +/- 4g                        |
| 10         | +/- 8g                        |
| 11         | Not authorised code           |

#### Important note:

Please refer to the comment in chapter 3 of how to protect bits 5, 6 and 7 when modifying other bits of register 14h.

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### 3.1.3 Bandwidth

These three bits (address 14h, bits 2-0) are used to setup the digital filtering of ADC output data to obtain the desired bandwidth. A second order analogue filter defines the max. bandwidth to 1.5kHz. Digital filters can be activated to reduce the bandwidth down to 25Hz in order to reduce signal noise. The digital filters are moving average filters of various length with a refresh rate of 3kHz.

Since the bandwidth is reduced by a digital filter for the factor  $\frac{1}{2}$ ,  $\frac{1}{4}$ , ... of the analogue filter frequency of 1.5kHz the mean values of the bandwidth are slightly deviating from the rounded nominal values. Table 4 shows the corresponding data:

**Table 4:** Settings of bandwidth

| bandwidth<2:0> | Nominal selected bandwidth<br>[Hz] | Min. | Mean<br>bandwidth[Hz] | Max. |
|----------------|------------------------------------|------|-----------------------|------|
| 000            | 25                                 | -10% | 23                    | +10% |
| 001            | 50                                 |      | 47                    |      |
| 010            | 100                                |      | 94                    |      |
| 011            | 190                                |      | 188                   |      |
| 100            | 375                                |      | 375                   |      |
| 101            | 750                                |      | 750                   |      |
| 110            | 1500                               |      | 1500                  |      |
| 111            | Not authorised code                | -    | -                     | -    |

At wake-up from sleep mode to normal operation, the bandwidth is set to its maximum value and then reduced to bandwidth setting as soon as enough ADC samples are available to fill the whole digital filter.


Important note:

Please refer to the comment in chapter 3 of how to protect bits 5, 6 and 7 when modifying other bits of register 14h.

### 3.1.4 Wake\_up

This bit (address 15h, bit 0) makes BMA023 automatically switching from sleep mode to normal mode after the delay defined by wake\_up\_pause (section 3.1.5). When the sensor IC goes from sleep to normal mode, it starts acceleration acquisition and performs interrupt verification (section 3.2). The sensor IC automatically switches back from normal to sleep mode again if no fulfilment of programmed interrupt criteria has been detected. The IC wakes-up for a minimum duration which depends on the number of required valid acceleration data to determine if an interrupt should be generated.

If a latched interrupt is generated, this can be used to wake-up a microprocessor. The sensor IC will wait for a reset\_INT command and restart interrupt verification. BMA023 can not go back to sleep mode if reset\_INT is not issued after a latched interrupt.

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If a not-latched interrupt is generated, the device waits in the normal mode till the interrupt condition disappears. The minimum duration of interrupt activation is 330 $\mu$ s. If no interrupt is generated, the sensor IC goes to sleep mode for a defined time (wake\_up\_pause).

For more details on the wake-up functionality, please refer to chapter 7.3

### 3.1.5 Wake\_up\_pause

These bits (address 15h, bit 2 and 1) define the sleep phase duration between each automatic wake-up.


**Table 5:** Settings of wake\_up\_pause

| wake_up_pause<1:0> | Sleep phase duration |
|--------------------|----------------------|
| 00                 | 20 ms                |
| 01                 | 80 ms                |
| 10                 | 320 ms               |
| 11                 | 2560 ms              |

Note: The accuracy of the wake-up timer is about  $\pm 30\%$ .

### 3.1.6 Shadow\_dis

BMA023 provides the possibility to block the update of data MSB while LSB are read out. This avoids a potential mixing of LSB and MSB of successive conversion cycles. When this bit (address 15h, bit 3) is at 1, the blocking procedure for MSB is not realized and MSB only reading is possible.

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### 3.2 Interrupt settings

Five different types of interrupts can be programmed. When the corresponding criterion becomes valid, the interrupt pin is triggered to a high level. All interrupt criteria are combined and drive the interrupt pad with a Boolean <OR> condition.

Interrupt generations may be disturbed by changes of control bits because some of these bits influence the interrupt calculation. As a consequence, no write sequence should occur when microprocessor is triggered by interrupt or the interrupt should be deactivated on the microprocessor side when write sequences are operated.

Interrupt criteria are using digital code coming from digital filter output. As a consequence all thresholds are scaled with range selection (section 3.1.3.2). Timings used for high acceleration and low acceleration debouncing are absolute values (1 LSB of HG\_dur and LG\_dur registers corresponds to 1 millisecond, timing accuracy is proportional to oscillator accuracy = +/-10%), thus it does not depend on selected bandwidth. Timings used for any motion interrupt and alert detection are proportional to bandwidth settings (section 3.1.3).

#### 3.2.1 Enable\_LG

This bit (address 0Bh, bit 0) enables the LG\_thres criteria to generate an interrupt.

#### 3.2.2 Enable\_HG

This bit (address 0Bh, bit 1) enables the HG\_thres criteria to generate an interrupt.

#### 3.2.3 Enable\_adv\_INT


This bit (address 15h, bit 6) is used to disable advanced interrupt control bits (any\_motion, alert). If enable\_adv\_INT=0, writing to these bits has no effect on sensor IC function.

#### 3.2.4 Any\_motion

This bit ((address 0Bh, bit 6) enables the any motion criteria to generate directly an interrupt. It can not be turned on simultaneously with alert. This bit can be masked by enable\_adv\_INT, the value of this bit is ignored when enable\_adv\_INT=0 (section 3.2.3).

#### 3.2.5 Alert

If this bit (address 0Bh, bit 7) is at 1, the any\_motion criterion will set BMA023 into alert mode (section 3.2.9). This bit can be masked by enable\_adv\_INT, the value of this bit is ignored when enable\_adv\_INT=0 (section 3.2.3).

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### 3.2.6 Latch\_INT

If this bit (address 15h, bit 4) is at 1, interrupts are latched. The INT pad stays high until microprocessor detects it and writes reset\_INT control bit to 1 (section 3.3.1). When this bit is at 0, interrupts are set and reset directly by BMA023 according to programmable criteria (sections 3.2.7 and 3.2.8).

### 3.2.7 LG\_thres, LG\_hyst, LG\_dur, counter\_LG

LG\_thres (address 0C, bits 7-0 / low-g threshold) and LG\_hyst (address 11h, bits 2-0 / low-g threshold hysteresis) can basically (although not recommended with BMA023) be used to detect a free fall. The threshold and duration codes define one criterion for interrupt generation when absolute value of acceleration is low for long enough duration.

Data format is unsigned integer.

LG\_thres criterion\_x is true if  $|acc_x| \leq LG\_thres / 255 * range$

LG\_thres interrupt is set if (LG\_thres criterion\_x AND LG\_thres criterion\_y AND LG\_thres criterion\_z) AND interrupt counter = (LG\_dur+1)

LG\_thres criterion\_x is false if  $|acc_x| > (LG\_thres + 32*LG\_hyst) / 255 * range$

LG\_thres interrupt is reset if NOT(LG\_thres criterion\_x AND LG\_thres criterion\_y AND LG\_thres criterion\_z)

LG\_thres and LG\_hyst codes must be chosen to have  $(LG\_thres + 32*LG\_hyst) < 511$ .


When LG\_thres criterion becomes active, an interrupt counter is incremented by 1 LSB/ms. When the low-g interrupt counter value equals (LG\_dur+1), an interrupt is generated. Depending on counter\_LG (address 0Bh, bit 3 and 2) register, the counter could also be reset or count down when LG\_thres criterion is false.

**Table 6:** Description of debouncing counter counter\_LG

| counter_LG<1:0> | low acceleration interrupt counter status when LG_thres criteria is false |
|-----------------|---|
| 00              | reset   |
| 01              | Count down by 1 LSB/ms  |
| 10              | Count down by 2 LSB/ms  |
| 11              | Count down by 3 LSB/ms  |

If latch\_INT=0, the interrupt is not a latched interrupt and then it is reset as soon as LG\_thres criteria becomes false. When interrupt occurs, the interrupt counter is reset.

Remark: The LG\_thres criteria is set with an AND condition on all three axes to be used for free fall detection. However, please note due to the relatively wide sensitivity tolerance of the BMA023 the absolute threshold values for low-g and high-g interrupt can only provide a rough estimation of the motion profile.

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### 3.2.8 HG\_thres, HG\_hyst, HG\_dur, counter\_HG

HG\_thres (address 0Eh, bits 7-0 / high-g threshold) and HG\_hyst (address 11h, bits 5-3 / high-g threshold hysteresis) define the high-G level and its associated hysteresis. HG\_dur (high-g threshold qualification duration) and counter\_HG (address 0Bh, bits 5 and 4 / high-g counter down register) are used for debouncing the high-g criteria.

Threshold and duration codes define a criterion for interrupt generation when absolute value of acceleration is high for long enough duration.

The data format is unsigned integer.

HG\_threshold criterion\_x is true if  $|acc\_x| \geq HG\_thres / 255 * range$

HG\_threshold interrupt is set if  $(HG\_thres\_criterion\_x \text{ OR } HG\_thres\_criterion\_y \text{ OR } HG\_thres\_criterion\_z) \text{ AND } interrupt\ counter = (HG\_dur+1)$

HG\_threshold criterion\_x is false if  $|acc\_x| < (HG\_thres - 32*HG\_hyst) / 255 * range$

HG\_threshold interrupt is reset if  $NOT(HG\_thres\_criterion\_x \text{ OR } HG\_thres\_criterion\_y \text{ OR } HG\_thres\_criterion\_z)$


HG\_thres and HG\_hyst codes must be chosen to have  $(HG\_thres - 32*HG\_hyst) > 0$ .

When HG\_thres criterion becomes active, a counter is incremented by 1 LSB/ms. When the high-g acceleration interrupt counter value equals  $(HG\_dur+1)$ , an interrupt is generated. Depending on counter\_HG register value, the counter could also be reset or count down when HG\_thres criterion is false.

**Table 7:** Description of debouncing counter\_HG

| counter_HG<1:0> | High acceleration interrupt counter status when HG_thres criterion is false |
|-----------------|---|
| 00              | reset   |
| 01              | Count down by 1 LSB/ms  |
| 10              | Count down by 2 LSB/ms  |
| 11              | Count down by 3 LSB/ms  |

If latch\_INT=0, the interrupt is not a latched interrupt and then it is reset as soon as HG\_thres criterion becomes false. When interrupt occurs, the interrupt counter is reset.

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### 3.2.9 Any\_motion\_thres, any\_motion\_dur

For the evaluation using “any motion” criterion successive acceleration data from digital filter output are stored and moving differences for all axes are built. To calculate the difference the acceleration values of all axes at time t0 are compared to values at t0+3/(2\*bandwidth). The difference of both values is equal to the difference of two successive moving averages (from three data points).

The differential value is compared to a global critical threshold any\_motion\_thres (address 10h, bits 7-0). Interrupt can be generated when the absolute value of measured difference is higher than the programmed threshold for long enough duration defined by any\_motion\_dur (address 11h, bits 7 and 6).

Any\_motion\_thres and any\_motion\_dur data are unsigned integer. Any\_motion\_thres LSB size corresponds to 15.6mg for +/- 2g range and scales with range selection (section 3.1.2).

Any motion criterion is valid if  $|acc(t0)-acc(t0+3/(2*bandwidth))| \geq any\_motion\_thres$ .

An interrupt is set if (any motion criterion\_x OR any motion criterion\_y OR any motion criterion\_z) for any\_motion\_dur consecutive times.

The any motion interrupt is reset if NOT(any\_motion criterion\_x OR any\_motion criterion\_y OR any\_motion criterion\_z) for any\_motion\_dur consecutive times.


Table 8: any\_motion\_dur settings

| any_motion_dur<1:0> | Number of required consecutive conditions to set or reset the any motion interrupt |
|---------------------|--|
| 00                  | 1  |
| 01                  | 3  |
| 10                  | 5  |
| 11                  | 7  |

Any\_motion\_dur is used to filter the motion profile and also to define a minimum interrupt duration because the reset condition is also filtered.

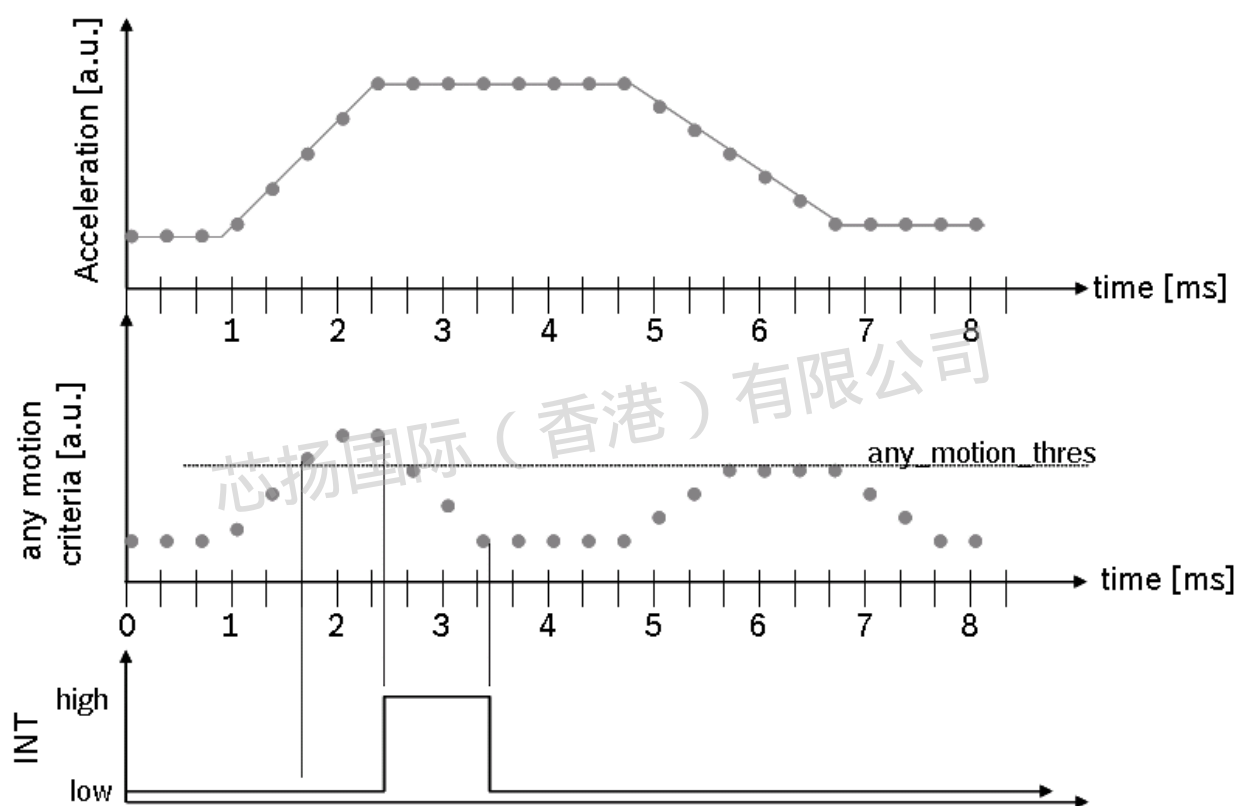
Any\_motion\_thres can be used to generate an any\_motion interrupt or to put BMA023 in alert mode to preload the low-g or high-g threshold logic (enables reduction of reaction time in tumbling mode); this is selected by alert bit (section 3.2.5). These two modes (any\_motion and alert) can not be turned on simultaneously.




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**Figure 2:** Any motion criterion (middle graph) is determined from digital filter output (upper graph) and depends on bandwidth settings: for example for any\_motion\_dur=01b and bandwidth=110b (1.5kHz), we have  $2 * \text{bandwidth} = 3 \text{ksamples/s}$  which leads to reaction for interrupt activation of  $3 * 333 \mu\text{s} = 1 \text{ms}$  and a minimum any motion interrupt duration of  $3 * 333 \mu\text{s} = 1 \text{ms}$  (see lower graph).

If lower bandwidth is selected i) the digitally filtered values (lower noise) are taken for the verification of the any motion criterion and ii) the time scale to evaluate the criterion is stretched. Thus adjusting the bandwidth, the any motion threshold, the any motion duration as well as the full scale range enables to tailor the sensitivity of the any motion algorithm.



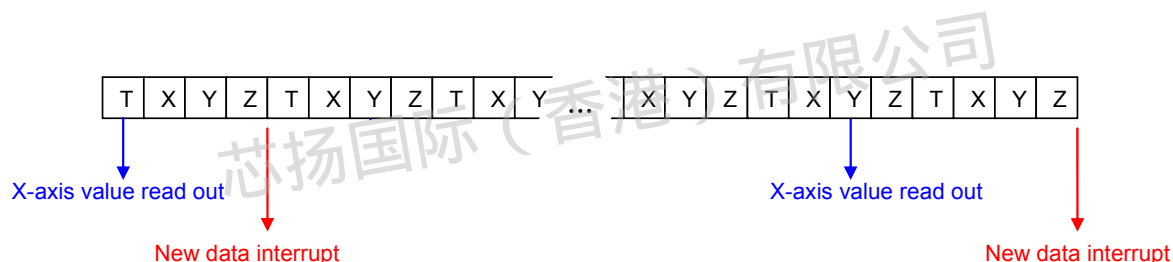
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### 3.2.10 New\_data\_int

If this bit (address 15h, bit 5) is set to 1, an interrupt will be generated when all three axes acceleration values are new, i.e. BMA023 updated all acceleration values after latest serial read-out. Interrupt generated from new data detection is a latched one; microcontroller has to write reset\_INT at 1 after interrupt has been detected high (section 3.3.1). This interrupt is also reset by any acceleration byte read procedure (read access to address 02h to 07h). New data interrupt always occurs at the end of the Z-axis value update in the output register (3kHz rate). Following figure shows two examples of X-axis read out and the corresponding interrupt generation.


**Figure 3:** Explanation of new data interrupt.

- left side - read out command of x-axis prior to next x-axis conversion  
 → new data interrupt after completion of current conversion cycle after z-axis conversion
- right side - read out of x-axis send after x-axis conversion  
 → new data interrupt at the end of next period when x axis has been updated



Please refer to chapter 8.1 for more details.

Note: When using the I<sup>2</sup>C interface for data transfer, the data read out phase can be longer than 330µs (depending on I<sup>2</sup>C clock frequency and the amount of data transmitted). Starting a new data read out sequence may lead to the situation that the new\_data\_int may not be cleared right in time. This must be considered and taken care of properly.

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### 3.3 Control registers

All single control bits are active at 1.

#### 3.3.1 Reset\_INT

This interrupt (address 0Ah, bit 6) is reset (interrupt pad goes to low) each time this bit is written to 1.

#### 3.3.2 Selftest\_0

The self-test command (address 0Ah, bit 2) uses electrostatic forces to move the MEMS common electrode. The result from selftest can be verified by reading st\_result (section 3.4.1). During the self-test procedure no external change of the acceleration should be generated.

#### 3.3.3 Selftest\_1

This self test bit (address 0Ah, bit3) does not generate any electrostatic force in the MEMS element but is used to verify the interrupt function is working correctly and that microprocessor is able to react to the interrupts.

0g acceleration is emulated at ADC input and the user can detect the whole logic path for interrupt, including the PCB path integrity. The LG\_thres register must be set to about 0.4g while LG\_dur = 0 to generate a low-g interrupt

#### 3.3.4 Soft\_reset

BMA023 is reset each time this bit (address 0Ah, bit 1) is written to 1. The effect is identical to power-on reset. Control, status and image registers are reset to values stored in the default setting registers (see also memory map). After soft\_reset or power-on reset BMA023 comes up in normal mode or wake-up mode. It is not possible to boot BMA023 to sleep mode.


No serial transaction should occur within 10 $\mu$ s after soft\_reset command.

The soft\_reset procedure may overwrite the SPI4 setting (section 3.1.1). Thus the correct interface configuration may have to be updated.

#### 3.3.5 Sleep

This bit (address 0Ah, bit 0) turns the sensor IC in sleep mode. Control and image registers are not cleared.

When BMA023 is in sleep mode no operation can be performed but wake-up the sensor IC by setting sleep=0 or soft\_reset. As a consequence all write and read operations are forbidden when the sensor IC is in sleep mode except command used to wake up the device or soft\_reset command. After sleep mode removal, it takes 1ms to obtain stable acceleration values (>99% data integrity).

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### 3.4 Status registers

#### 3.4.1 St\_result

This is the self test result bit (address 09h, bit 7). It can be used together with selftest\_0 control bit (section 3.3.4). After selftest\_0 has been set, self-test procedure starts. At the end selftest\_0 is written to 0 and microcontroller can react by reading st\_result bit. When st\_result=1 the self test passed successfully.

The result of the st\_result can be taken into account to evaluate the basic function of the sensor. Note: Evaluation of the st\_result bit should only be understood as one part of a wider functionality test. It should not be taken into consideration as the only criterion.

#### 3.4.2 Alert\_phase

This status bit (address 09h, bit 4) is set when BMA023 has been set to alert mode (section 3.2.5) and an any motion criterion has been detected. During alert phase, HG\_dur and LG\_dur variables are decreased to have a smaller reaction time when HG\_thres and LG\_thres thresholds are crossed; the decrease rate is by 1 ms per ms.

The alert mode is reset when an interrupt generated due to a high threshold or a low threshold event or when both HG\_dur and LG\_dur variables are at 0. When alert is reset, HG\_dur and LG\_dur variables come back to their original values stored in image registers.

#### 3.4.3 LG\_latched, HG\_latched


These status bits (address 09h, bit 3 and address 09h, bit 2) are set when the corresponding criteria have been issued. They are latched and thus only the microcontroller can reset them. When both high acceleration and low acceleration thresholds are enabled, these bits can be used by microprocessor to detect which criteria generated the interrupt.

#### 3.4.4 Status\_LG, status\_HG

These status bits (address 09h, bit 1 and address 09h, bit 2) are set when the corresponding criteria have been issued; they are automatically reset by BMA023 when the criteria disappear.

#### 3.4.5 Customer\_reserved 1, customer\_reserved 2

Both bytes (address 12h, bit 7-0 and address 13h, bit 7-0) can be used by customer. Writing or reading of these registers has no effect on the sensor IC functionality.

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### 3.5 Data registers

#### 3.5.1 Acc\_x, acc\_y, acc\_z

Acceleration values are stored in the following registers to be read out through serial interface.

acc\_x (02h, 7-6; 03h, 7-0)

acc\_y (04h, 7-6; 05h, 7-0)

acc\_z (06h, 7-6; 07h, 7-0)

The description of the digital signals acc\_x, acc\_y and acc\_z is “2’s complement”.

From negative to positive accelerations, the following sequence for the  $\pm 2g$  measurement range can be observed ( $\pm 4g$  and  $\pm 8g$  correspondingly):

|         |   |               |
|---------|---|---------------|
| -2.000g | : | 10 0000 0000  |
| -1.996g | : | 10 0000 0001  |
| ...     |   |               |
| -0.004g | : | 11 1111 1111  |
| 0.000g  | : | :00 0000 0000 |
| +0.004g | : | 00 0000 0001  |
| ...     |   |               |
| +1.992g | : | 01 1111 1110  |
| +1.996g | : | 01 1111 1111  |

Data is periodically updated (rate 3kHz) with values from the digital filter output. LSB acceleration bytes must be read first. After an acceleration LSB byte read access, the corresponding MSB byte update can optionally be blocked until it is also accessed for read. Thus, MSB / LSB mix from different samples can be avoided (section 3.1.6).


It is not possible to read-out only MSB bytes if shadow\_dis=0, an LSB byte must first be read out. To be able to read out only MSB byte, shadow\_dis must be written to 1.

new\_data\_\* flags on bits 0 of acc\_x (LSB), acc\_y (LSB) and acc\_z (LSB) can be used to detect if acceleration values have already been read out (section 3.5.3).

If systematic acceleration values read out is planned (for signal processing by the microcontroller), the interrupt pad can be programmed to flag the new data (section 3.2.10). Every time all three axes values have been updated, the interrupt goes high and microcontroller can read out data. With this method, microcontroller accesses are synchronized with internal sensor IC updates.

Synchronization of read-out sequence has several advantages:

- it enables a constant phase shift between acceleration conversion and its corresponding digital value read by microprocessor
- it reduces interface communication by avoiding over-sampling.
- potential noise due to serial interface activity perturbation would always be generated during a less critical phase of the conversion cycle. The maximum delay advised to start read out acceleration data is 20 $\mu$ s after INT high (window 0-80 $\mu$ s).

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### 3.5.2 New\_data\_x, new\_data\_y, new\_data\_z


These bits (New\_data\_x (02h, 0), new\_data\_y (04h, 0), new\_data\_z (06h, 0)) are flags which are turned at 1 when acceleration registers have been updated. Reading acceleration data MSB or LSB registers turns the flags at 0. The flag value can be read by microprocessor.

### 3.5.3 Al\_version, ml\_version, chip\_id

al\_version (address 01h, bit 7-4) and ml\_version (address 01h, bit 3-0) are used to identify the chip revision. These codes are programmed with metal layer.

chip\_id (address 00h, bit 2-0) is used by customer to be able to recognize BMA023. This code is fixed to 010b.

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## 4. Digital interface

BMA023 is capable to be adjusted to customer's specific hardware requirements. It provides three different digital interfaces (SPI 4-wire, SPI 3-wire, I<sup>2</sup>C) and an interrupt output pin.

The digital interface is used for regular reading of data registers (acceleration). For a complete read out of acceleration data two successive read cycles are required. The 10 bit coded data word is split into 8 MSB and 2 LSB. The most significant bit (MSB) is transferred first during address and data phases.

The serial interface is also used for verifying status registers or writing to control registers.

### 4.1 SPI

The SPI interfaces using three wire or four wire bus provide 16-bit protocols. Multiple read out is possible.

The communication is opened with a read/write control bit (R/W=0 for writing, R/W=1 for reading) followed by 7 address bits and at least 8 data bits (see figure 6 and figure 7). For a complete readout of 10 bit acceleration data from all axes the sensor IC provides the option to use an automatic incremented read command to read more than one byte (multiple read). This is activated when the serial enable pin CSB (chip select) stays active low after the read out of a data register. Thus, read out of data LSB will also cause read out of MSB if the CSB stays low for further 8 cycles of system clock.


The customer has the possibility to communicate with operational registers at addresses 00h-15h via SPI interface (chip identification Bytes, data Bytes, status and control registers with setting parameters). Access to the residual part of the memory map is locked (section 3.3.3). If the master addresses outside the range 00h-15h then SDI will go to tri-state enabling the communication of a second device on the same CSB and SDI line.

The CSB input has an internal 120kΩ pull-up resistor to V<sub>DDIO</sub>.

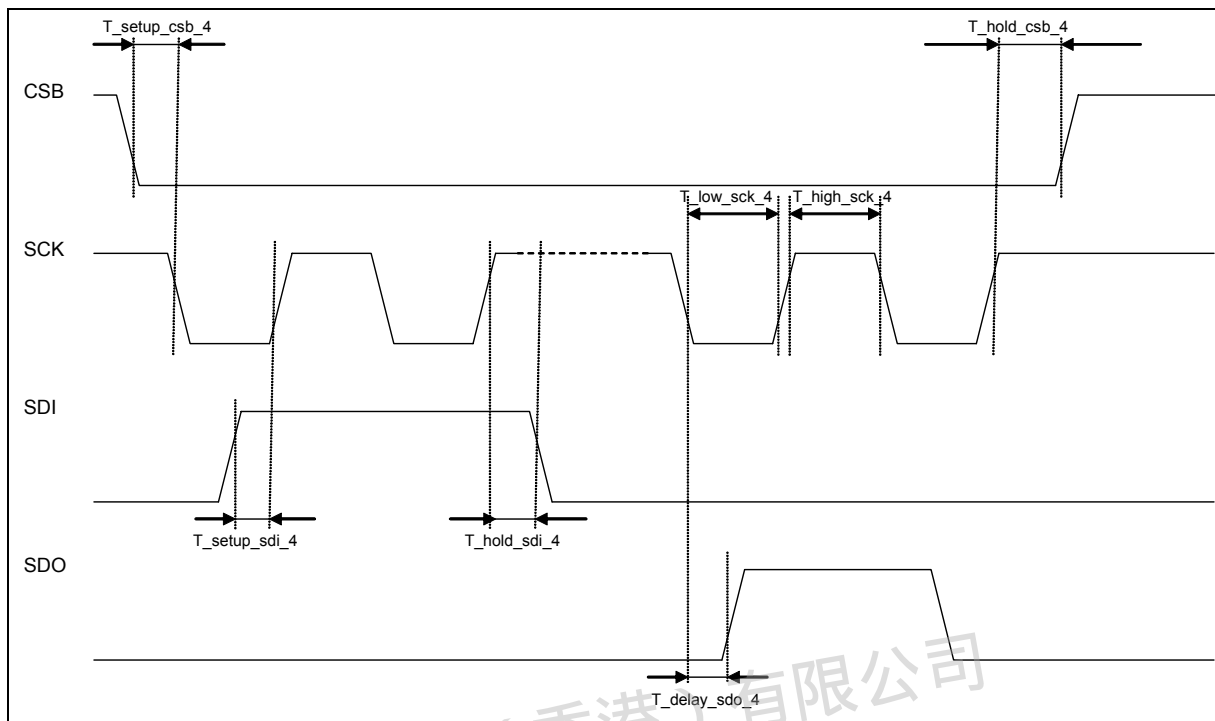
#### 4.1.1 Four-wire SPI interface

The 4-wire SPI is the default serial interface. The customer can easily activate the 3-wire SPI by writing a control bit (SPI4=0). The 4-wire SPI interface uses SCK (serial clock), CSB (chip select), SDI (serial data in) and SDO (serial data out).

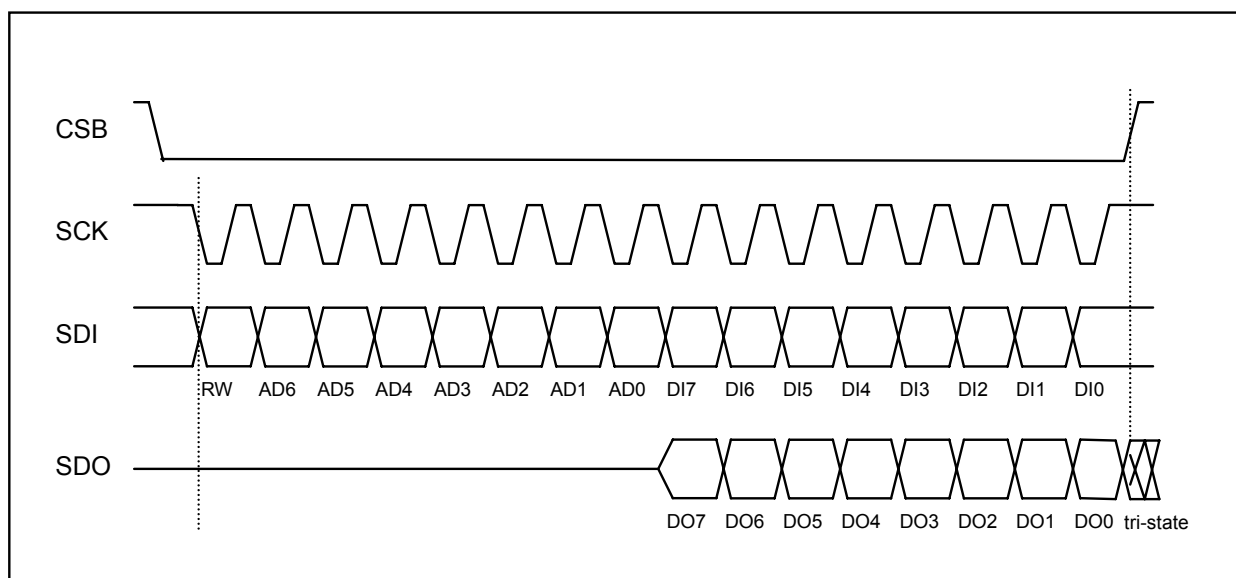
CSB is active low. Data on SDI is latched by BMA023 at SCK rising edge and SDO is changed at SCK falling edge (SPI mode 3). Communication starts when CSB goes to low and stops when CSB goes to high; during these transitions on CSB, SCK must be high. While CSB=1, no SDI change is allowed when SCK=1.

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**Figure 4: Timing diagram for four-wire SPI interface**



**Figure 5: Four wire SPI bit transfer**






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**Table 9:** Specification of four-wire SPI serial interface

| Interface parameters :      |              | Conditions                                       | Min.                  | Typ. | Max.                  | unit |
|-----------------------------|--------------|--|-----------------------|------|-----------------------|------|
| Input - low level           | Vil_si       | V <sub>DDIO</sub> =1.62V to 3.6V                 |                       |      | 0.3*V <sub>DDIO</sub> | V    |
| Input - high level          | Vih_si       | V <sub>DDIO</sub> =1.62V to 3.6V                 | 0.7*V <sub>DDIO</sub> |      |                       | V    |
| Output – low level          | Vol_SDI      | V <sub>DDIO</sub> =1.8V, iol=3 mA                |                       |      | 0.4                   | V    |
| Output – high level         | Voh_SDI      | V <sub>DDIO</sub> =1.8V, ioh=1mA                 | 1.4                   |      |                       | V    |
| Load capacitor (on SDO)     | Csdo_spi     | For 10MHz SPI transfer                           |                       |      | 25                    | pF   |
| CSB pull-up resistor        | CSB_pull_up  | Internal pull-up resistance to V <sub>DDIO</sub> | 70                    | 120  | 190                   | kΩ   |
| <b>4-wire SPI timings :</b> |              |  |                       |      |                       |      |
| SPI clock input frequency   | Fspi_4       |  |                       |      | 10                    | MHz  |
| SCK low pulse               | Tlow_sck_4   |  | 5                     |      |                       | ns   |
| SCK high pulse              | Thigh_sck_4  |  | 5                     |      |                       | ns   |
| SDI setup time              | Tsetup_sdi_4 |  | 5                     |      |                       | ns   |
| SDI hold time               | Thold_sdi_4  |  | 5                     |      |                       | ns   |
| SDO output delay            | Tdelay_sdo_4 |  |                       |      | 25                    | ns   |
| CSB setup time              | Tsetup_csb_4 |  | 5                     |      |                       | ns   |
| CSB hold time               | Thold_csb_4  |  | 5                     |      |                       | ns   |

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**Figure 6:** When write is required, sequences of 2 bytes are necessary: 1 control byte to define the address to be written and the data byte.

|         |    | Control byte           |   |   |   |   |   |   |   | Data byte                  |   |   |   |   |   |   |   |    |                        |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |         |
|---------|----|------------------------|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|----|------------------------|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|---------|
| Start   | RW | Register address (16h) |   |   |   |   |   |   |   | Data register - adress 1Eh |   |   |   |   |   |   |   | RW | Register address (0Bh) |   |   |   |   |   |   |   | Data register - adress 02h |   |   |   |   |   |   |   | Stop    |
| CSB = 0 | 0  | 0                      | 0 | 0 | 1 | 0 | 1 | 1 | 0 | X                          | X | X | X | X | X | X | X | X  | 0                      | 0 | 0 | 0 | 1 | 0 | 1 | 1 | X                          | X | X | X | X | X | X | X | CSB = 1 |

**Figure 7:** When read access is required, the sequence consists of 1 control byte to define first address to be read followed by data bytes. Addresses are automatically incremented as long as CSB stays active low.

|         |    | Control byte           |   |   |   |   |   |   |   | Data byte                  |   |   |   |   |   |   |   | Data byte                  |   |   |   |   |   |   |   | Data byte                  |   |   |   |   |   |   |   |         |  |
|---------|----|------------------------|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|---------|--|
| Start   | RW | Register address (02h) |   |   |   |   |   |   |   | Data register - adress 02h |   |   |   |   |   |   |   | Data register - adress 03h |   |   |   |   |   |   |   | Data register - adress 04h |   |   |   |   |   |   |   | Stop    |  |
| CSB = 0 | 1  | 0                      | 0 | 0 | 0 | 0 | 0 | 1 | 0 | X                          | X | X | X | X | X | X | X | X                          | X | X | X | X | X | X | X | X                          | X | X | X | X | X | X | X | CSB = 1 |  |

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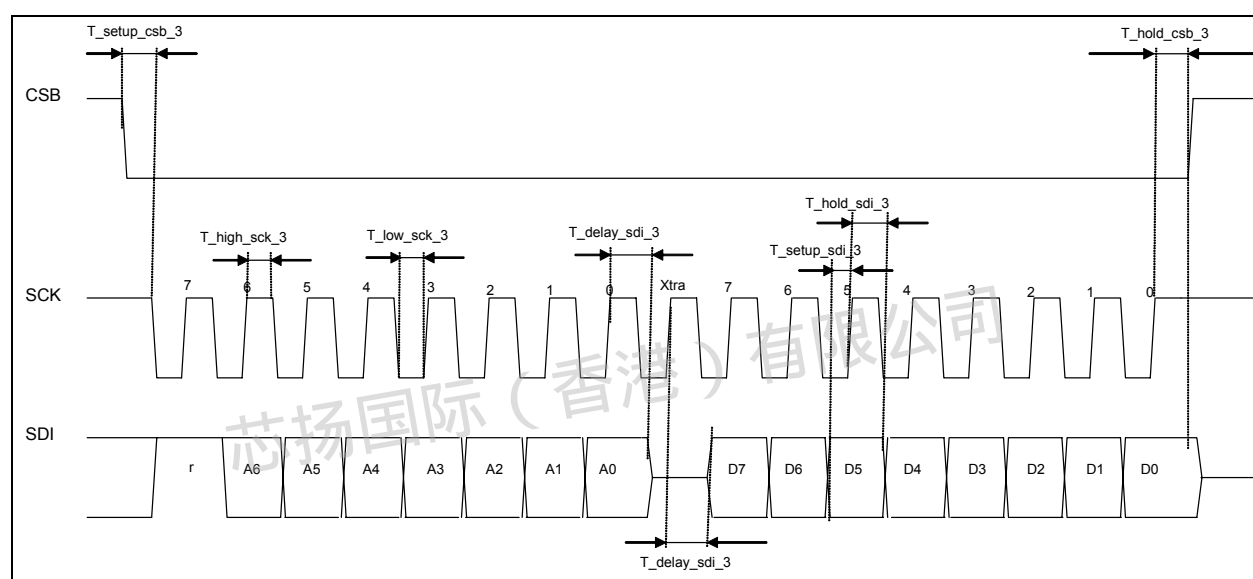
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#### 4.1.2 Three-wire SPI interface

3-wire SPI is not the default serial interface. The customer can easily activate the 3-wire SPI by setting a control bit (SPI4=0). The 3-wire SPI interface uses SCK (serial clock), CSB (chip select, active low) and SDA (serial data in/out). A maximum clock frequency up to 70MHz can be handled.

The protocol data acquisition by the sensor IC occurs at the rising edge of SCK. The output data provided by the sensor IC is synchronized also on the rising edges of SCK. The 3-wire read protocol needs one extra clock cycle between address byte and data output byte.


**Figure 8:** Timing diagram for three-wire SPI interface (SDI = SDA)



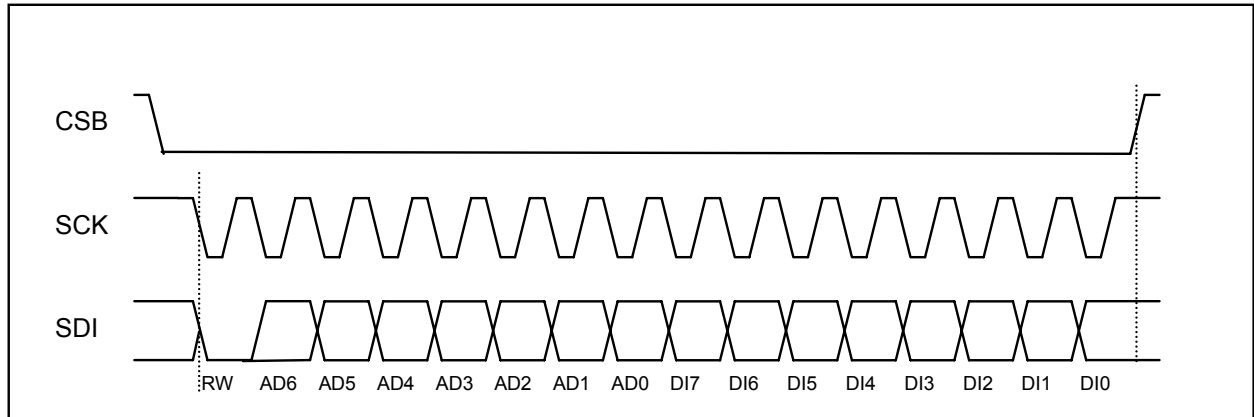
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|  <b>BOSCH</b> | Data sheet<br><b>BMA023</b><br>Digital, triaxial acceleration sensor | Bosch Sensortec |
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**Table 10:** Specification of three-wire SPI serial interface

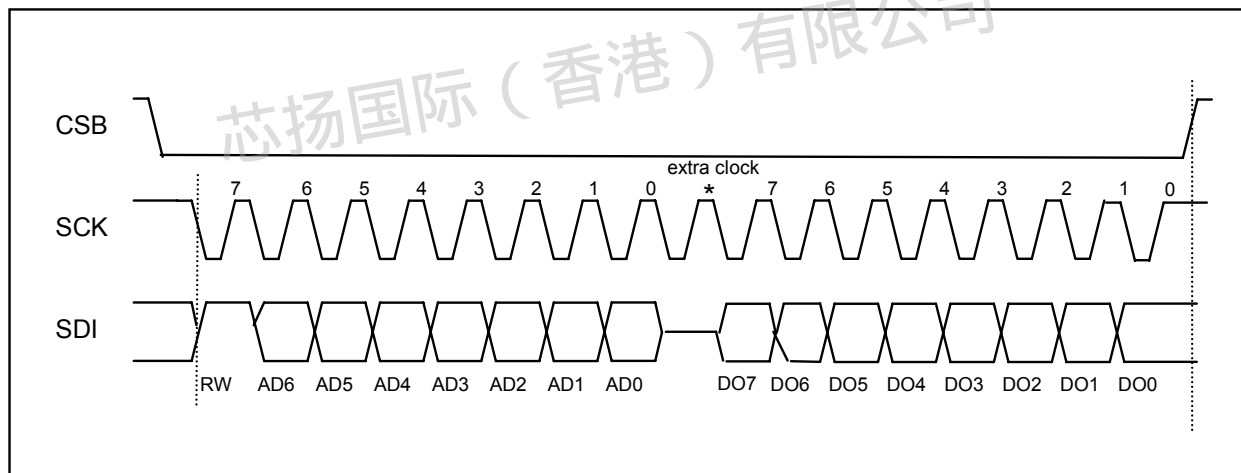
|                              |              | Conditions  | Min.                  | Typ. | Max.                  | unit |
|------------------------------|--------------|---|-----------------------|------|-----------------------|------|
| Input - low level            | Vil_si       | V <sub>DDIO</sub> =1.62V to 3.6V                    |                       |      | 0.3*V <sub>DDIO</sub> | V    |
| Input - high level           | Vih_si       | V <sub>DDIO</sub> =1.62V to 3.6V                    | 0.7*V <sub>DDIO</sub> |      |                       | V    |
| Output – low level           | Vol_SDI      | V <sub>DDIO</sub> =1.8V,<br>iol=3 mA                |                       |      | 0.4                   | V    |
| Output – high level          | Voh_SDI      | V <sub>DDIO</sub> =1.8V, ioh=1mA                    | 1.4                   |      |                       | V    |
| CSB pull-up resistor         | CSB_pull_up  | Internal pull-up<br>resistance to V <sub>DDIO</sub> | 70                    | 120  | 190                   | kΩ   |
| Load capacitor<br>(on SDO)   | Csdo_spi     | for 70MHz<br>SPI transfer                           |                       |      | 10                    | pF   |
| <b>3-wire SPI timings :</b>  |              |   |                       |      |                       |      |
| SPI clock<br>input frequency | Fspi_3       |   |                       |      | 70                    | MHz  |
| SCK low pulse                | Tlow_sck_3   |   | 5                     |      |                       | ns   |
| SCK high pulse               | Thigh_sck_3  |   | 5                     |      |                       | ns   |
| SDI setup time               | Tsetup_sdi_3 |   | 3.8                   |      |                       | ns   |
| SDI hold time                | Thold_sdi_3  |   | 2                     |      |                       | ns   |
| SDI output delay             | Tdelay_sdi_3 | when SDI<br>is an output for read                   |                       |      | 10.5                  | ns   |
| CSB setup time               | Tsetup_csb_3 |   | 5                     |      |                       | ns   |
| CSB hold time                | Thold_csb_3  |   | 5                     |      |                       | ns   |


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**Figure 9:** The three wire SPI write protocol is identical to four wire bus



**Figure 10:** For three wire read protocol one extra clock between address byte and data out byte is required. Output data are changed on SDI (SDI=SDA) by SCK rising edge and should be latched by microprocessor during next SCK rising edge.

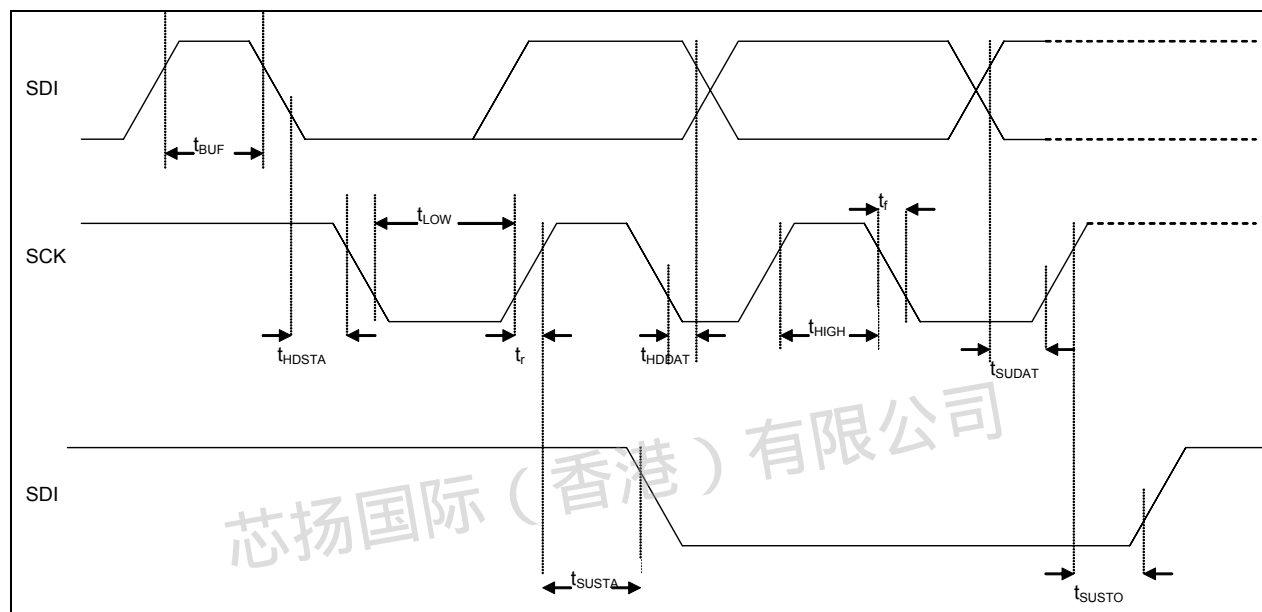



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### 4.2 I<sup>2</sup>C interface

The I<sup>2</sup>C bus uses SCK (serial clock) and SDA (=SDI, serial data input/output). SDA is bidirectional with open drain; it must be connected externally to V<sub>DDIO</sub> via a pull up resistor. CSB is not used and must be connected to V<sub>DDIO</sub>.


**Figure 11:** Timing diagram for I<sup>2</sup>C interface (SDI=SDA)



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**Table 11:** Specification of I<sup>2</sup>C serial interface (SDI=SDA)

| Interface parameters :                    |                  | Conditions                        | Min.                  | Typ. | Max.                  | unit |
|---|------------------|-----------------------------------|-----------------------|------|-----------------------|------|
| Input - low level                         | Vil_si           | V <sub>DDIO</sub> =1.62V to 3.6V  |                       |      | 0.3*V <sub>DDIO</sub> | V    |
| Input - high level                        | Vih_si           | V <sub>DDIO</sub> =1.62V to 3.6V  | 0.7*V <sub>DDIO</sub> |      |                       | V    |
| Output – low level                        | Vol_SDI          | V <sub>DDIO</sub> =1.8V, iol=3 mA |                       |      | 0.4                   | V    |
| Output – high level                       | Voh_SDI          | V <sub>DDIO</sub> =1.8V, ioh=1mA  | 1.4                   |      |                       | V    |
| I <sup>2</sup> C bus load capacitor       | Cb               | On SDI and SCK                    |                       |      | 100                   | pF   |
| <b>I<sup>2</sup>C timings :</b>           |                  |                                   |                       |      |                       |      |
| SCK frequency                             | F <sup>I2C</sup> |                                   |                       |      | 3.4                   | MHz  |
| SCK low period                            | Tlow             |                                   | 160                   |      |                       | ns   |
| SCK high period                           | Thigh            |                                   | 60                    |      |                       | ns   |
| SDI setup time                            | Tsudat           |                                   | 10                    |      |                       | ns   |
| SDI hold time                             | Thddat           |                                   | 10                    |      | 70                    | ns   |
| Setup time for a repeated start condition | Tsusta           |                                   | 160                   |      |                       | ns   |
| Hold time for a start condition           | Thdsta           |                                   | 160                   |      |                       | ns   |
| Setup time for a stop condition           | Tsusto           |                                   | 160                   |      |                       | ns   |
| Time before a new transmission can start  | Tbuf             |                                   | 100                   |      |                       | ns   |

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#### Start and stop conditions:

Data transfer begins by a falling edge on SDA when SCK is high (start condition (S) indicated by I<sup>2</sup>C bus master). Stop condition (P) is a rising edge on SDA when SCK is high (see figure 12).

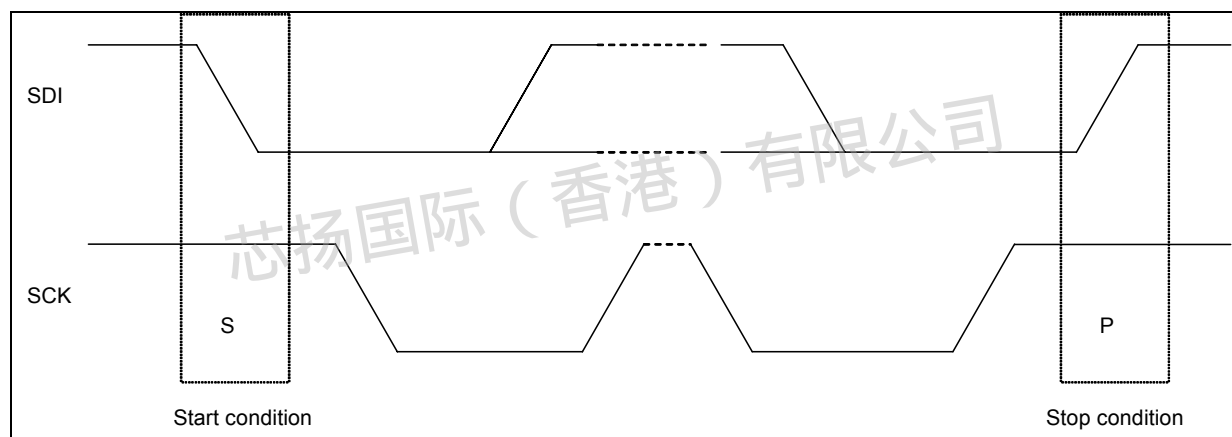
#### Bit transfer:

One data bit is transferred during each SCK pulse. Data on SDA line must remain stable during high period of SCK pulse (see figure 13).


#### Acknowledge:

After start condition each byte of data transfer is followed by an acknowledge bit. The transmitter let the SDA line high (no pull down) and generates a high SCK pulse. If BMA023 has been addressed and data transfer has performed correctly it generates a low SDA level (active pull down). Then SDA line is let free enabling the next transfer (see figure 14).

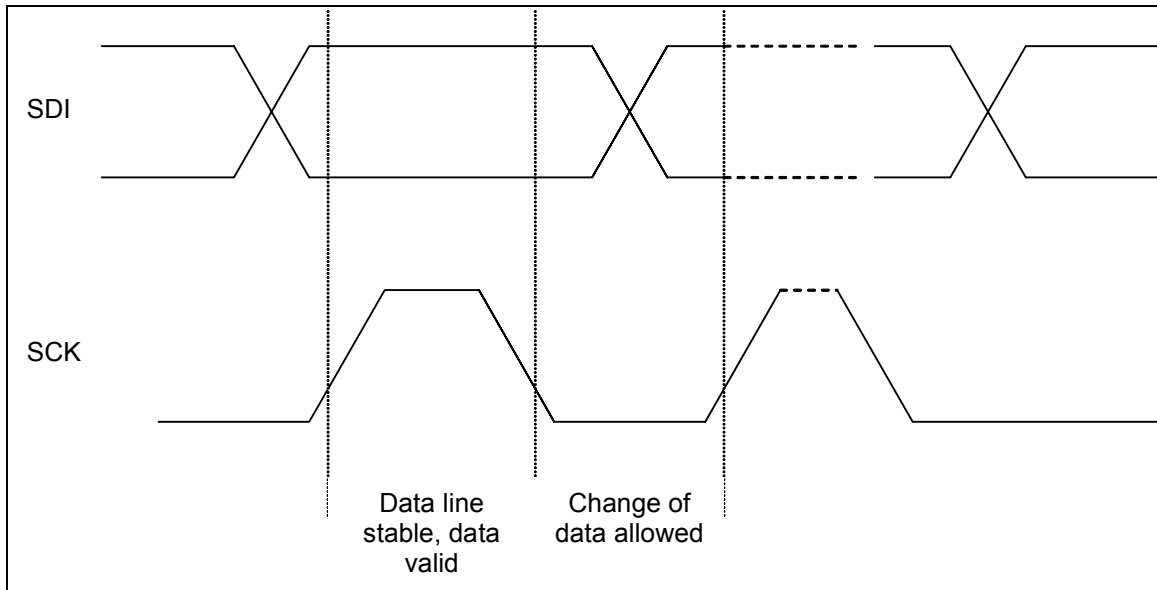
**Figure 12:** Timing diagram for I<sup>2</sup>C start and stop condition (SDI=SDA)



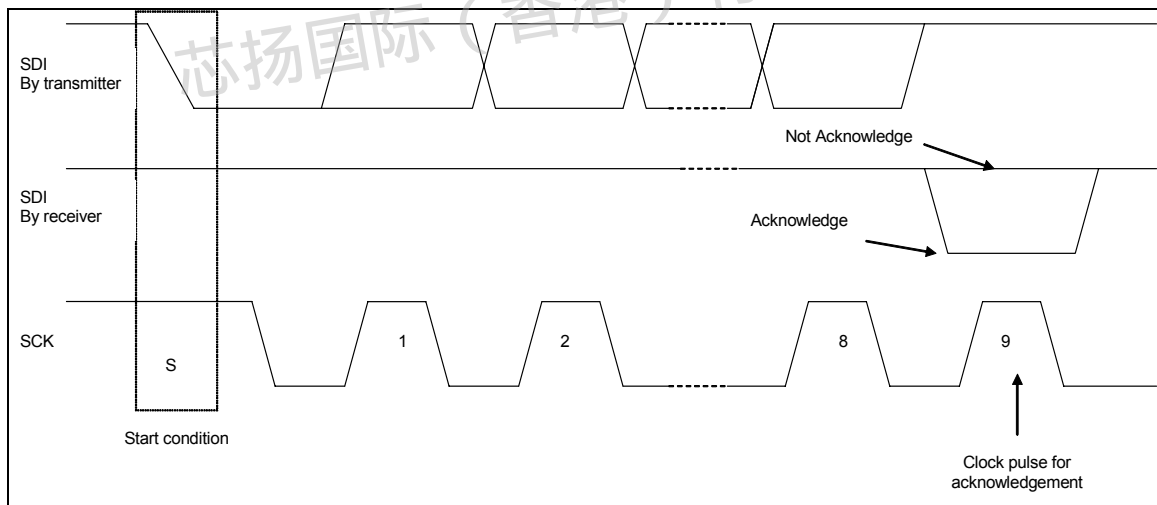



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**Figure 13:** Timing diagram for one bit transfer with I<sup>2</sup>C interface (SDI=SDA)



**Figure 14:** Timing diagram for I<sup>2</sup>C acknowledgement on SDI (SDI=SDA)



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### 4.2.1 I<sup>2</sup>C protocol:

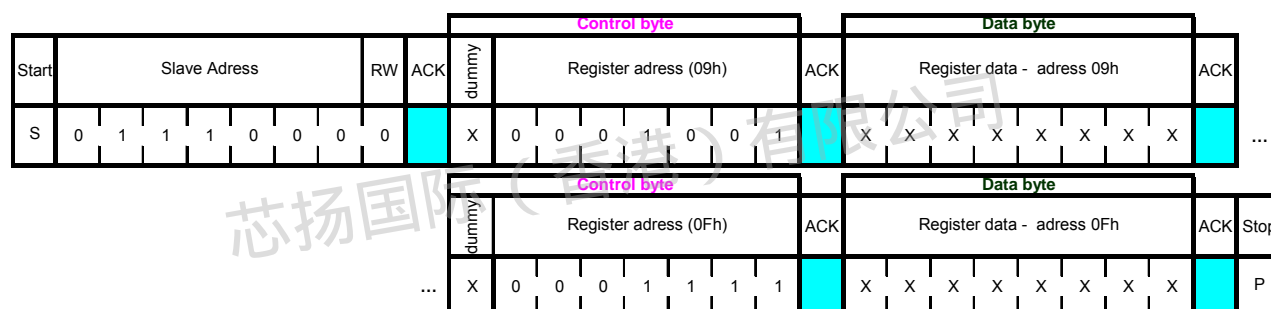
The BMA023 I<sup>2</sup>C slave address is coded on 7 bits (0111000b=38h) fixed by a metal option. Thus I<sup>2</sup>C write address is 01110000b (=70h), read address is 01110001b (=71h).


After a start condition, the slave address + RW bit must be send. If the slave address does not match with BMA023 there is no acknowledgement and the following data transfer will not affect the chip. If the slave address corresponds to BMA023 it will acknowledge (pull SDA down during 9th clock pulse) and data transfer is enabled. The 8th bit RW sets the chip in read or write mode, RW=1 for reading, RW=0 for writing.

After slave address and RW bit, the master sends 1 control byte: the 7-bit register address and one dummy bit.

When BMA023 is accessed in write mode, sequences of 2 bytes (= 1 control byte to define which address will be written and 1 data byte) must be sent:

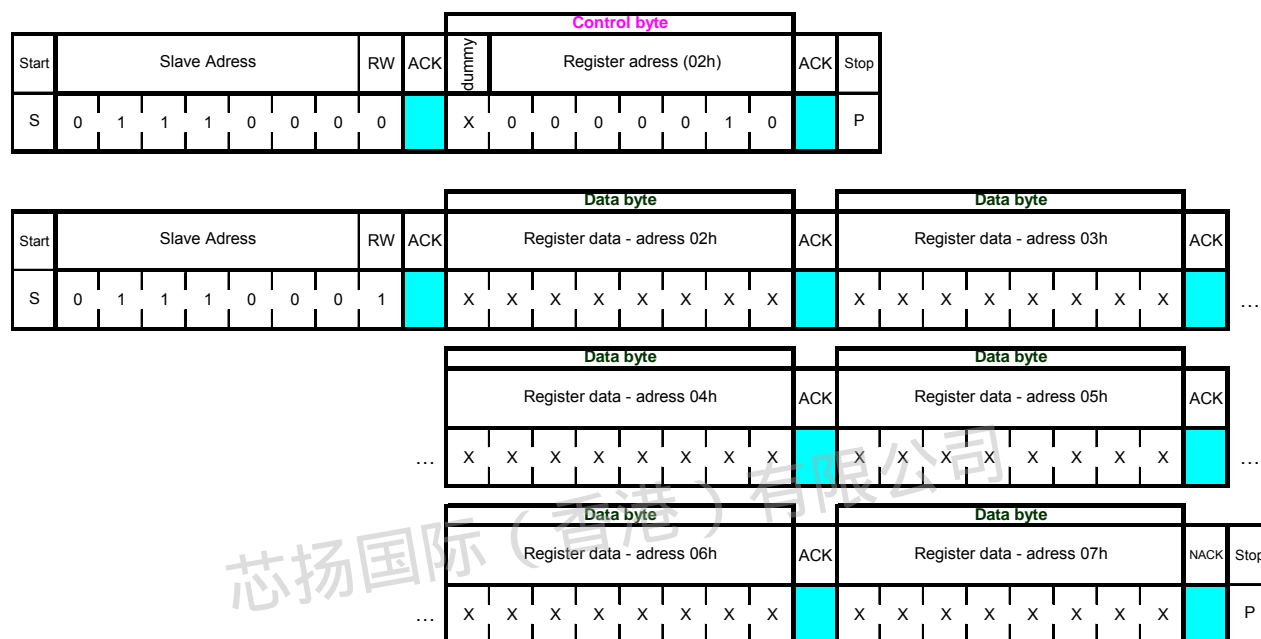
Figure 15: I<sup>2</sup>C multiple write protocol




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To be able to access registers in read mode, first address has to be send in write mode. Then a stop and a start conditions are issued and data bytes are transferred with automatic address increment:

**Figure 16:** I<sup>2</sup>C multiple read protocol. Address register is first written to BMA023, the RW=0 (lowest acceleration data located at address 02h). I<sup>2</sup>C transfer is stopped and restarted with RW=1, address is automatically incremented and the 6 bytes can be sequentially read out.



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## 5. Package

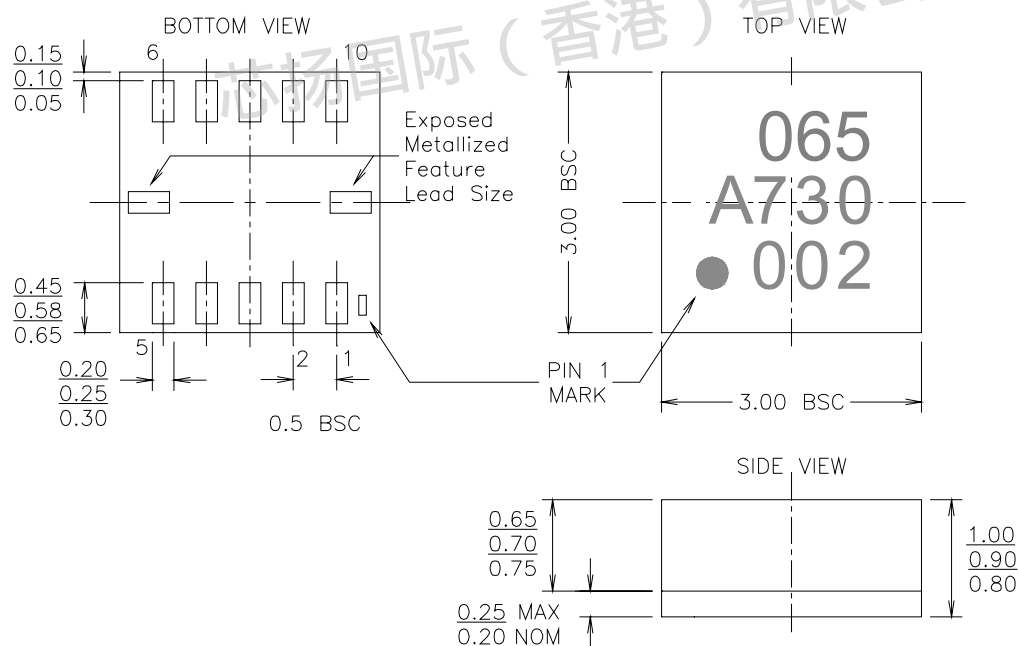
### 5.1 Outline dimensions


The BMA023 is packaged in a 3mm x 3mm x 0.9mm LGA package following JEDEC MO-229.

Basic outline geometry is based on:

- Mold package footprint      3mm x 3mm (tolerance  $\pm 0.1\text{mm}$ )
- Height                            0.9mm
- No. of leads                    12
  - 8 used for electrical connection
  - 2 not used / reserved
  - 2 additional metal features on front edges without electrical functionality (not available on first engineering samples)
- Lead pitch                      0.5mm

**Figure 17: Top, bottom and side views of the 3mm x 3mm x 0.9mm LGA package outline drawing (dimensions in mm)**

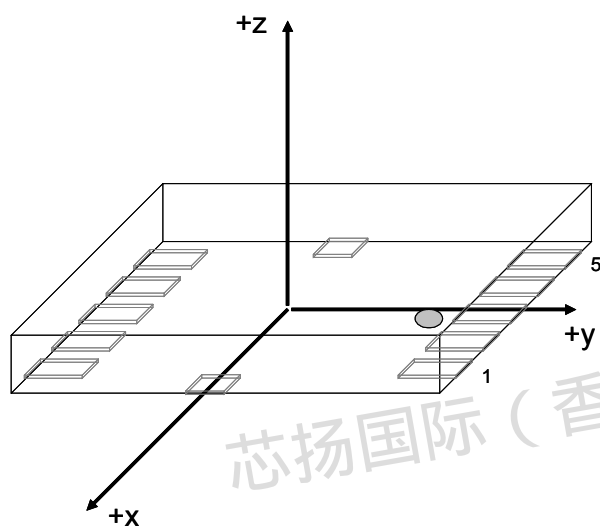



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|  <b>BOSCH</b> | <p style="text-align: center;">Data sheet<br/><b>BMA023</b><br/>Digital, triaxial acceleration sensor</p> | <p style="text-align: center;">Bosch Sensortec</p> |
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## 5.2 Axes orientation

The following diagram describes the orientation of the package with respect to the axes of acceleration measurement.

**Figure 18:** Axes orientation of the BMA023

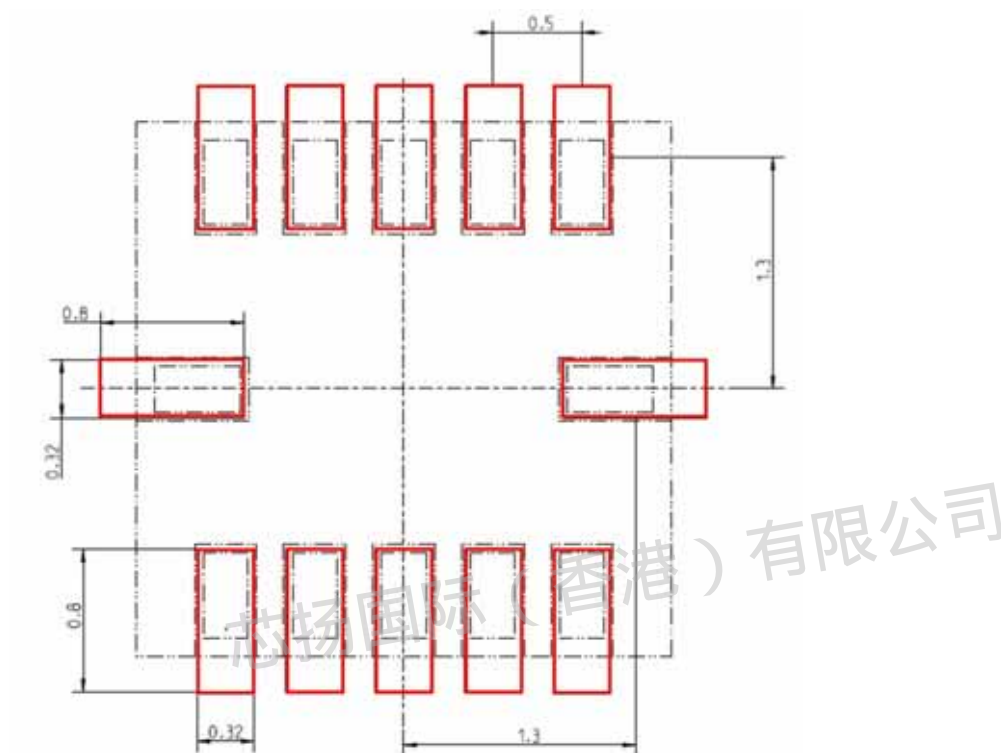


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|  <b>BOSCH</b> | <p style="text-align: center;">Data sheet<br/><b>BMA023</b><br/>Digital, triaxial acceleration sensor</p> | <p style="text-align: center;">Bosch Sensortec</p> |
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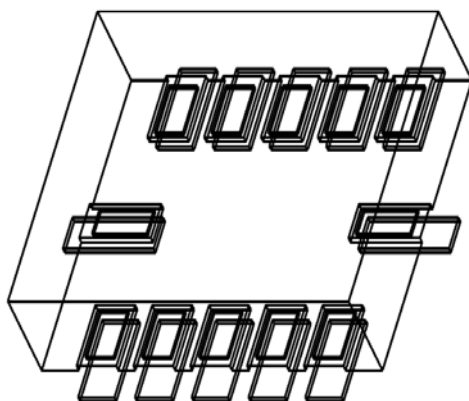
### 5.3 Landing pattern recommendations


As for the design of the landing patterns, the following recommendations can be given:

**Figure 19:** Landing patterns for the BMA023 relative to the device pins, dimensions are in mm



**Figure 20:** Perspective view of the BMA023 relative to the PCB landing pattern.



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#### 5.4 Moisture sensitivity level and soldering

The moisture sensitivity level (MSL) of the BMA023 sensor IC corresponds to JEDEC Level 1, see also

- IPC/JEDEC J-STD-020C "Joint Industry Standard: Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices"
- IPC/JEDEC J-STD-033A "Joint Industry Standard: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices".

The sensor IC fulfils the lead-free soldering requirements of the above-mentioned IPC/JEDEC standard, i.e. reflow soldering with a peak temperature up to 260°C.

#### 5.5 RoHS compliancy

The BMA023 sensor IC meets the requirements of the EC restriction of hazardous substances (RoHS) directive, see also "Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment".

#### 5.6 Halogen content

Results of chemical analysis show that the BMA023 contains less than 900ppm (by weight) of Fluorine, Chlorine, Iodine and Bromine (i.e. <900ppm per each substance).

Therefore the BMA023 can be regarded as halogen-free.


For more details on the analysis results please contact your Bosch Sensortec representative.

#### 5.7 Note on internal package structure

Within the scope of Bosch Sensortec's ambition to improve its products and secure the product supply while in mass production, Bosch Sensortec qualifies additional sources for the LGA package of the BMA023.

While Bosch Sensortec took care that all of the technical package parameters as described above are 100% identical for both sources, there can be differences in the chemical analysis and internal structural between the different package sources.

However, as secured by the extensive product qualification processes of Bosch Sensortec, this has no impact to the usage or to the quality of the BMA023 product.

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## 6. Pin-out out and connection diagrams

Figure 21: Pin-out of the BMA023 (bottom view);

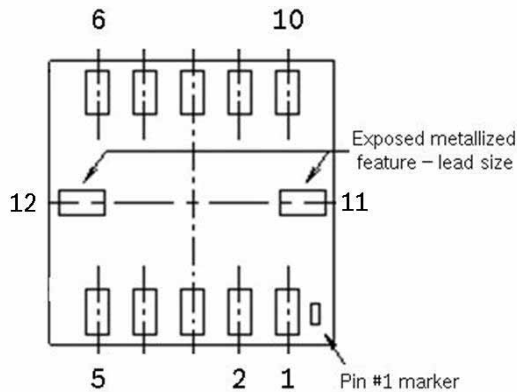


Table 12: Pin-out description of the BMA023

| Pin No | Name              | Type           | Description                    | Connect to (in SPI 4w) | Connect to (in SPI 3w) | Connect to (in I <sup>2</sup> C) | Stand alone (without $\mu$ C) |
|--------|-------------------|----------------|--------------------------------|------------------------|------------------------|----------------------------------|-------------------------------|
| 1      | reserved          |                | Do not connect                 | NC                     | NC                     | NC                               | NC                            |
| 2      | V <sub>DD</sub>   | Power          | Analogue power supply          | V <sub>DD</sub>        | V <sub>DD</sub>        | V <sub>DD</sub>                  | V <sub>DD</sub>               |
| 3      | GND               | Power          | Ground                         | GND                    | GND                    | GND                              | GND                           |
| 4      | INT               | Output         | Interrupt                      | INT / NC               | INT / NC               | INT / NC                         | INT                           |
| 5      | CSB               | Input          | Chip select                    | CSB                    | CSB                    | V <sub>DDIO</sub>                | V <sub>DD</sub>               |
| 6      | SCK               | Input          | Serial clock                   | SCK                    | SCK                    | SCK                              | GND                           |
| 7      | SDO               | Output         | Serial data out                | SDO                    | GND                    | GND                              | GND                           |
| 8      | SDI               | Input / Output | Serial data in / out           | SDI                    | SDA                    | SDA                              | GND                           |
| 9      | V <sub>DDIO</sub> | Power          | Digital interface power supply | V <sub>DDIO</sub>      | V <sub>DDIO</sub>      | V <sub>DDIO</sub>                | V <sub>DD</sub>               |
| 10     | reserved          |                | Do not connect                 | NC                     | NC                     | NC                               | NC                            |
| 11     | reserved          |                | Do not connect                 | NC                     | NC                     | NC                               | NC                            |
| 12     | reserved          |                | Do not connect                 | NC                     | NC                     | NC                               | NC                            |

Recommendation for decoupling: between GND and V<sub>DD</sub> (pin 1 or 2) a 22nF capacitor and between GND and IOVDD (pin 9) a 100nF capacitor should be connected.




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Figure 22: Connection diagram for use with 4-wire SPI interface

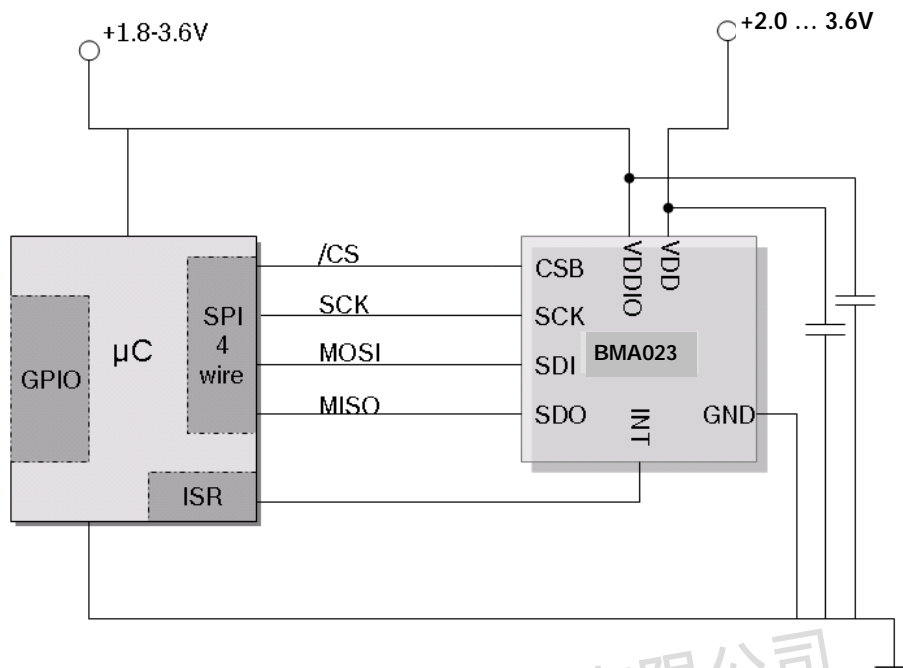
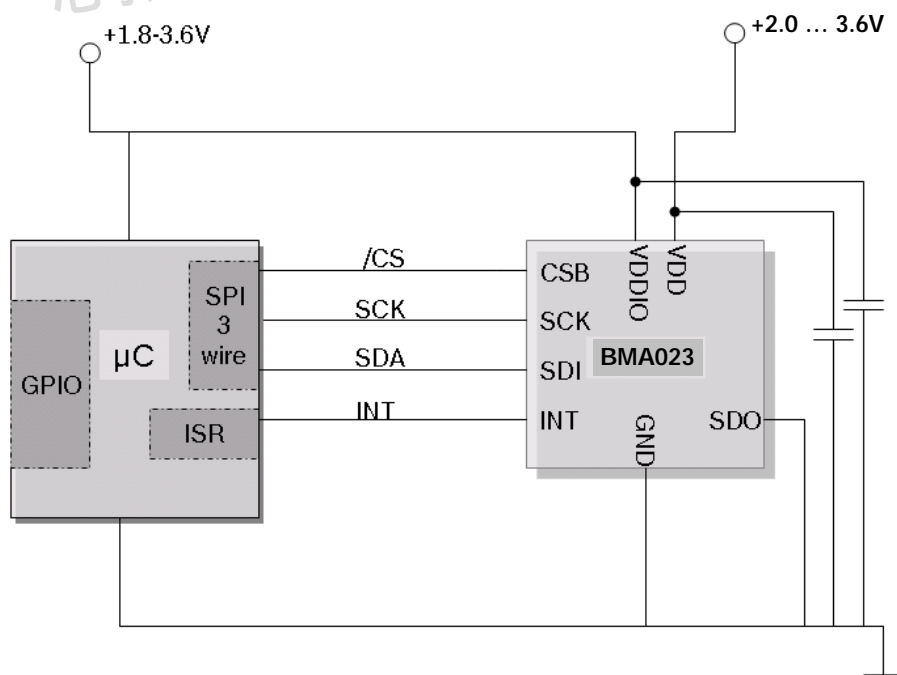

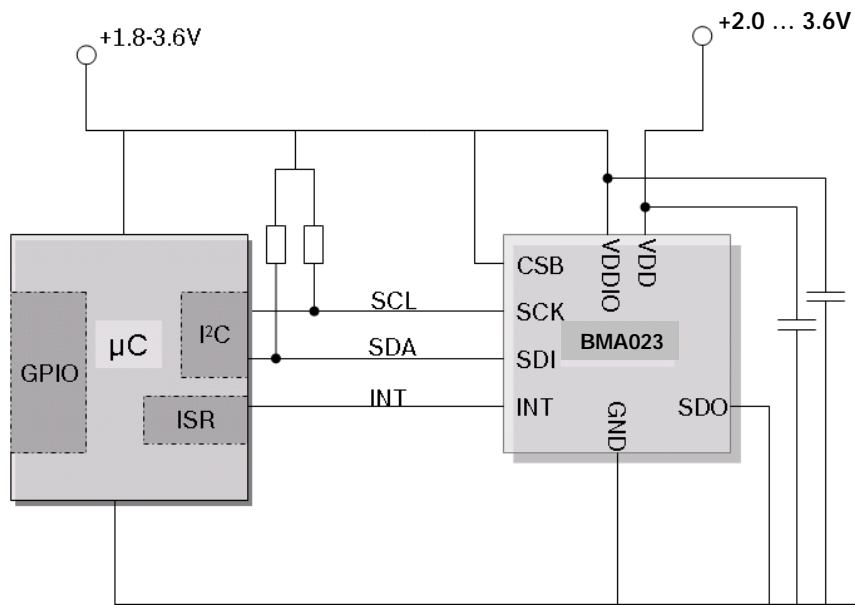


Figure 23: Connection diagram for use with 3-wire SPI interface




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**Figure 24:** Connection diagram for use with I<sup>2</sup>C interface



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## 7. Operation modes

### 7.1 Normal operational mode

In normal operational mode the sensor IC can be addressed via digital interface. Data and status registers can be read out and control registers can be read and changed. In parallel to normal operation the user has the option to activate several internal logic paths and set criteria to trigger the interrupt pin. BMA023 is designed to enable low current consumption of 200 $\mu$ A in operational mode.

A self-test procedure can be started in operational mode for testing of the complete signal evaluation path including the micro-machined sensor IC structure, the evaluation ASIC and the physical connection to the host system.

### 7.2 Sleep mode

Sleep mode is activated by setting a control bit. In sleep mode no communication with the sensor IC is possible – all read and write commands are forbidden. The recommended command to switch to operational mode is the wake-up call.

Wake-up time from sleep to operational mode is 1ms.

In case of a soft-reset, it is recommended to do this reset after having switched from sleep to operational mode. In this case the total typical wake-up and reset time at maximum bandwidth is "switching to operational mode = 1ms" and "time after soft reset until acceleration data is available = 1.3ms", i.e. 2.3ms in total.

In case a soft-reset is activated during sleep mode it can take up to 30msec. until normal operation has resumed.


The current consumption in sleep mode is 1 $\mu$ A.

### 7.3 Wake-up mode

In general BMA023 is attributed to low power applications and can contribute to the system power management.

- Current consumption 200 $\mu$ A operational
- Current consumption 1 $\mu$ A sleep mode
- Wake-up time 1ms
- Start-up time 3ms
- Data ready indicator to reduce unnecessary interface communication
- Wake-up mode to trigger a system wake-up (interrupt output to master) when motion detected
- Current consumption in wake-up mode

The BMA023 provides the possibility to wake up a system master when specific acceleration values are detected. Therefore the BMA023 stays in an ultra low power mode and periodically evaluates the acceleration data with respect to interrupt criteria defined by the user. An interrupt

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output can be generated and trigger the system master. The wake-up mode is used for ultra-low power applications where inertial factors can be an indicator to change the activity mode of the system.

The following table shows values calculated for the average current consumption during the wake-up mode of the BMA023. The power consumption in wake-up mode is dependent on the duration of the interrupt algorithm (number of data acquisitions) and the bandwidth (for more details on setting of the bandwidth please refer to chapter 3.1.3).

Table 13: Average current consumption in self wake-up mode using high-g or low-g interrupt

| <b>Current consumption during BMA023 wake-up mode [μA]</b><br>(depending on bandwidth, calculated using typical values) |             |           |          |          |          |         |         |
|---|-------------|-----------|----------|----------|----------|---------|---------|
| <b>Pause [ms]</b>   | (@ 1,500Hz) | (@ 750Hz) | (@375Hz) | (@190Hz) | (@100Hz) | (@50Hz) | (@25Hz) |
| <b>20</b>   | 16.3        | 21,8      | 31.8     | 48.4     | 71.6     | 102.9   | 134.7   |
| <b>80</b>   | 5.1         | 6.6       | 9.7      | 15.4     | 25.0     | 42.3    | 68.4    |
| <b>360</b>  | 1.9         | 2.3       | 3.0      | 4.4      | 6.9      | 12.0    | 21.3    |
| <b>2,560</b>  | 1.1         | 1.2       | 1.3      | 1.5      | 1.9      | 2.6     | 4.1     |

Durations of the pause values can vary for about ±30% due to the accuracy of the ultra-low-power oscillator implemented within the sensor.

For estimating the typical current consumption in wake-up mode the following formula can be applied:


$$i_{self\_wake\_up} = (i_{DD} \cdot t_{active} + i_{DDsm} \cdot wake\_up\_pause) / (t_{active} + wake\_up\_pause)$$

With the approximation:

$$t_{active} = 1ms + 0.333ms \cdot (4 \cdot 750 / bandwidth) + 0.333ms \cdot (1500 / bandwidth) \cdot n$$

With the following parameters:

|               |  |
|---------------|--|
| $i_{DD}$      | Current in normal mode   |
| $i_{DDsm}$    | Current in sleep mode  |
| wake_up_pause | Setting of wake-up pause   |
| n             | number of data points in any-motion logic<br>(n=0 for high-g threshold and low-g threshold interrupt,<br>n=3 for any-motion logic) |
| Bandwidth     | Setting of bandwidth (750-25 Hz),<br>for 1500Hz $t_{active} = 1ms + 0.333ms \cdot (1500/bandwidth) \cdot n$                        |

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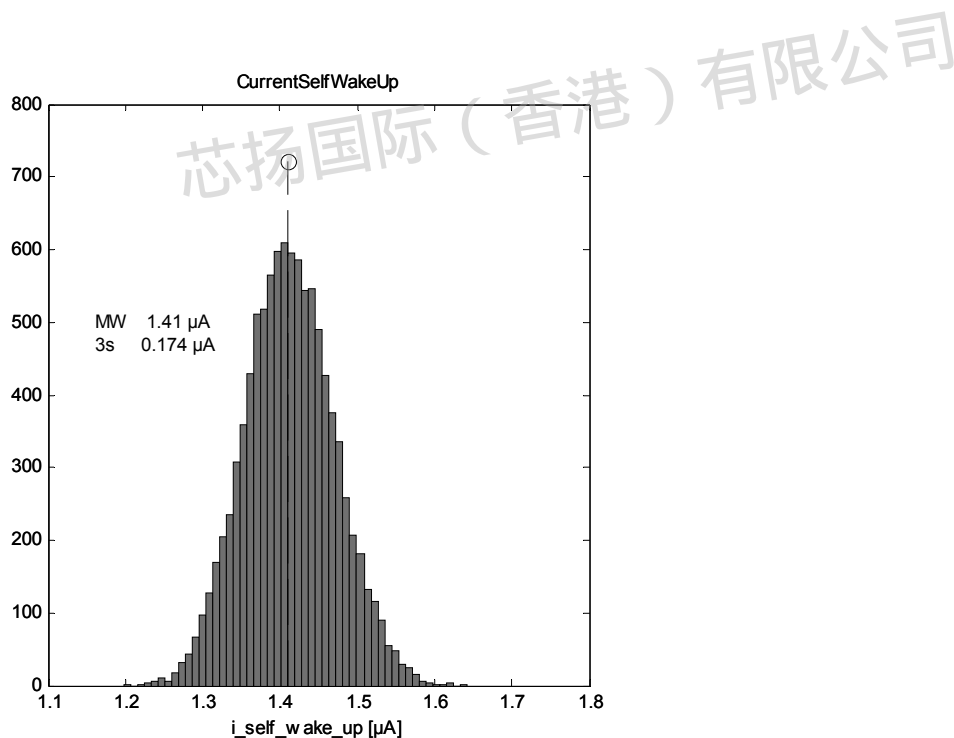
So, the relevant parameters for power consumption in self-wake up mode are:


- the current consumption in normal mode
- the current consumption in sleep mode
- the self-wake up pause duration
- the bandwidth (ie. length of digital filter to be filled for one data point)
- the interrupt criteria (determines the duration of normal operation):
  - high-g and low-g criteria (ie. acquisition of one data point)
  - any-motion criterion (ie. four data points)

As some of these parameters have certain deviations from the typical value results of various example Monte Carlo Simulations on the current consumption are shown in figures 25, 26 and 27.

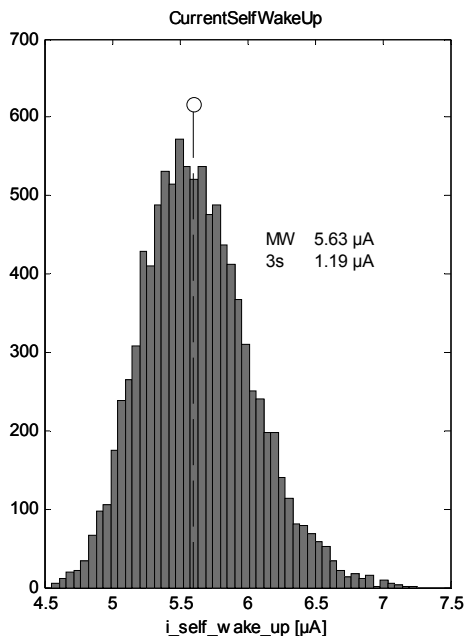
The graphs provide an indication on the expected current consumption for different settings.

**Figure 25:** Estimation of current consumption using Monte Carlo simulation, example #1: bandwidth 750Hz, 2560ms wake-up setting, any-motion interrupt

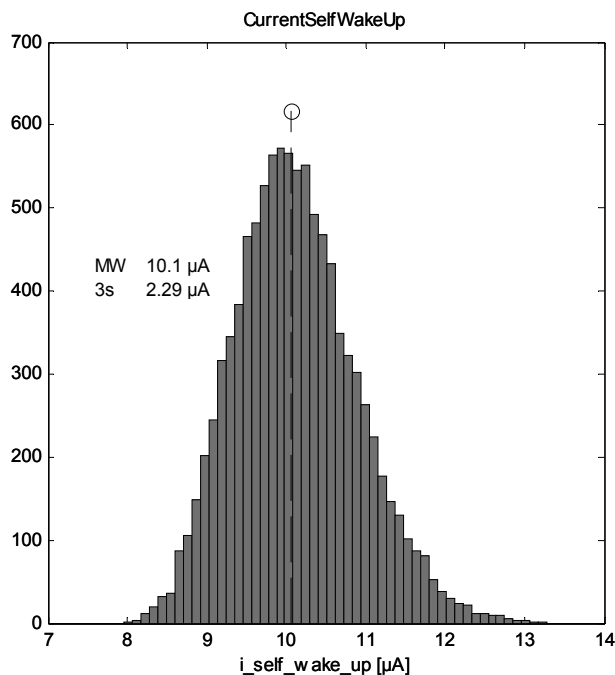



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**Figure 26:** Estimation of current consumption using Monte Carlo simulation, example #2: bandwidth 47Hz, 2560ms wake-up setting, any-motion interrupt



**Figure 27:** Estimation of current consumption using Monte Carlo simulation, example #3: Bandwidth 23Hz, 2560ms wake-up setting, any-motion interrupt



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## 8. Data conversion

### 8.1 Acceleration data

Acceleration data are converted by a 10bit ADC. The description of the digital signal is "2's complement". The 10 bit data are available as LSB (at lower register address) and MSB. It is possible to read out MSB only (8 bit) and LSB/MSB (16 bits with 10 data bits and 1 data ready bit) while LSB- and MSB-data are closely linked to avoid unintentional LSB/MSB mixing when read out and data conversion overlap accidentally (section 3.5.1).

The update rate of data registers is 3 kHz, independent of the digital filter. The acceleration data is filtered by a second order analog filter at 1.5 kHz. Additionally the data can be processed by digital averaging filters (moving average) to reduce the noise level (750Hz – 25Hz).


The transfer function of the mechanical element is designed to avoid resonance effects at frequencies below the bandwidth of the ASIC.

The availability of new data can be checked in two ways:

- Bit 0 from the LSB data registers is an indicator whether the data have already been read out or the data are new (Bit0=1) (section 3.5.2).
- The interrupt pin can be configured to indicate new data availability (not possible in parallel to internal interrupt logic). The synchronization of data acquisition and data read out enables the customer to avoid unnecessary interface traffic in order to reduce the system power consumption and the crosstalk between interface communication and data conversion. For a detailed explanation see Figure 3. (section 3.2.10)

**Figure 28:** Explanation of data ready interrupt: For a bandwidth of e.g. 1.5kHz the data refresh cycle takes 330µs to update all data registers. After the final conversion of z-axis the INT pad will be set high. New data can be read out via interface. The interrupt resets automatically after read out.



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## 9. Internal logic functions

The sensor IC can inform the host system about specific conditions (e.g. new data ready flag or acceleration thresholds passed) by setting an interrupt pin high even if interface communication is not taking place. This feature can be used as “wake-up” indicator or “data ready flag” for instance.

The interrupt performance can be programmed by means of control bits. Thus the criteria to identify a special event can be tailored to a customer’s application and the sensor IC output can be defined specifically.

### 9.1 High-g logic

For indicating high-g events an upper threshold can be programmed. This logic can also be activated by a control bit. Threshold, duration and reset behaviour can be programmed. See also section 3.2.8.

### 9.2 Any motion detection

The “any motion algorithm” can be used to detect changes of the acceleration. Thus it provides a relative evaluation of the acceleration signals. The criterion is kind of a gradient threshold of the acceleration over time. Thus one can distinguish between fast events with strong inertial dynamic (e.g. shock), instant changes of force balance (e.g. drop, tumbling) and even slight changes (e.g. touch of a mobile device).

Due to a high bandwidth and a fast response MEMS device the BMA023 is capable to detect shock situations. The “any motion interrupt” or a high-g criterion setting can be used to give a shock alert. The phase shift between onset of mechanical shock and interrupt output is defined by the mechanical transfer function of the chassis and internal mounting interfaces (e.g. PDA shell) and the data output rate of the sensor IC (currently 330 $\mu$ s, 100 $\mu$ s under consideration).


See also section 3.2.9.

### 9.3 Alert mode

Using the BMA023 it is possible to combine the “any motion criterion” with low-g and high-g interrupt logic to improve the reaction time.

See also sections 3.2.9 and 3.4.2.



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## 10. Legal disclaimer

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## 11. Document history and modification

| Rev. No | Chapter | Description of modification/changes | Date        |
|---------|---------|-------------------------------------|-------------|
| 1.0     |         | Document creation                   | 23-Feb-2009 |
| 1.1     | 1       | Added comment on 3-sigma values     | 07-Apr-2009 |

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