

FNK N-Channel Enhancement Mode Power MOSFET

Description

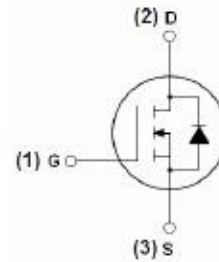
The FNK1520 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- $V_{DS} = 150V, I_D = 20A$
 $R_{DS(ON)} < 85m\Omega$ @ $V_{GS} = 10V$ (Typ: $78m\Omega$)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Boost converters
- LED backlighting
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



TO-220-3L top view

Package Marking and Ordering Information

| Device Marking | Device | Device Package | Reel Size | Tape width | Quantity |
|----------------|---------|----------------|-----------|------------|----------|
| FNK1520 | FNK1520 | TO-220-3L | - | - | - |

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

| Symbol | Parameter | Limit | Unit |
|--------------------|--|------------|---------------|
| V_{DS} | Drain-Source Voltage | 150 | V |
| V_{GS} | Gate-Source Voltage | ± 20 | V |
| I_D | Drain Current-Continuous | 20 | A |
| $I_D(100^\circ C)$ | Drain Current-Continuous($T_C = 100^\circ C$) | 14 | A |
| I_{DM} | Pulsed Drain Current | 40 | A |
| P_D | Maximum Power Dissipation | 75 | W |
| | Derating factor | 0.5 | W/ $^\circ C$ |
| E_{AS} | Single pulse avalanche energy (Note 5) | 200 | mJ |
| T_J, T_{STG} | Operating Junction and Storage Temperature Range | -55 To 175 | $^\circ C$ |

Thermal Characteristic

| | | | |
|-----------------|---|-----|---------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case (Note 2) | 2.0 | $^{\circ}C/W$ |
|-----------------|---|-----|---------------|

Electrical Characteristics ($T_c=25^{\circ}C$ unless otherwise noted)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|------------------------------------|----------------------------------|--|-----|------|------|------|
| Off Characteristics | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | V _{GS} =0V I _D =250μA | 150 | 160 | - | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =150V, V _{GS} =0V | - | - | 1 | μA |
| I _{GSS} | Gate-Body Leakage Current | V _{GS} =±20V, V _{DS} =0V | - | - | ±100 | nA |
| On Characteristics (Note 3) | | | | | | |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} , I _D =250μA | 2 | 3 | 4 | V |
| R _{DS(ON)} | Drain-Source On-State Resistance | V _{GS} =10V, I _D =10A | - | 78 | 85 | mΩ |
| g _{FS} | Forward Transconductance | V _{DS} =5V, I _D =10A | - | 20 | - | S |
| Dynamic Characteristics (Note4) | | | | | | |
| C _{iss} | Input Capacitance | V _{DS} =25V, V _{GS} =0V, F=1.0MHz | - | 2000 | - | PF |
| C _{oss} | Output Capacitance | | - | 290 | - | PF |
| C _{rss} | Reverse Transfer Capacitance | | - | 180 | - | PF |
| Switching Characteristics (Note 4) | | | | | | |
| t _{d(on)} | Turn-on Delay Time | V _{DD} =75V, R _L =5Ω V _{GS} =10V, R _{GEN} =3Ω | - | 10.5 | - | nS |
| t _r | Turn-on Rise Time | | - | 5.5 | - | nS |
| t _{d(off)} | Turn-Off Delay Time | | - | 14.5 | - | nS |
| t _f | Turn-Off Fall Time | | - | 3 | - | nS |
| Q _g | Total Gate Charge | V _{DS} =75V, I _D =10A, V _{GS} =10V | - | 17 | - | nC |
| Q _{gs} | Gate-Source Charge | | - | 4 | - | nC |
| Q _{gd} | Gate-Drain Charge | | - | 4.4 | - | nC |
| Drain-Source Diode Characteristics | | | | | | |
| V _{SD} | Diode Forward Voltage (Note 3) | V _{GS} =0V, I _S =20A | - | - | 1.2 | V |
| I _S | Diode Forward Current (Note 2) | - | - | - | 20 | A |
| t _{rr} | Reverse Recovery Time | T _J = 25°C, I _F = 10A | - | 32 | - | nS |
| Q _{rr} | Reverse Recovery Charge | di/dt = 100A/μs(Note3) | - | 53 | - | nC |
| t _{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

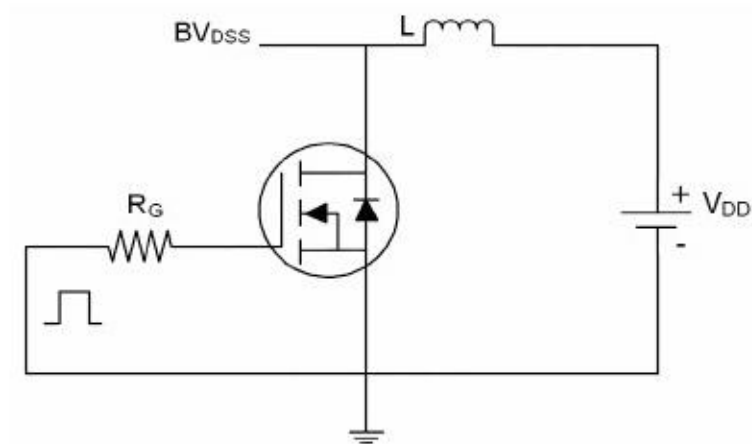
Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

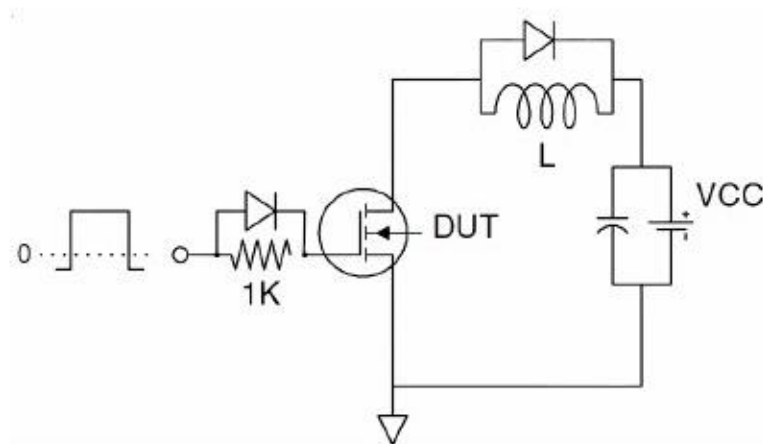
5. EAS condition: $T_J=25^{\circ}C, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

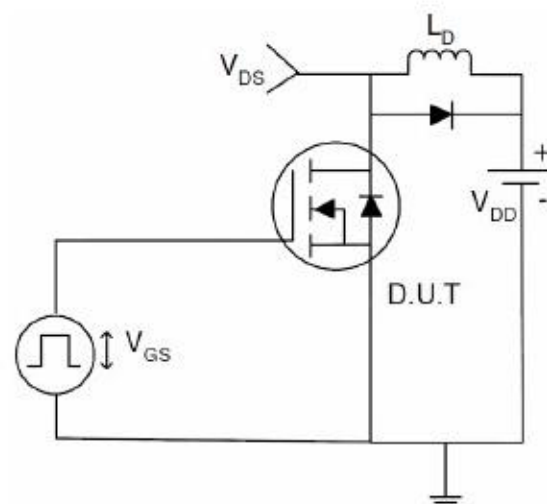
1) Eas Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

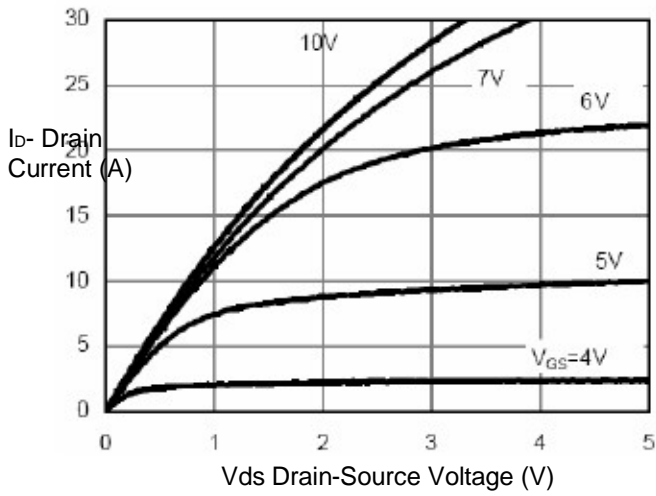


Figure 1 Output Characteristics

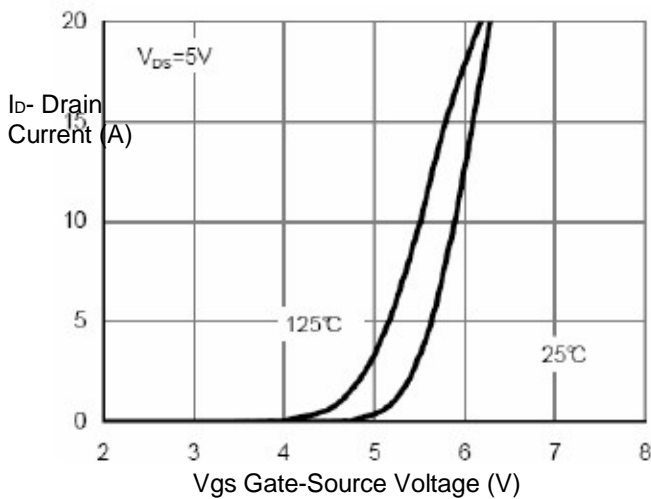


Figure 2 Transfer Characteristics

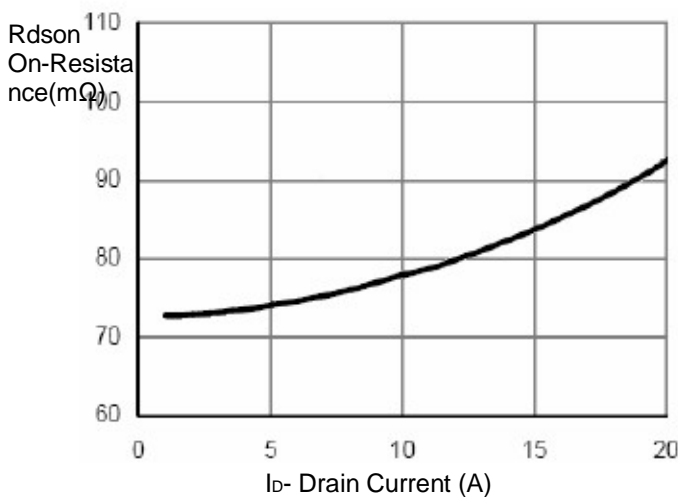


Figure 3 $R_{DS(on)}$ - Drain Current

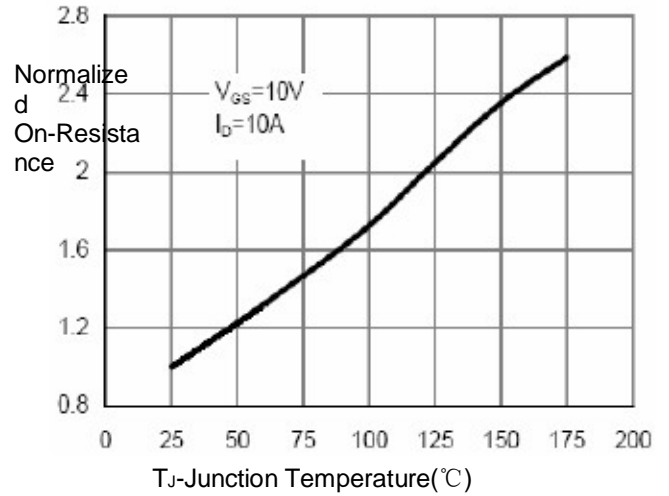


Figure 4 $R_{DS(on)}$ -Junction Temperature

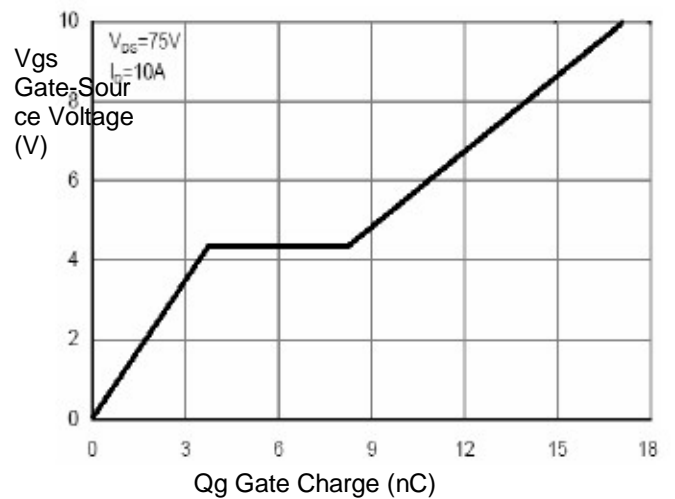


Figure 5 Gate Charge

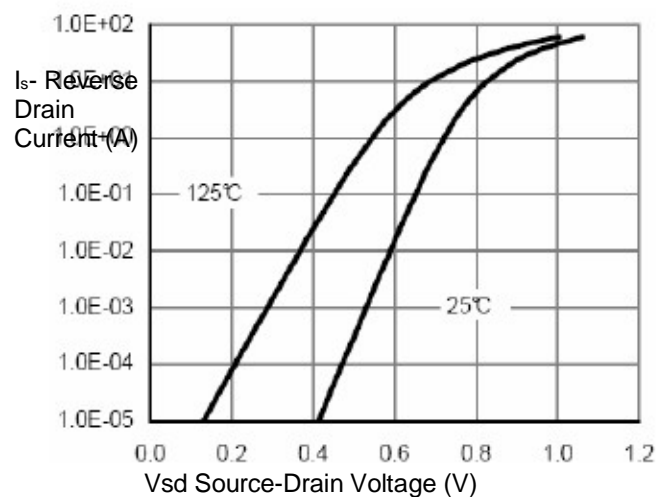


Figure 6 Source- Drain Diode Forward

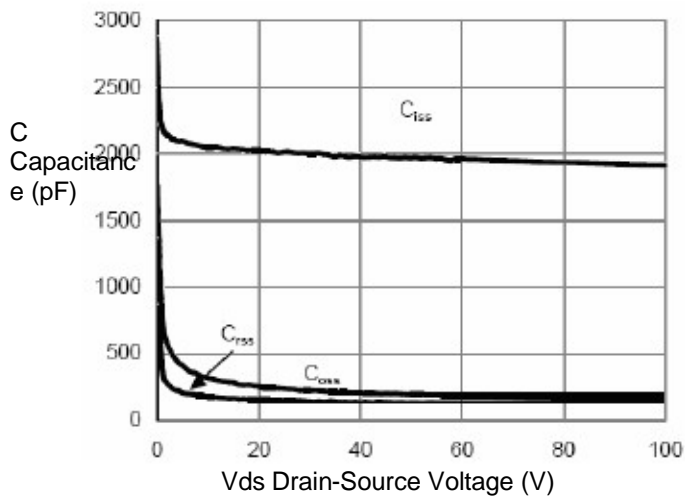


Figure 7 Capacitance vs Vds

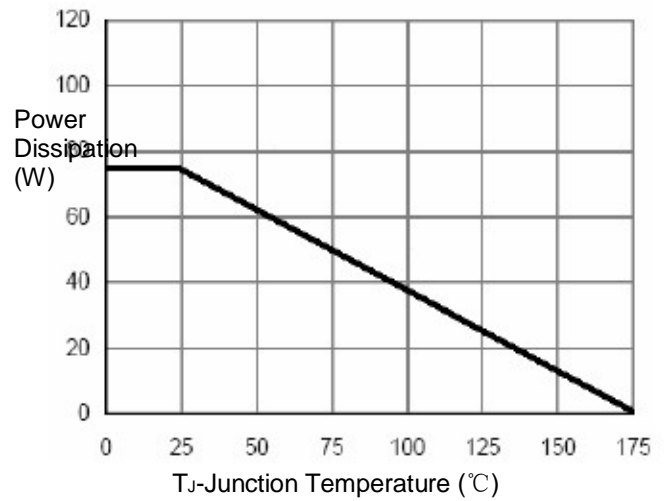


Figure 9 Power De-rating

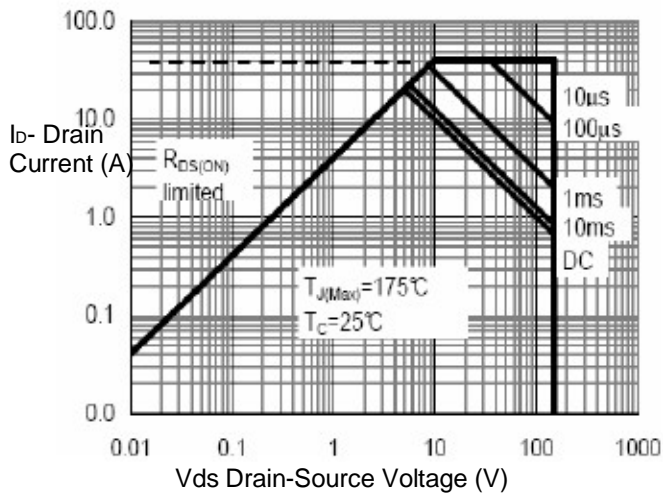


Figure 8 Safe Operation Area

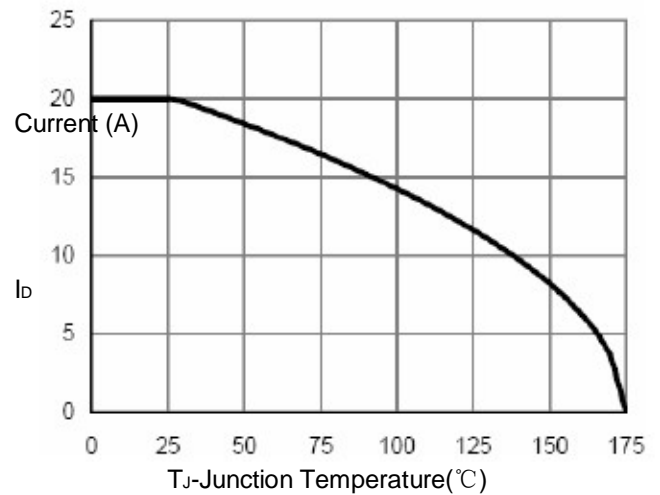


Figure 10 ID Current- Junction Temperature

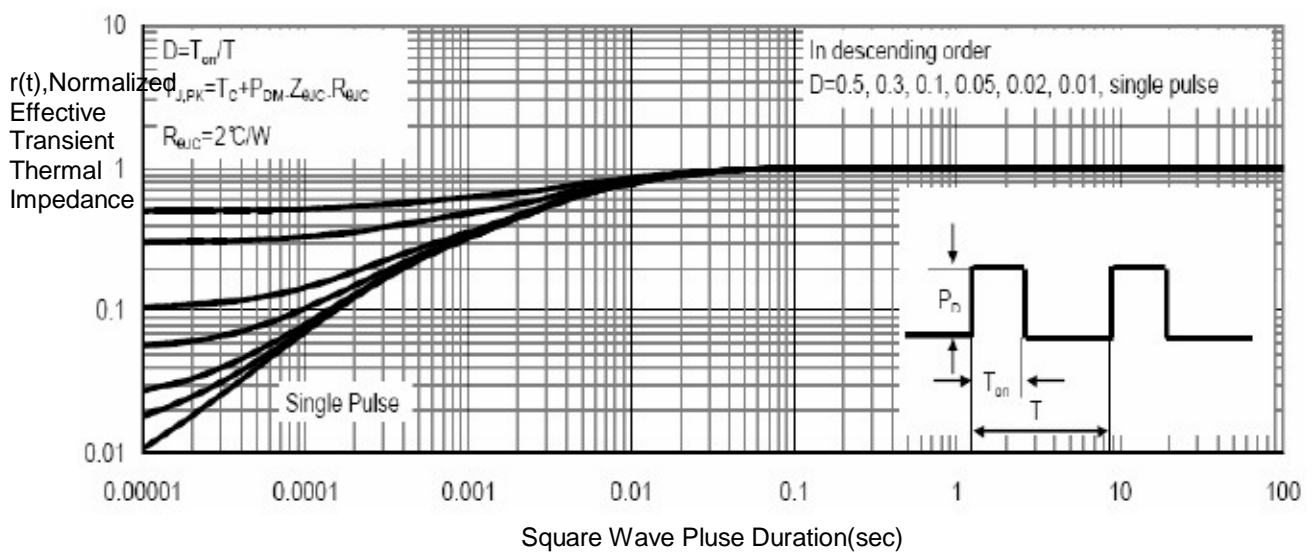
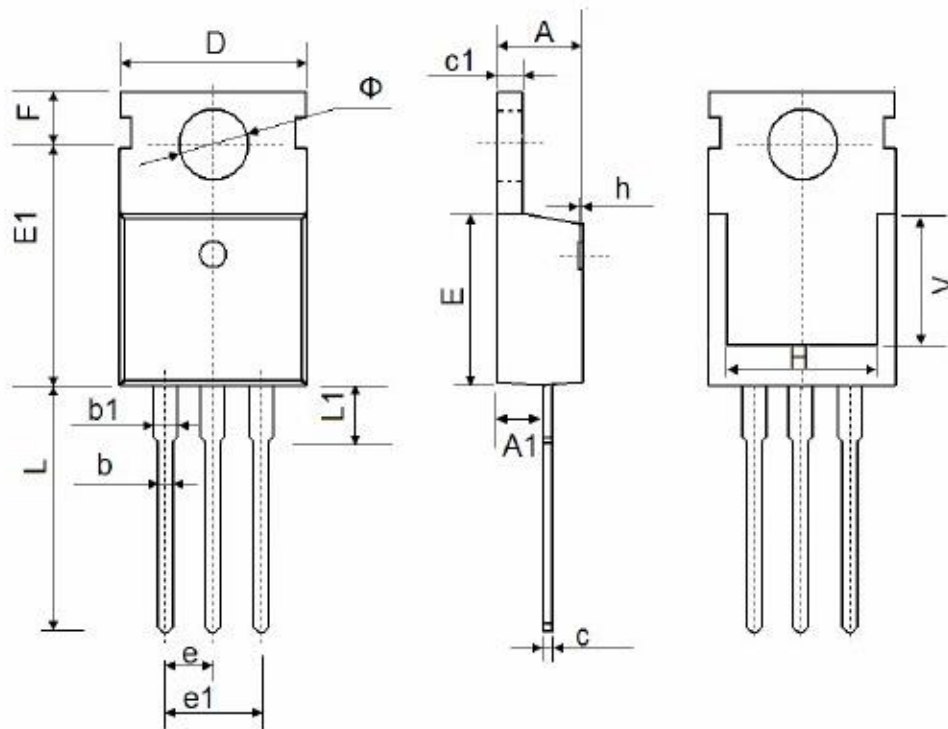


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220-3L Package Information



| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|---------------------------|--------|----------------------|-------|
| | Min. | Max. | Min. | Max. |
| A | 4.400 | 4.600 | 0.173 | 0.181 |
| A1 | 2.250 | 2.550 | 0.089 | 0.100 |
| b | 0.710 | 0.910 | 0.028 | 0.036 |
| b1 | 1.170 | 1.370 | 0.046 | 0.054 |
| c | 0.330 | 0.650 | 0.013 | 0.026 |
| c1 | 1.200 | 1.400 | 0.047 | 0.055 |
| D | 9.910 | 10.250 | 0.390 | 0.404 |
| E | 8.9500 | 9.750 | 0.352 | 0.384 |
| E1 | 12.650 | 12.950 | 0.498 | 0.510 |
| e | 2.540 TYP. | | 0.100 TYP. | |
| e1 | 4.980 | 5.180 | 0.196 | 0.204 |
| F | 2.650 | 2.950 | 0.104 | 0.116 |
| H | 7.900 | 8.100 | 0.311 | 0.319 |
| h | 0.000 | 0.300 | 0.000 | 0.012 |
| L | 12.900 | 13.400 | 0.508 | 0.528 |
| L1 | 2.850 | 3.250 | 0.112 | 0.128 |
| V | 7.500 REF. | | 0.295 REF. | |
| Φ | 3.400 | 3.800 | 0.134 | 0.150 |