

Universal High Brightness LED Driver

General Description

The FP7172 is an open loop, current mode, control LED driver IC. The FP7172 can be programmed to operate in either a constant frequency or constant off-time mode. It includes an 15 - 450V linear regulator which allows it to work from a wide range of input voltages without the need for an external low voltage supply. The FP7172 is ideally suited for buck LED drivers. Since the FP7172 operates in open loop current mode control, the controller achieves good output current regulation without the need for any loop compensation.

The FP7172 is available in the small footprint SOT23-6L package to fit in space-saving PCB layout for miscellaneous application fields.

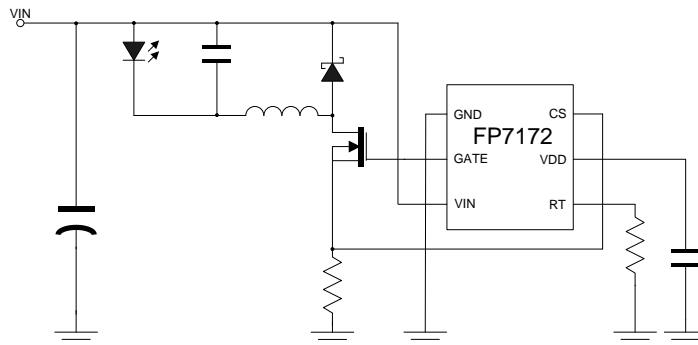
Features

- Switch mode controller for single switch LED drivers
- Enhanced drop-in replacement to the FP7172
- Open loop peak current controller
- Internal 15 to 450V linear regulator
- Constant frequency or constant off-time operation
- Requires few external components for operation

Applications

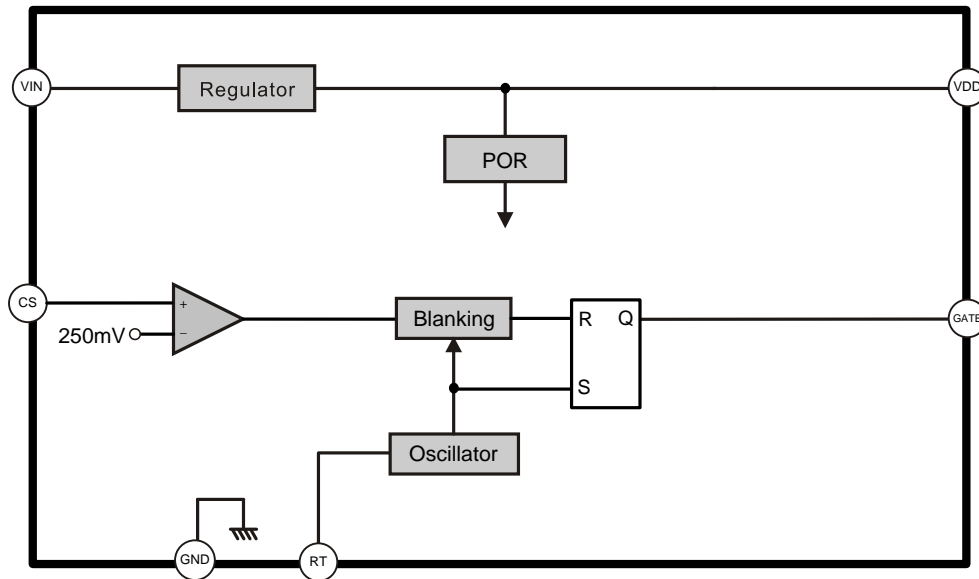
- DC/DC or AC/DC LED driver applications
- RGB backlighting LED driver
- Back lighting of flat panel displays
- General purpose constant current source
- Signage and decorative LED lighting
- Chargers

Typical Application Circuit



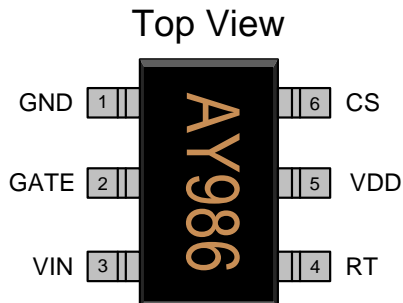
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Function Block Diagram



Pin Descriptions

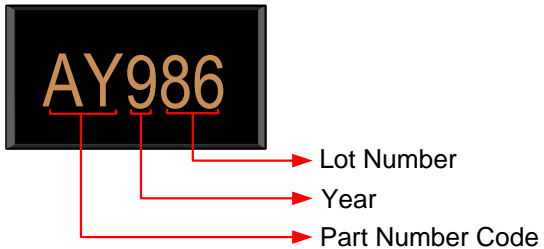
SOT23-6L



Name	No.	I / O	Description
GND	1	P	Ground return for all internal circuitry.
GATE	2	O	This pin is the output GATE driver for an external N-channel power MOSFET.
VIN	3	I	This pin is the input of an 15 - 450V linear regulator
RT	4	I	This pin sets the oscillator frequency. When a resistor is connected between RT and GND, the FP7172 operates in constant frequency mode. When the resistor is connected between RT and GATE, the IC operates in constant off-time mode.
VDD	5	I	This is the power supply pin for all internal circuits.
CS	6	I	This pin is the current sense pin used to sense the FET current by means of an external sense resistor.

Marking Information

SOT23-6L



Lot Number: Wafer lot number's last two digits

For Example: 132386TB → 86

Year: Production year's last digit

Part Number Code: Part number identification code for this product. It should be always "AV".

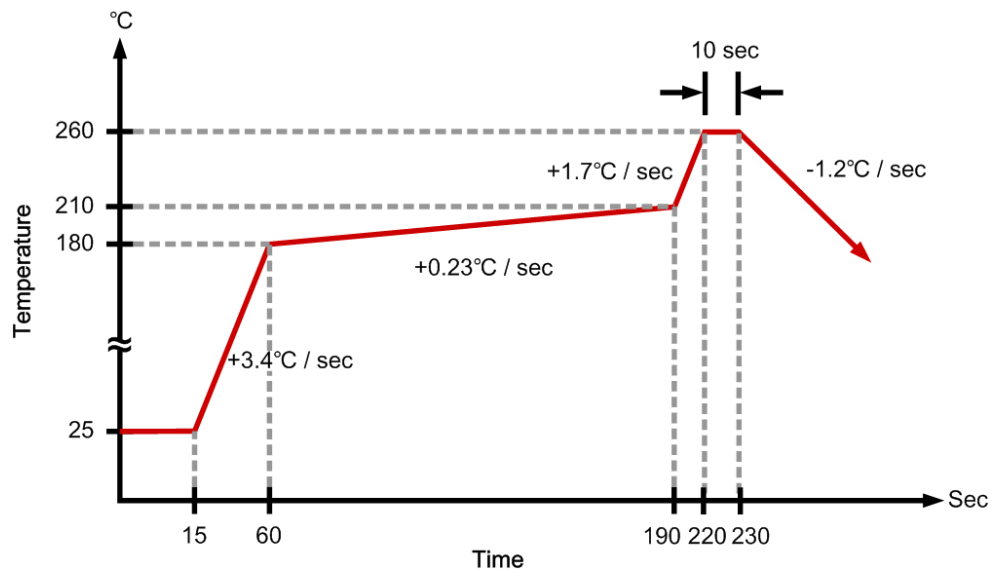
Ordering Information

Part Number	Code	Operating Temperature	Package	MOQ	Description
FP7172LR-G1	AY	-40°C ~ 85°C	SOT23-6L	3000EA	Tape & Reel

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V _{IN}	V _{IN} to GND			470	V
	V _{DD}	V _{DD} to GND			8	V
CS, GATE, RT			-0.3		V _{DD} -0.3V	V
Allowable Power Dissipation	P _D	SOT23-6L T _A ≤ +25°C			455	mW
Junction to Ambient Thermal Resistance	θ _{JA}	SOT23-6L			220	°C / W
Operating Temperature			-25		+125	°C
Storage Temperature	T _S	SOP-8L	-40		+150	°C
SOP-8L Lead Temperature		(soldering, 10 sec)			+260	°C

IR Re-flow Soldering Curve



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Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		15		450	V
Operating Temperature Range	T_A	Ambient Temperature	-25		125	°C

DC Electrical Characteristics ($V_{CC}=15V$, $T_A=25^\circ C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Internal Regulator						
Internally regulated voltage	V_{DD}	$V_{IN} = 15V$, $I_{DD(ext)} = 0$, 500pF at GATE; $R_T = 226k\Omega$	7.25	7.5	7.75	V
Line regulation of V_{DD}	ΔV_{DD}	$V_{IN} = 15 - 450V$, $I_{DD(ext)} = 0$, 500pF at GATE; $R_T = 226k\Omega$	0	-	1.0	V
Internal Regulator						
Load regulation of V_{DD}	$\Delta V_{DD,load}$	$I_{DD(ext)} = 0 - 1.0mA$, 500pF at GATE; $R_T = 226k\Omega$	0		100	mV
V_{DD} undervoltage lockout threshold	UVLO	V_{DD} rising	6.45	6.7	6.95	V
V_{DD} undervoltage lockout hysteresis	$\Delta UVLO$	V_{DD} falling		500		mV
Current Sense Comparator						
Current sense pull-in threshold voltage	$V_{CS,TH}$	$-40^\circ C < T_A < +85^\circ C$ $T_A < +125^\circ C$				
Current sense blanking interval	T_{BLANK}	$0 < T_A < +85^\circ C$, $V_{CS} = V_{CS,TH}$ + 50mV after T_{BLANK}	150	215	280	ns
		$-40 < T_A < +125^\circ C$, $V_{CS} =$ $V_{CS,TH} + 50mV$ after T_{BLANK}	145	215	315	
Delay to output	t_{DELAY}			80	150	ns
Oscillator						
Oscillator frequency	f_{OSC}	$R_T = 1.00M\Omega$	20	25	30	kHz
		$R_T = 226k\Omega$	80	100	120	
GATE Driver						
GATE sourcing current	I_{SOURCE}	$V_{GATE} = 0V$, $V_{DD} = 7.5V$	165			mA
GATE sinking current	I_{SINK}	$V_{GATE} = V_{DD}$, $V_{DD} = 7.5V$	165			mA
GATE output rise time	t_{RISE}	$C_{GATE} = 500pF$, $V_{DD} = 7.5V$		30	50	ns
GATE output fall time	t_{FALL}	$C_{GATE} = 500pF$, $V_{DD} = 7.5V$		30	50	ns

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Function Description

Input Voltage Regulator

The FP7172 can be powered directly from its VIN pin and can work from 15 - 450VDC at its VIN pin. When a voltage is applied at the VIN pin, the FP7172 maintains a constant 7.5V at the VDD pin. This voltage is used to power the IC and any external resistor dividers needed to control the IC. The VDD pin must be bypassed by a low ESR capacitor to provide a low impedance path for the high frequency current of the output GATE driver.

The FP7172 can also be operated by supplying a voltage at the VDD pin greater than the internally regulated voltage. This will turn off the internal linear regulator of the IC and the FP7172 will operate directly off the voltage supplied at the VDD pin. Please note that this external voltage at the VDD pin should not exceed 8V.

Although the VIN pin of the FP7172 is rated up to 450V, the actual maximum voltage that can be applied is limited by the power dissipation in the IC. For example, if an 6-pin SOT23-6L (junction to ambient thermal resistance $R_{\theta j-a} = 220^{\circ}\text{C/W}$) FP7172 draws about $I_{IN} = 2.0\text{mA}$ from the VIN pin, and has a maximum allowable temperature rise of the junction temperature limited to about $\Delta T = 100^{\circ}\text{C}$, the maximum voltage at the VIN pin would be:

$$V_{IN(MAX)} = \frac{\Delta T}{R_{\theta j-a}} \cdot \frac{1}{I_{in}} = \frac{100^{\circ}\text{C}}{220^{\circ}\text{C/W}} \cdot \frac{1}{2\text{mA}} = 227\text{V}$$

In these cases, to operate the FP7172 from higher input voltages, a Zener diode can be added in series with the VIN pin to divert some of the power loss from the FP7172 to the Zener diode. In the above example, using a 100V zener diode will allow the circuit to easily work up to 450V.

The input current drawn from the VIN pin is a sum of the 1.0mA current drawn by the internal circuit and the current drawn by the GATE driver (which in turn depends on the switching frequency and the GATE charge of the external FET).

$$I_{IN} \approx 1.0\text{mA} + Q_G \cdot f_S$$

In the above equation, f_S is the switching frequency and Q_G is the GATE charge of the external FET (which can be obtained from the datasheet of the FET).

Current Sense

The current sense input of the FP7172 goes to the noninverting inputs of two comparators. The inverting terminal of one comparator is tied to an internal 250mV reference. The outputs of the comparators also include a 150-280ns blanking time which prevents spurious turn-offs of the external FET due to the turn-on spike normally present in peak current mode control. In rare cases, this internal blanking might not be enough to filter out the turn-on spike. In these cases, an external RC filter needs to be added between the external sense resistor (R_{CS}) and the CS pin.

Please note that the comparators are fast (with a typical 80ns response time). Hence these comparators are more susceptible to be triggered by noise than the comparators of the FP7172. A proper layout minimizing external inductances will prevent false triggering of these comparators.

Oscillator

The oscillator in the FP7172 is controlled by a single resistor connected at the RT pin. The equation governing the oscillator time period t_{OSC} is given by:

$$t_{OSC}(us) = \frac{R_T(k\Omega) + 22}{25}$$

If the resistor is connected between RT and GND, FP7172 operates in a constant frequency mode and the above equation determines the time-period. If the resistor is connected between RT and GATE, the FP7172 operates in a constant off-time mode and the above equation determines the offtime.

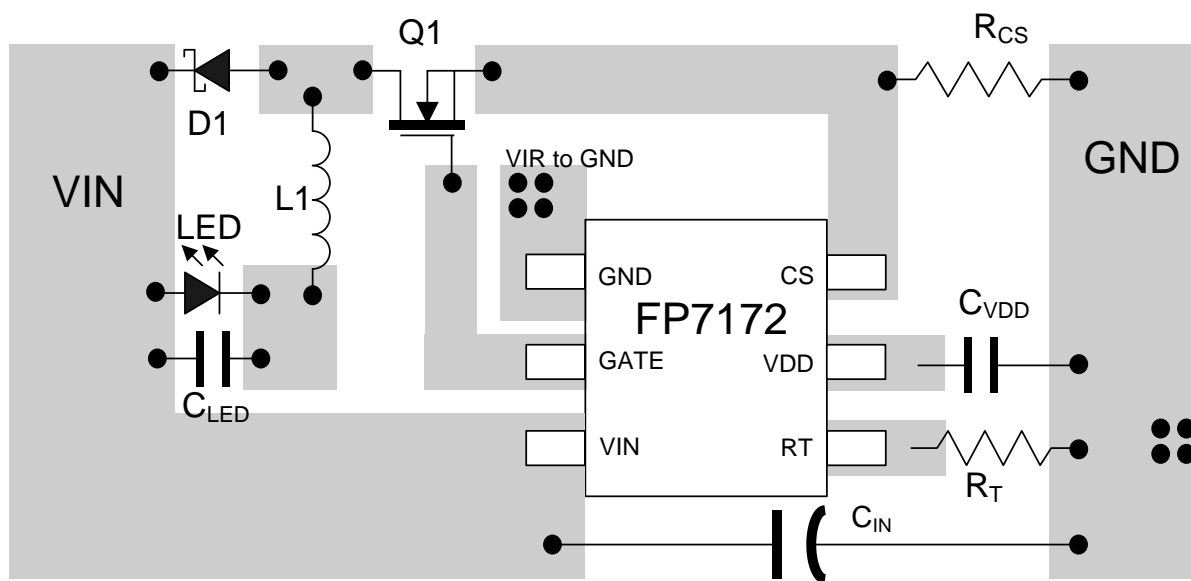
Application Information

The FP7172 is optimized to drive buck LED drivers using open-loop peak current mode control. This method of control enables fairly accurate LED current control without the need for high side current sensing or the design of any closed loop controllers. The IC uses very few external components.

A resistor connected to the RT pin programs the frequency of operation (or the off-time). The oscillator produces pulses at regular intervals. These pulses set the SR flip-flop in the FP7172 which causes the GATE driver to turn on. The same pulses also start the blanking timer which inhibits the reset input of the SR flip flop and prevent false turn-offs due to the turn-on spike. When the FET turns on, the current through the inductor starts ramping up. This current flows through the external sense resistor R_{CS} and produces a ramp voltage at the CS pin. The comparators are constantly comparing the CS pin voltage to the internal 250mV. Once the blanking timer is complete, the output of these comparators is allowed to reset the flip flop. When the output of either one of the two comparators goes high, the flip flop is reset and the GATE output goes low. The GATE goes low until the SR flip flop is set by the oscillator. Assuming a 30% ripple in the inductor, the current sense resistor R_{CS} can be set using:

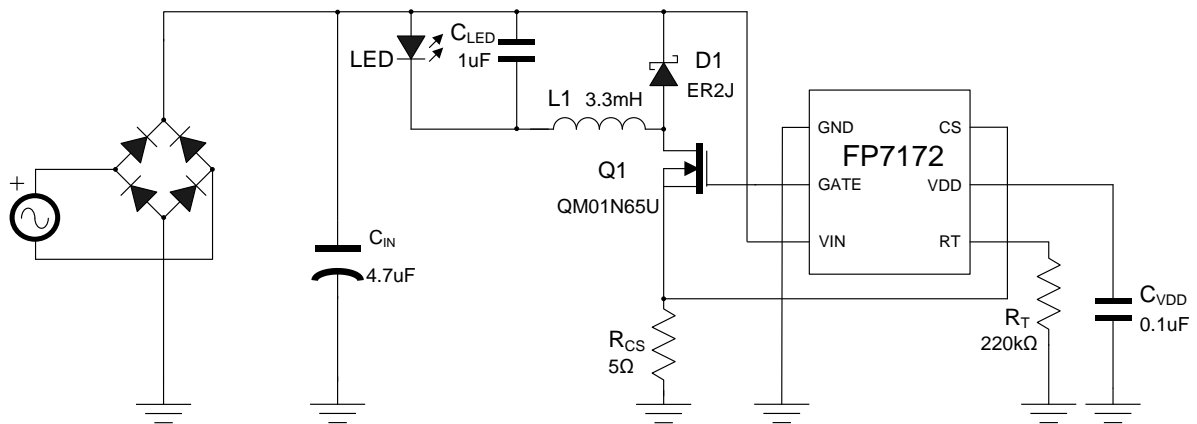
$$R_{CS} = \frac{0.25V}{1.15 \cdot I_{LED} (A)}$$

Constant frequency peak current mode control has an inherent disadvantage – at duty cycles greater than 0.5, the control scheme goes into subharmonic oscillations. To prevent this, an artificial slope is typically added to the current sense waveform. This slope compensation scheme will affect the accuracy of the LED current in the present form. However, a constant off-time peak current control scheme does not have this problem and can easily operate at duty cycles greater than 0.5 and also gives inherent input voltage rejection making the LED current almost insensitive to input voltage variations. But, it leads to variable frequency operation and the frequency range depends greatly on the input and output voltage variation. FP7172 makes it easy to switch between the two modes of operation by changing one connection (see oscillator section).

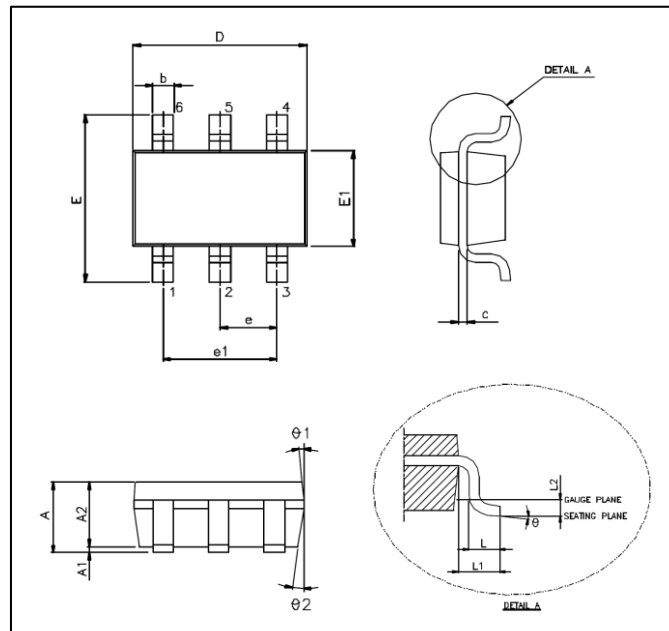


Suggested Layout

Typical Application



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Package Outline
SOT23-6L

Unit: mm

Symbols	Min. (mm)	Max. (mm)
A	1.050	1.450
A1	0.050	0.150
A2	0.900	1.300
b	0.300	0.500
c	0.080	0.220
D	2.900 BSC	
E	2.800 BSC	
E1	1.600 BSC	
e	0.950 BSC	
e1	1.900 BSC	
L	0.300	0.600
L1	0.600 REF	
L2	0.250 BSC	
θ°	0°	8°
$\theta 1^\circ$	3°	7°
$\theta 2^\circ$	6°	15°

Note:

1. Package dimensions are in compliance with JEDEC outline: MO-178 AB.
2. Dimension "D" does not include molding flash, protrusions or gate burrs.
3. Dimension "E1" does not include inter-lead flash or protrusions.

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