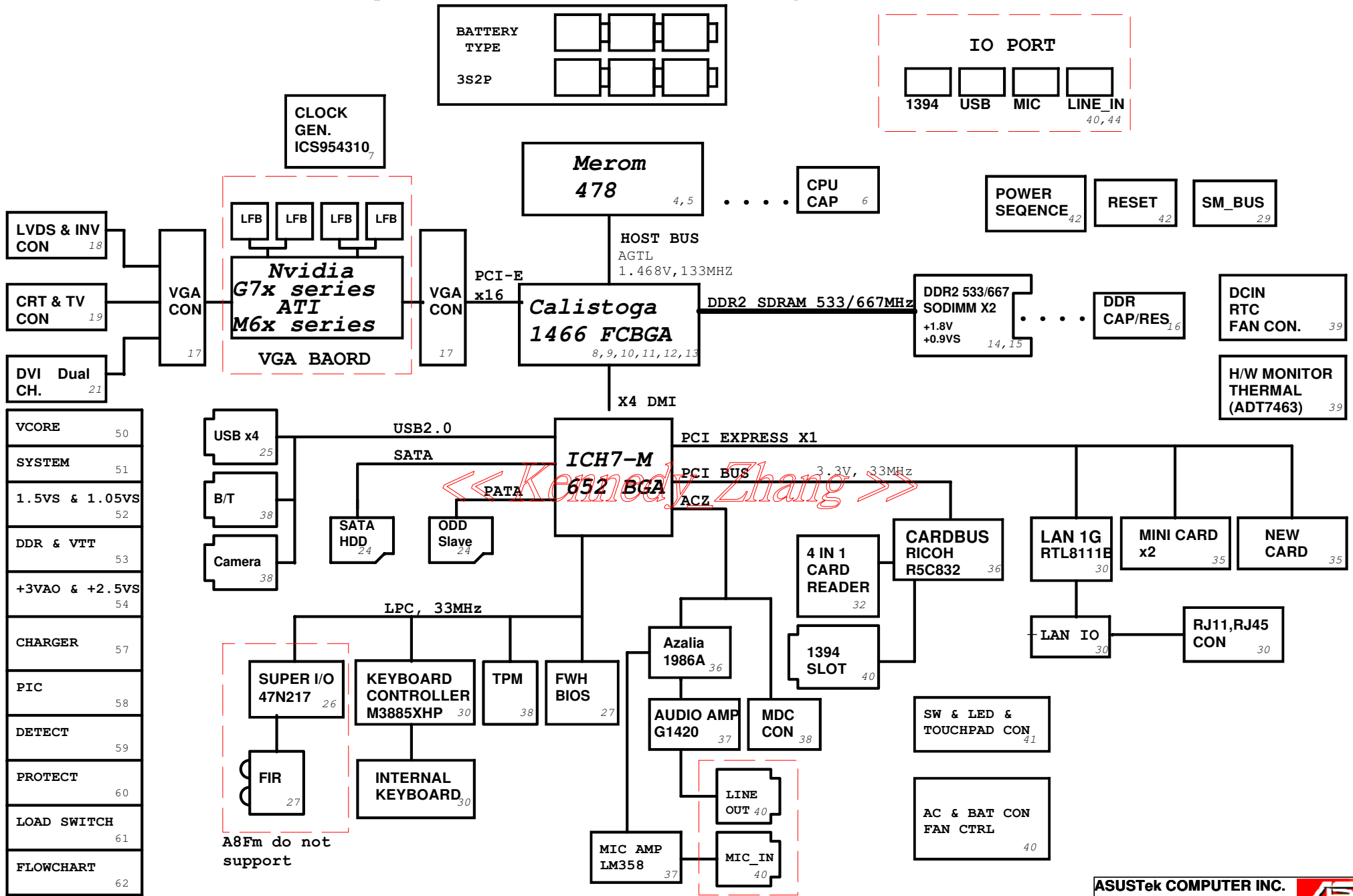


A8Jp/Jv/Je/Jn/Fm SCHEMATIC

PAGE	Content	PAGE	Content
	SYSTEM PAGE REF.		POWER PAGE REF.
4	Merom CPU (1)	50	POWER_VCORE
5	Merom CPU (2)	51	POWER_SYSTEM
6	CPU CAP/THERMAL SENSOR	52	POWER_I/O_1.8V & 1.05VS
7	CLOCK GEN.	53	POWER_I/O_+1.5VS
8	Calistoga--CPU	54	POWER_I/O_VTT & +2.5VS
9	Calistoga--PCIE	55	POWER_VGA_CORE (Empty)
10	Calistoga--DDR2	56	POWER_VGA_RAM (Empty)
11	Calistoga--POWER	57	POWER_CHARGER
12	Calistoga--GND	58	POWER_PIC
13	Calistoga--Strap	59	POWER_SELECTOR
14	DDR2 SO-DIMM_0	60	POWER_PROTECT
15	DDR2 SO-DIMM_1	61	POWER_LOAD SWITCH
16	DDR2 ADDRESS TERMINATION	62	POWER_FLOWCHART
17	VGA CONN	63	POWER_SIGNAL
18	LVDS & INVERTER CONN		
19	CRT & TV_OUT		
20	ICH7M--CPU, IDE, AUDIO		
21	ICH7M--PCI, PCI-E, USB		
22	ICH7M--GPIO		
23	ICH7M--VCC, GND		
24	HDD & CD-ROM CONN		
25	USB PORTS		
26	SUPER I/O LPC47N217		
27	BIOS & FIR		
28	KBC 38857		
29	SM BUS & POWER PORT		
30	PCI-E--GIGA_LAN RTL8111B		
31	PCI-E--MINI CARD		
32	PCI-E--NEW CARD		
33	PCI--1394, CardReader R5C832		
34	PCI--4 IN1 CON		
35	PCI--Empty		
36	AUDIO CODEC AD1986A		
37	AUDIO AMP G1420		
38	MDC, B/T, TPM & DISCHG, HOLE		
39	DVI CONN		
40	ACIN, BAT, FAN, I/O PORT		
41	SW & LED & TP		
42	POWER-ON SEQUENCE		
43	HISTORY		
44	I/O PORT		

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A8Jp/Fm Merom/Calistoga BLOCK DIAGRAM



VCORE	50
SYSTEM	51
1.5VS & 1.05VS	52
DDR & VTT	53
+3VAO & +2.5VS	54
CHARGER	57
PIC	58
DETECT	59
PROTECT	60
LOAD SWITCH	61
FLOWCHART	62
SIGNAL	63

A8Fm do not support

PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
Integrated LAN	AD24 (NO USE)			
1394	AD16	0	A	
4 IN 1		0	B	

SM_BUS ADDRESS : Thermal MAX6657 = 1001100x (98h)
 CLK_GEN. = 1101001x (D2h)
 DDR_SODIMMO = 1010000x (A0h)
 DDR_SODIMM1 = 1010010x (A4h)
 VGA_Thermal IC = 1001100x (9Ah)

ICH7M_GPIO	Use As	Signal Name	Power	
GPIO 00	i	GPI	PM_BMBUSY#	+3VS
GPIO 01	i	GPI	PCI_REQ#5	+3VS
GPIO [5:2]	i	GPI	PCI_INT[E:H]#	+3VS
GPIO 06	i	GPO	BACK_OFF#	+3VS
GPIO 07	i	GPI	RF_SW_OFF#	+3VS
GPIO 08	i	GPI	EXTSMI#_3A	+3VSUS
GPIO 09	i	GPI	PD_DET#	+3VSUS
GPIO 10	i	GPI	CHG_FULL_OC	+3VSUS
GPIO 11	i	Native	SMB_ALERT#	+3VSUS
GPIO 12	i	GPI	KB_SCI#	+3VSUS
GPIO 13	i	GPI	SIO_SMI#	+3VSUS
GPIO 14	i	GPI	PD_UnDock# (PWRLMT#)	+3VSUS
GPIO 15	i	GPO	802_LED_EN#	+3VSUS
GPIO 16	00	GPO	PM DPRSLPVR	+3VS
GPIO 17	01	GPO	PCI_GNT#5	+3VS
GPIO 18	01	GPO	STP_PCI#	+3VS
GPIO 19	i1	GPI	PD_RDY#	+3VS
GPIO 20	01	GPO	STP_CPU#	+3VS
GPIO 21	i1	GPO	PD_SIO_RST#	+3VS
GPIO 22	i1	Native	PCI_REQ#4	+3VS
GPIO 23	i1	Native	LPC_DRQ#1	+3VS
GPIO 24	00	GPO	PD_EN#	+3VSUS
GPIO 25	01	GPO	CB_SD#	+3VSUS
GPIO 26	00	GPO	OP_SD#	+3VSUS
GPIO 27	00	GPO	WLAN_ON#	+3VSUS
GPIO 28	00	GPO	1Hz	+3VSUS
GPIO 29	i0	Native	USB_OC#5	+3VSUS
GPIO 30	i0	Native	USB_OC#6	+3VSUS
GPIO 31	i0	Native	USB_OC#7	+3VSUS
GPIO 32	01	GPO	PM_CLKRUN#	+3VS
GPIO 33	01	GPO	BT_ON/OFF#	+3VS
GPIO 34	00	GPO	FWH_WP#	+3VS
GPIO 35	00	GPO	SATACLKREQ#	+3VS
GPIO 36	i0	GPO	BT_LED_EN#	+3VS
GPIO 37	i0	GPI	PCB_ID0	+3VS
GPIO 38	i0	GPI	PCB_ID1	+3VS
GPIO 39	i0	GPI	PCB_ID2	+3VS
GPIO [40:47]	NA	NA	NA	NA
GPIO 48	Native	PCI_GNT#4	+3VS	
GPIO 49	Native	H_PWRGD	+VCORE	

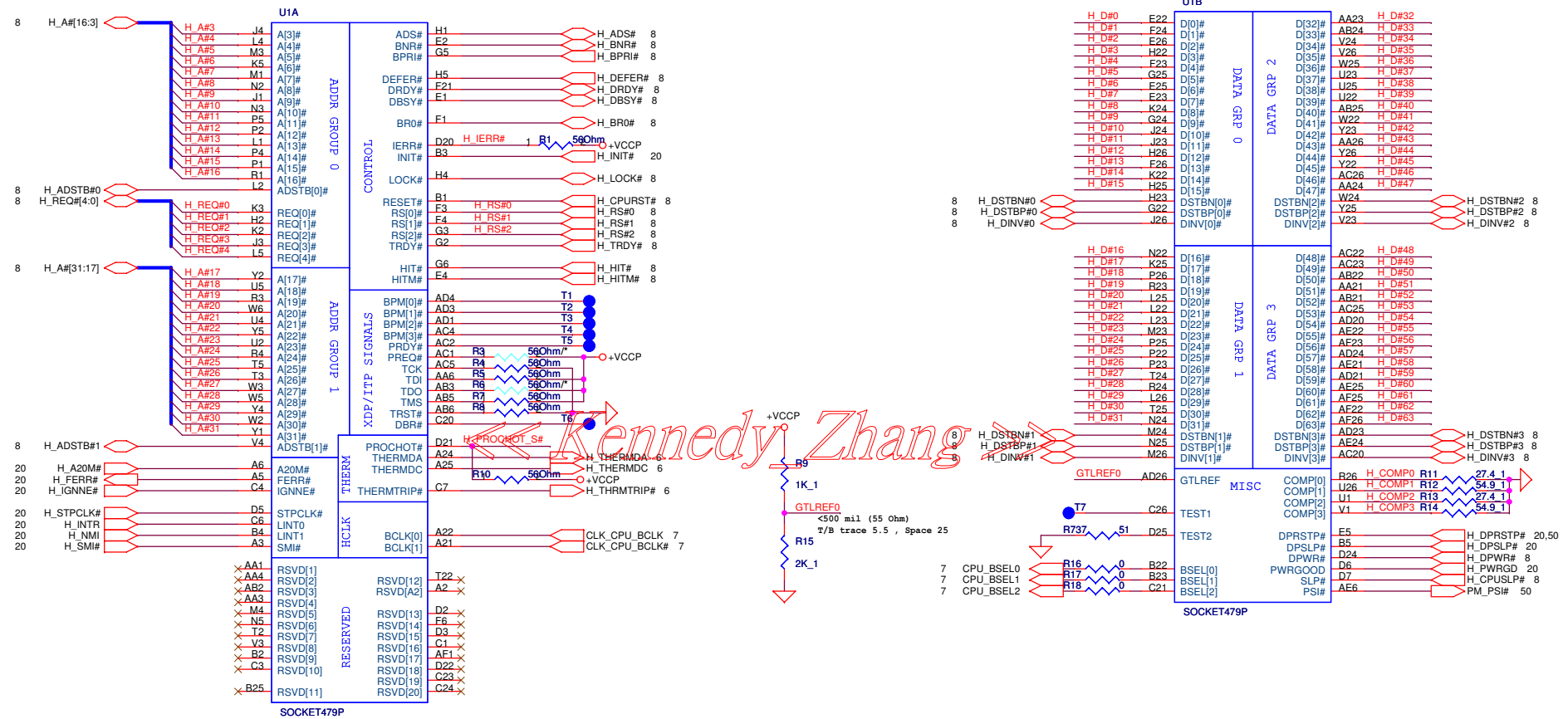
M38857_GPIO	USE_AS	SIGNAL_NAME	Power
P23	GPO	MSK_INSTKEY#	+3V
P22	GPO	BAT_LEARN	+3V
P21	GPO		+3V
P20	GPO	KBCRSM	+3V
P42	GPO	WATCHDOG	+3V
P43	GPI	SWDJ_EN	+3V
P44	GPO	KBCPURST_3Q	+3V
P45	GPO	KBC_GA20	+3V
P46	GPO	KBSCI_3Q	+3V
P47	GPI	PM_CLKRUN#	+3V
P50	GPI	BAT_LLOW#_OC	+3V
P51	GPI	FAN1_TACH	+3V
P52	GPO	KBDDT0	+3V
P53	GPO	KBDDT1	+3V
P54	GPI	LID_KBC#	+3V
P55	GPI	BAT_IN_OC#	+3V
P56	GPO	FAN1_DC	+3V
P57	GPO	ADJ_BL	+3V
P67	GPI	NEWCARD_OFF#	+3V
P66	GPI	PANLOCK_#	+3V
P65	GPI	MARATHON_#	+3V
P64	GPI	ACIN_OC#	+3V
P63	GPI	NEWCARD_DET#	+3V
P62	GPI	WIRELESS_#	+3V
P61	GPI	INTERNET_#	+3V
P60	GPI	BLUETOOTH_#	+3V
P76	GPIO	SMD_BAT	+3V
P77	GPIO	SMC_BAT	+3V
P27	GPO	SCR_LED#	+3V
P26	GPO	NUM_LED#	+3V
P25	GPO	CAP_LED#	+3V
P24	GPO	SET_PCIRSTNS#	+3V
P40	GPO	KBC_EXTSMI	+3V
P41	GPO	PANLOCK_LED	+3V

47N217_GPIO	USE_AS	SIGNAL_NAME	Power
GPIO10	GPI	NONE	+3VS
GPIO11	GPO	NONE	+3VS
GPIO12	GPO	NONE	+3VS
GPIO13	GPI	NONE	+3VS
GPIO14	GPI	NONE	+3VS
GPIO23	GPO	ATI_RST#	+3VS
GPIO40	GPI		+3VS
GPIO41	GPI		+3VS
GPIO40	GPI		+3VS
GPIO43	GPI		+3VS
GPIO44	GPI		+3VS
GPIO45	GPI		+3VS
GPIO46	GPI	VGA_DETEC#	+3VS
GPIO47	GPI		+3VS

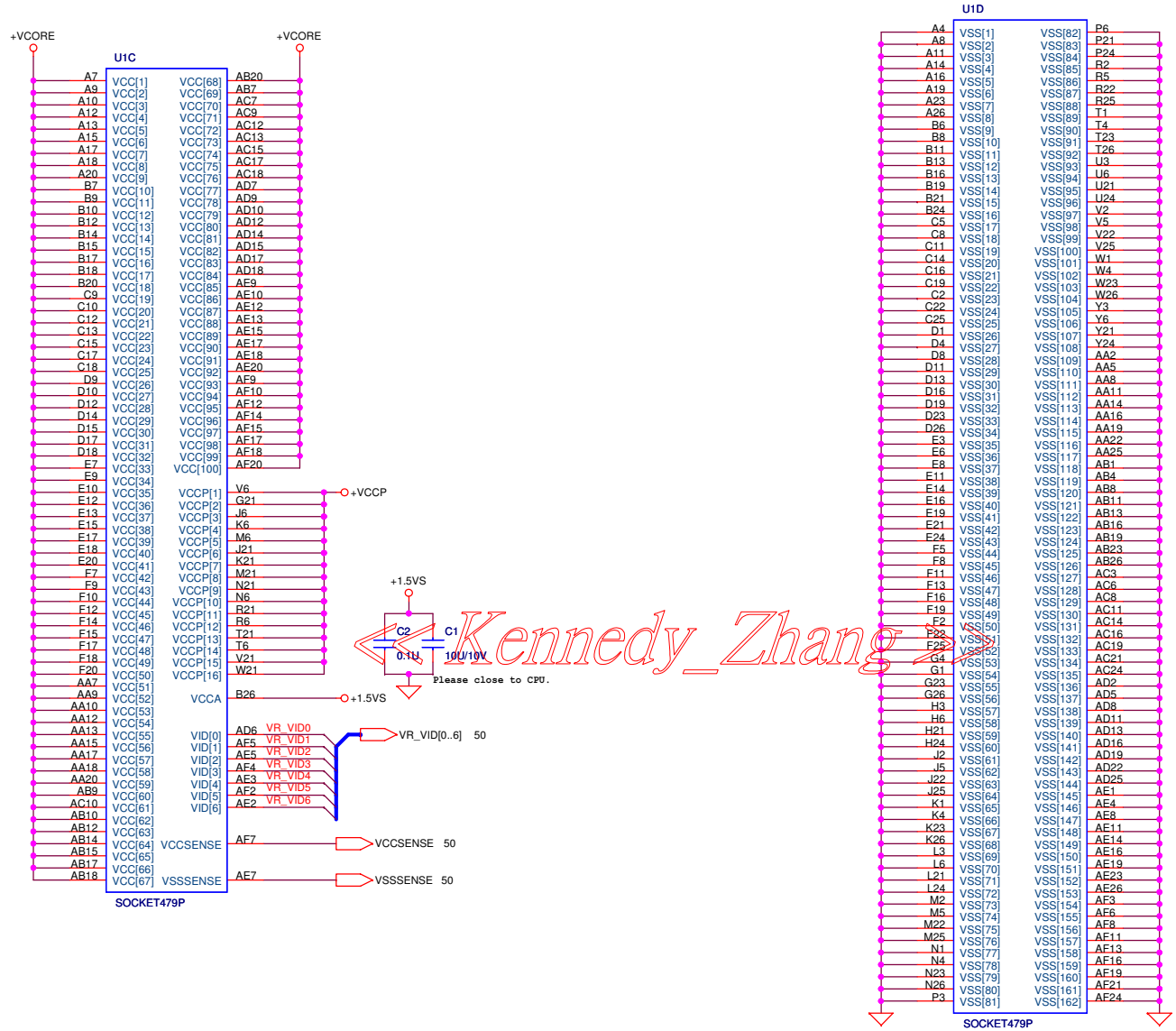
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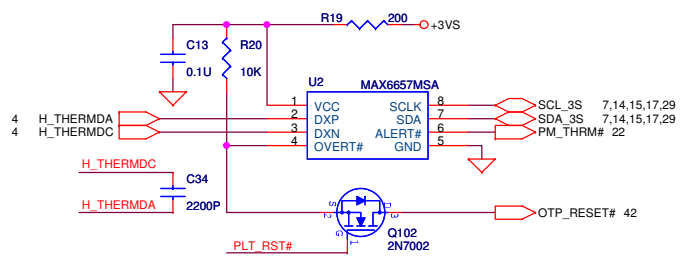
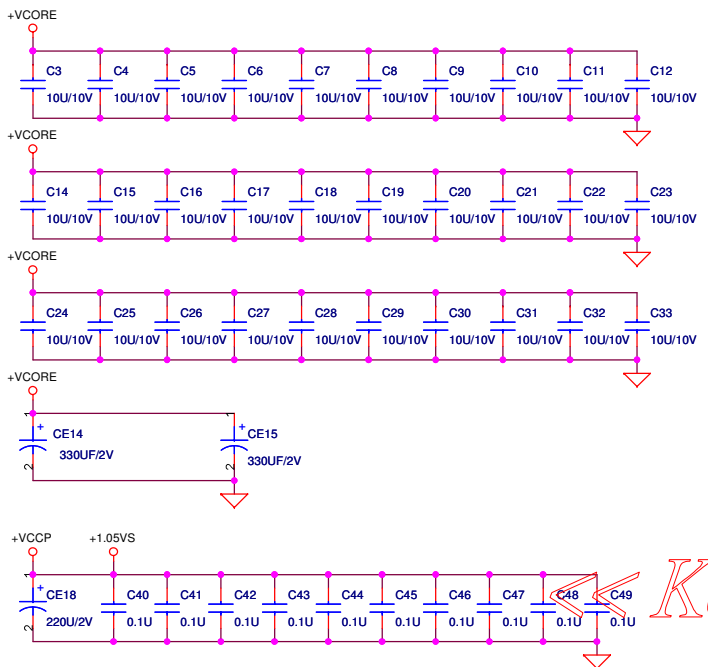
+VCCP ○ ———— ⊞ ———— +VCCP 5,6,8,11,12,20,23,52

H_D#[63:0] ⊞ H_D#[63:0] 8

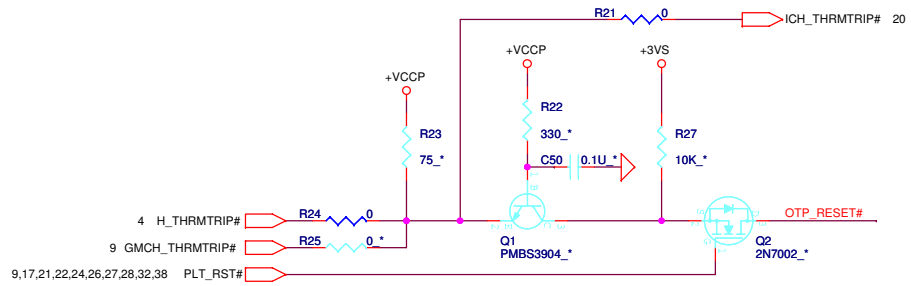
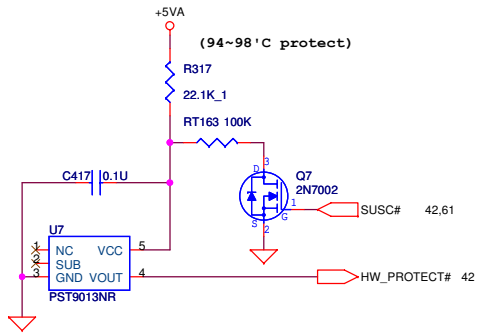


+VCCP 4,6,8,11,12,20,23,52
 +1.5VS 9,11,12,17,23,31,32,38,52
 +VCORE 6,50





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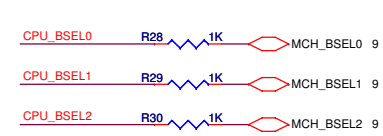
+VCCP	4,5,8,11,12,20,23,52
+VCCORE	5,50
+3VS	7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61
+5VA	51,54

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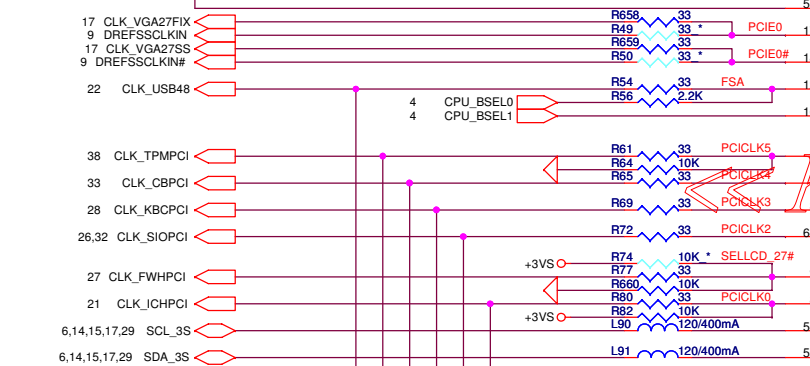
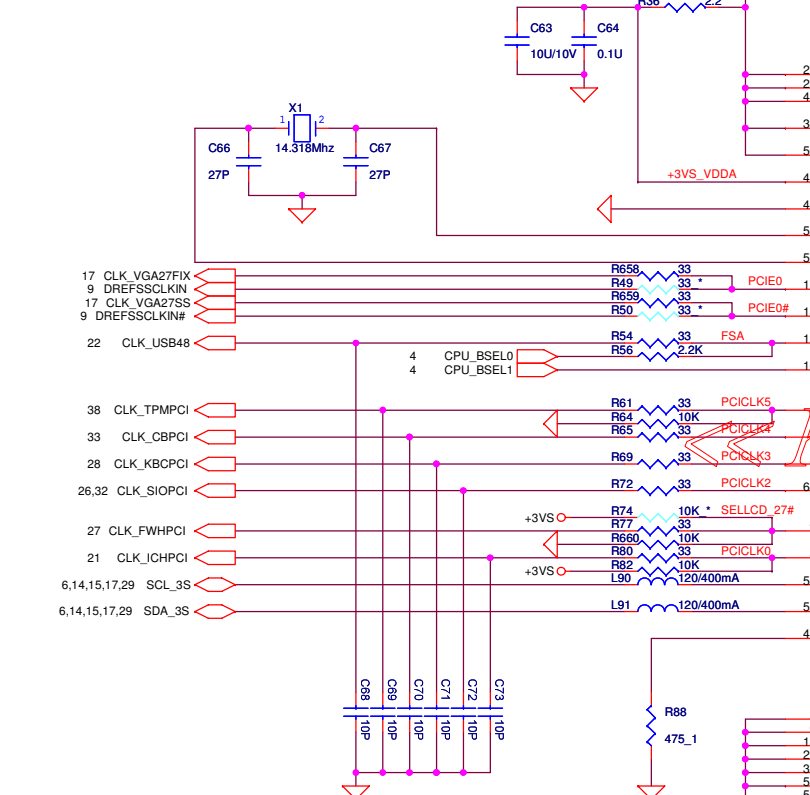
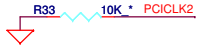
4 FL No.150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC

Title: **CPU CAP, THERMAL SENSOR**

Size: Custom	Document Number: A8J/F	Rev: 2.0
Date: Thursday, September 07, 2006	Sheet: 6	of 63



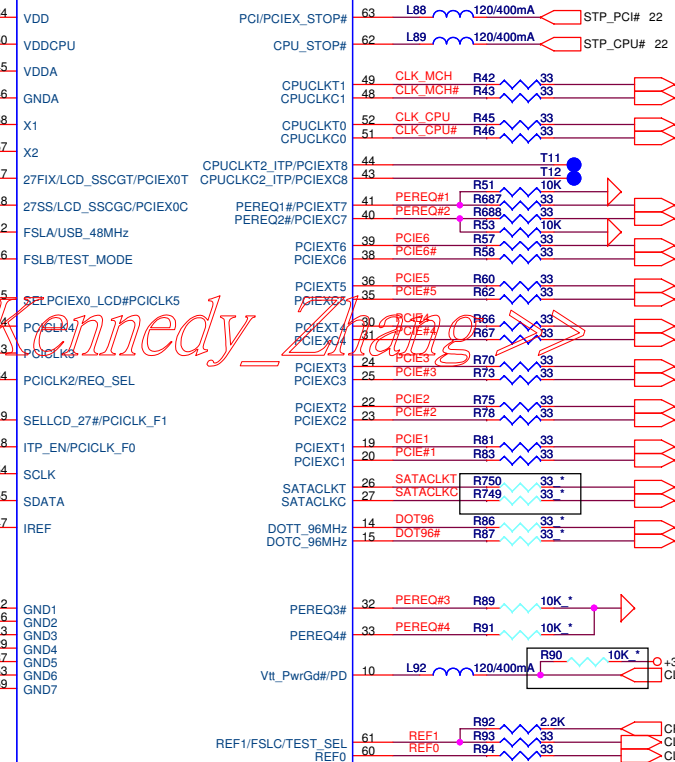
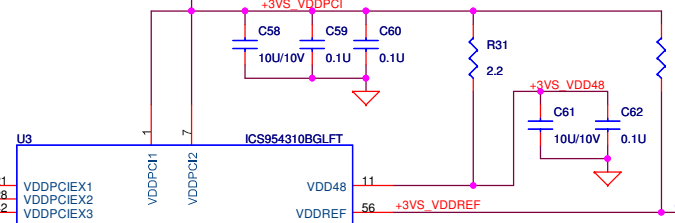
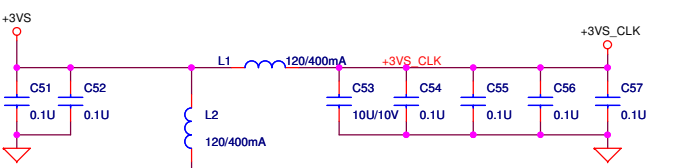
Bclk	FSB	FSLC	FSLB	FSLA
133	533	L	L	H
166	667	L	H	H



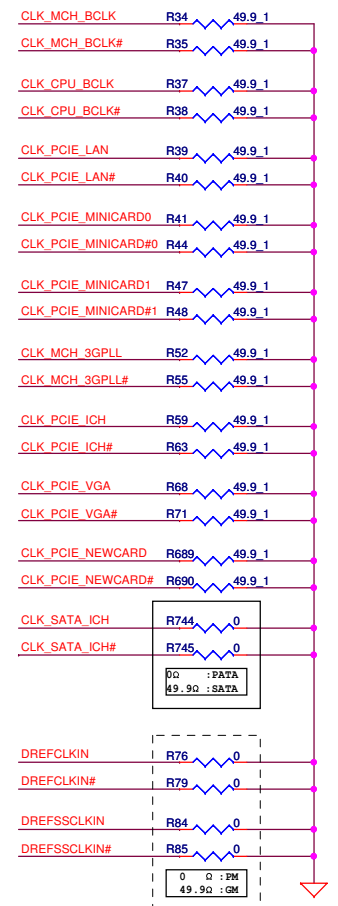
/	PIN9	PIN5	PIN17	PIN18
*	0	X	27FIX	27SS
	1	0	96MSS_T	96MSS_C
	1	1	PCIEX0_T	PCIEX0_C

PIN8 : 0=SRC Pair, 1=CPU_ITP pair
 PIN64: 0=PCIEXCLK, 1=PEREQ#

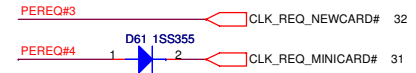
Int. PU: PIN5, PIN9, PIN32, PIN33, PIN34
 Int. PD: PIN64

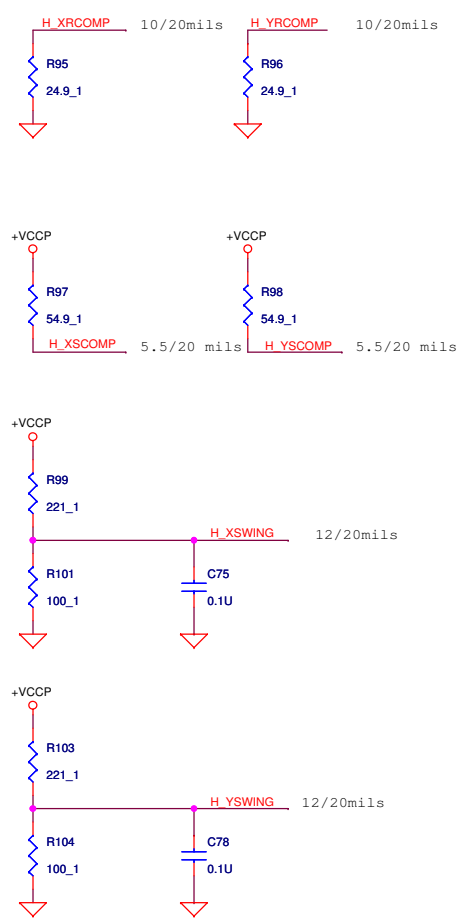


PLACE termination close to source IC



PEREQ#1: PCIEX0, PCIEX6
 PEREQ#2: PCIEX1, PCIEX8
 PEREQ#3: PCIEX2, PCIEX4
 PEREQ#4: PCIEX3, PCIEX5, PCIEX7



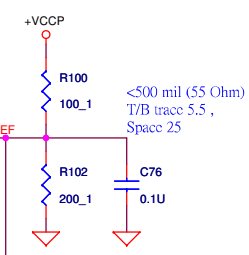


4 H_D#[0..63]		U4A		H_A#[3..31]	
H_D#0	F1	H_D#_0	H_A#_3	H9	H_A#3
H_D#1	J1	H_D#_1	H_A#_4	C9	H_A#4
H_D#2	H1	H_D#_2	H_A#_5	E11	H_A#5
H_D#3	J6	H_D#_3	H_A#_6	G11	H_A#6
H_D#4	H3	H_D#_4	H_A#_7	F11	H_A#7
H_D#5	K2	H_D#_5	H_A#_8	G12	H_A#8
H_D#6	G1	H_D#_6	H_A#_9	F9	H_A#9
H_D#7	G2	H_D#_7	H_A#_10	H11	H_A#10
H_D#8	K9	H_D#_8	H_A#_11	J12	H_A#11
H_D#9	K4	H_D#_9	H_A#_12	G14	H_A#12
H_D#10	K7	H_D#_10	H_A#_13	D9	H_A#13
H_D#11	J8	H_D#_11	H_A#_14	J14	H_A#14
H_D#12	H4	H_D#_12	H_A#_15	H13	H_A#15
H_D#13	J3	H_D#_13	H_A#_16	J15	H_A#16
H_D#14	K11	H_D#_14	H_A#_17	F14	H_A#17
H_D#15	G4	H_D#_15	H_A#_18	D12	H_A#18
H_D#16	T10	H_D#_16	H_A#_19	A11	H_A#19
H_D#17	W11	H_D#_17	H_A#_20	C11	H_A#20
H_D#18	T3	H_D#_18	H_A#_21	A12	H_A#21
H_D#19	U7	H_D#_19	H_A#_22	A13	H_A#22
H_D#20	U9	H_D#_20	H_A#_23	E13	H_A#23
H_D#21	U11	H_D#_21	H_A#_24	G13	H_A#24
H_D#22	T11	H_D#_22	H_A#_25	F12	H_A#25
H_D#23	W9	H_D#_23	H_A#_26	B12	H_A#26
H_D#24	T1	H_D#_24	H_A#_27	B14	H_A#27
H_D#25	T8	H_D#_25	H_A#_28	C12	H_A#28
H_D#26	T4	H_D#_26	H_A#_29	A14	H_A#29
H_D#27	W7	H_D#_27	H_A#_30	C14	H_A#30
H_D#28	U5	H_D#_28	H_A#_31	D14	H_A#31
H_D#29	T9	H_D#_29			
H_D#30	W6	H_D#_30	H_ADS#	E8	H_ADS#0
H_D#31	T5	H_D#_31	H_ADSTB#_0	B9	H_ADSTB#0
H_D#32	AB7	H_D#_32	H_ADSTB#_1	C13	H_ADSTB#1
H_D#33	AA9	H_D#_33	H_ADSTB#_2	J13	H_ADSTB#2
H_D#34	W4	H_D#_34	H_AVREF		
H_D#35	W3	H_D#_35	H_BNR#	C6	H_BNR#
H_D#36	Y7	H_D#_36	H_BPRI#	F6	H_BPRI#
H_D#37	W5	H_D#_37	H_BREQ#	E7	H_BREQ#
H_D#38	Y10	H_D#_38	H_CPURST#	B7	H_CPURST#
H_D#39	AB8	H_D#_39	H_DBSY#	A7	H_DBSY#
H_D#40	W2	H_D#_40	H_DEFER#	C3	H_DEFER#
H_D#41	W2	H_D#_41	H_DPWR#	J9	H_DPWR#
H_D#42	AA4	H_D#_42	H_DRDY#	H8	H_DRDY#
H_D#43	AA7	H_D#_43	H_DVREF	K13	
H_D#44	AA2	H_D#_44			
H_D#45	AA6	H_D#_45	H_DINV#_0	J7	H_DINV#0
H_D#46	AA10	H_D#_46	H_DINV#_1	W8	H_DINV#1
H_D#47	AA11	H_D#_47	H_DINV#_2	U3	H_DINV#2
H_D#48	AA12	H_D#_48	H_DINV#_3	AA10	H_DINV#3
H_D#49	AA4	H_D#_49	H_DSTBN#_0	K4	H_DSTBN#0
H_D#50	AC9	H_D#_50	H_DSTBN#_1	G7	H_DSTBN#1
H_D#51	AB11	H_D#_51	H_DSTBN#_2	Y5	H_DSTBN#2
H_D#52	AC11	H_D#_52	H_DSTBN#_3	AC4	H_DSTBN#3
H_D#53	AB3	H_D#_53			
H_D#54	AC2	H_D#_54	H_DSTBP#_0	K3	H_DSTBP#0
H_D#55	AD1	H_D#_55	H_DSTBP#_1	T6	H_DSTBP#1
H_D#56	AD9	H_D#_56	H_DSTBP#_2	AA5	H_DSTBP#2
H_D#57	AC1	H_D#_57	H_DSTBP#_3	AC5	H_DSTBP#3
H_D#58	AD7	H_D#_58			
H_D#59	AC6	H_D#_59	H_HIT#	D3	H_HIT#
H_D#60	AB5	H_D#_60	H_HITM#	D4	H_HITM#
H_D#61	AD10	H_D#_61	H_LOCK#	B3	H_LOCK#
H_D#62	AD4	H_D#_62			
H_D#63	AC8	H_D#_63			
H_XRCOMP	E1	H_XRCOMP			
H_XSCOMP	E2	H_XSCOMP			
H_XSWING	E4	H_XSWING			
H_YRCOMP	Y1	H_YRCOMP			
H_YSCOMP	U1	H_YSCOMP			
H_YSWING	W1	H_YSWING			
CLK_MCH_BCLK	AG2	H_CLKIN			
CLK_MCH_BCLK#	AG1	H_CLKIN#			

+VCCP +VCCP 4,5,6,11,12,20,23,52

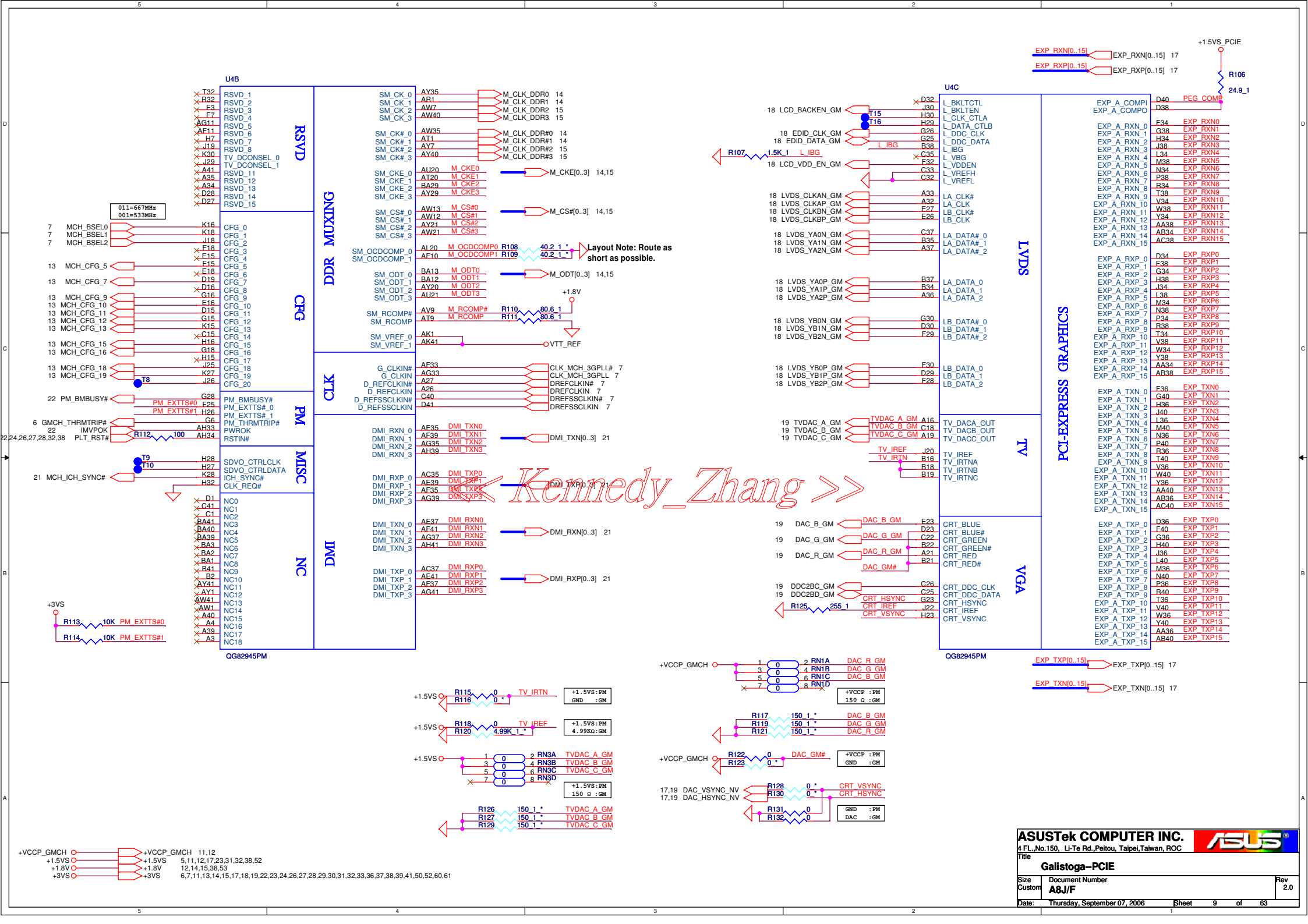
HOST

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H_DINV#_0	W8	H_DINV#1	H_DINV#1	H_DINV#1	4
H_DINV#_1	U3	H_DINV#2	H_DINV#2	H_DINV#2	4
H_DINV#_2	AA10	H_DINV#3	H_DINV#3	H_DINV#3	4
H_DINV#_3					
H_DSTBN#_0	K4	H_DSTBN#0	H_DSTBN#0	H_DSTBN#0	4
H_DSTBN#_1	G7	H_DSTBN#1	H_DSTBN#1	H_DSTBN#1	4
H_DSTBN#_2	Y5	H_DSTBN#2	H_DSTBN#2	H_DSTBN#2	4
H_DSTBN#_3	AC4	H_DSTBN#3	H_DSTBN#3	H_DSTBN#3	4
H_DSTBP#_0	K3	H_DSTBP#0	H_DSTBP#0	H_DSTBP#0	4
H_DSTBP#_1	T6	H_DSTBP#1	H_DSTBP#1	H_DSTBP#1	4
H_DSTBP#_2	AA5	H_DSTBP#2	H_DSTBP#2	H_DSTBP#2	4
H_DSTBP#_3	AC5	H_DSTBP#3	H_DSTBP#3	H_DSTBP#3	4
H_HIT#	D3	H_HIT#	H_HIT#	H_HIT#	4
H_HITM#	D4	H_HITM#	H_HITM#	H_HITM#	4
H_LOCK#	B3	H_LOCK#	H_LOCK#	H_LOCK#	4
H_REQ#_0	D8	H_REQ#0			
H_REQ#_1	G8	H_REQ#1			
H_REQ#_2	B8	H_REQ#2			
H_REQ#_3	F8	H_REQ#3	H_REQ#[4..0]	4	
H_REQ#_4	A8	H_REQ#4			
H_RS#_0	B4	H_RS#0	H_RS#[0..2]	4	
H_RS#_1	E6	H_RS#1			
H_RS#_2	D6	H_RS#2			
H_SLP0PU#	E3	H_TRDY#	R105	H_CPUSLP#	4
H_TRDY#	E7			H_TRDY#	4

QG82945PM



EXP_RXN[0..15] EXP_RXN[0..15] 17
 EXP_RXP[0..15] EXP_RXP[0..15] 17

+1.5V_PCIE
 R106
 24.9_1

U4B

U4C

RSVD

DDR MUXING

CFG

CLK

PM

MISC

NC

DDR MUXING

DMI

LVDS

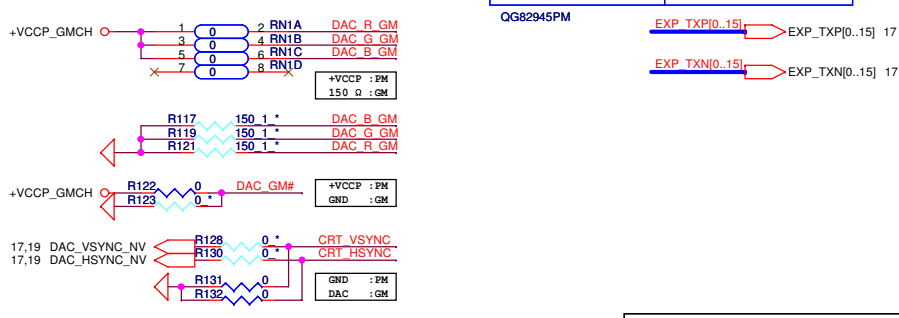
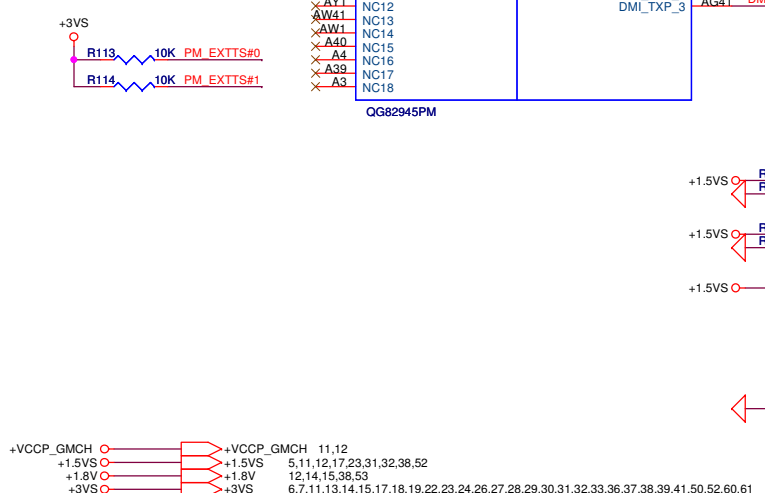
PCI-EXPRESS GRAPHICS

TV

VGA

Layout Note: Route as short as possible.

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4 FL_No.150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC
 Title Gallitoga-PCIE
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 Date Thursday, September 07, 2006 Sheet 9 of 63

14 M_A_DQ[0..63]

U4D

M_A_D00	AJ35	SA_D00
M_A_D01	AJ34	SA_D01
M_A_D02	AM31	SA_D02
M_A_D03	AM33	SA_D03
M_A_D04	AJ36	SA_D04
M_A_D05	AK35	SA_D05
M_A_D06	AJ32	SA_D06
M_A_D07	AH31	SA_D07
M_A_D08	AN35	SA_D08
M_A_D09	AP33	SA_D09
M_A_D010	AR31	SA_D010
M_A_D011	AP31	SA_D011
M_A_D012	AN38	SA_D012
M_A_D013	AM36	SA_D013
M_A_D014	AM34	SA_D014
M_A_D015	AN33	SA_D015
M_A_D016	AK26	SA_D016
M_A_D017	AL27	SA_D017
M_A_D018	AM26	SA_D018
M_A_D019	AN24	SA_D019
M_A_D020	AK28	SA_D020
M_A_D021	AL28	SA_D021
M_A_D022	AM24	SA_D022
M_A_D023	AP26	SA_D023
M_A_D024	AP23	SA_D024
M_A_D025	AL22	SA_D025
M_A_D026	AP21	SA_D026
M_A_D027	AN20	SA_D027
M_A_D028	AL23	SA_D028
M_A_D029	AP24	SA_D029
M_A_D030	AP20	SA_D030
M_A_D031	AT21	SA_D031
M_A_D032	AR12	SA_D032
M_A_D033	AR14	SA_D033
M_A_D034	AP13	SA_D034
M_A_D035	AP12	SA_D035
M_A_D036	AT13	SA_D036
M_A_D037	AT12	SA_D037
M_A_D038	AL14	SA_D038
M_A_D039	AL12	SA_D039
M_A_D040	AK9	SA_D040
M_A_D041	AN7	SA_D041
M_A_D042	AK8	SA_D042
M_A_D043	AK7	SA_D043
M_A_D044	AP9	SA_D044
M_A_D045	AN9	SA_D045
M_A_D046	AT5	SA_D046
M_A_D047	AL5	SA_D047
M_A_D048	AY2	SA_D048
M_A_D049	AW2	SA_D049
M_A_D050	AP1	SA_D050
M_A_D051	AN2	SA_D051
M_A_D052	AV2	SA_D052
M_A_D053	AT3	SA_D053
M_A_D054	AN1	SA_D054
M_A_D055	AL2	SA_D055
M_A_D056	AG7	SA_D056
M_A_D057	AF9	SA_D057
M_A_D058	AG4	SA_D058
M_A_D059	AF6	SA_D059
M_A_D060	AG9	SA_D060
M_A_D061	AH6	SA_D061
M_A_D062	AF4	SA_D062
M_A_D063	AF8	SA_D063

QG82945PM

DDR SYSTEM MEMORY A

SA_BS_0	AU12
SA_BS_1	AV14
SA_BS_2	BA20
SA_CAS#	AY13
SA_DM_0	AJ33
SA_DM_1	AM35
SA_DM_2	AL26
SA_DM_3	AN22
SA_DM_4	AM14
SA_DM_5	AL9
SA_DM_6	AR3
SA_DM_7	AH4
SA_DQS_0	AK33
SA_DQS_1	AT33
SA_DQS_2	AN28
SA_DQS_3	AM22
SA_DQS_4	AN12
SA_DQS_5	AN8
SA_DQS_6	AP3
SA_DQS_7	AK32
SA_DQS#_0	AU33
SA_DQS#_1	AN27
SA_DQS#_2	AM21
SA_DQS#_3	AM12
SA_DQS#_4	AL8
SA_DQS#_5	AN3
SA_DQS#_6	AH5
SA_DQS#_7	
SA_MA_0	AY16
SA_MA_1	AU14
SA_MA_2	AW16
SA_MA_3	BA16
SA_MA_4	BA17
SA_MA_5	AU16
SA_MA_6	AV17
SA_MA_7	AU17
SA_MA_8	AV17
SA_MA_9	AT16
SA_MA_10	AU13
SA_MA_11	AT17
SA_MA_12	AV20
SA_MA_13	AV12
SA_RAS#	AW14
SA_RCVENIN#	AK23
SA_RCVENOUT#	AK24
SA_WE#	AY14

M_A_BS#0	14	M_A_BS#0
M_A_BS#1	14	M_A_BS#1
M_A_BS#2	14	M_A_BS#2
M_A_CAS#	14,16	M_A_CAS#
M_A_DM[0..7]	14	M_A_DM[0..7]
M_A_DQS[0..7]	14	M_A_DQS[0..7]
M_A_DQS#[0..7]	14	M_A_DQS#[0..7]
M_A_A[0..13]	14	M_A_A[0..13]
M_A_RAS#	14,16	M_A_RAS#
M_A_WE#	14,16	M_A_WE#

15 M_B_DQ[0..63]

U4E

M_B_D00	AK39	SB_D00
M_B_D01	AJ37	SB_D01
M_B_D02	AP39	SB_D02
M_B_D03	AR41	SB_D03
M_B_D04	AJ38	SB_D04
M_B_D05	AK38	SB_D05
M_B_D06	AN41	SB_D06
M_B_D07	AN41	SB_D07
M_B_D08	AT40	SB_D08
M_B_D09	AV41	SB_D09
M_B_D010	AU38	SB_D010
M_B_D011	AV38	SB_D011
M_B_D012	AP38	SB_D012
M_B_D013	AR40	SB_D013
M_B_D014	AW38	SB_D014
M_B_D015	AY38	SB_D015
M_B_D016	BA38	SB_D016
M_B_D017	AV36	SB_D017
M_B_D018	AR36	SB_D018
M_B_D019	AP36	SB_D019
M_B_D020	AR36	SB_D020
M_B_D021	AU36	SB_D021
M_B_D022	AP35	SB_D022
M_B_D023	AP34	SB_D023
M_B_D024	AY33	SB_D024
M_B_D025	BA33	SB_D025
M_B_D026	AT31	SB_D026
M_B_D027	AU29	SB_D027
M_B_D028	AW31	SB_D028
M_B_D029	AV29	SB_D029
M_B_D030	AW29	SB_D030
M_B_D031	AM19	SB_D031
M_B_D032	AL19	SB_D032
M_B_D033	AP14	SB_D033
M_B_D034	AN14	SB_D034
M_B_D035	AN14	SB_D035
M_B_D036	AN17	SB_D036
M_B_D037	AM16	SB_D037
M_B_D038	AK15	SB_D038
M_B_D039	AL17	SB_D039
M_B_D040	AH14	SB_D040
M_B_D041	AH10	SB_D041
M_B_D042	AJ9	SB_D042
M_B_D043	AN10	SB_D043
M_B_D044	AK13	SB_D044
M_B_D045	AK11	SB_D045
M_B_D046	AK10	SB_D046
M_B_D047	AJ8	SB_D047
M_B_D048	BA10	SB_D048
M_B_D049	AW10	SB_D049
M_B_D050	BA4	SB_D050
M_B_D051	AW4	SB_D051
M_B_D052	AY10	SB_D052
M_B_D053	AY9	SB_D053
M_B_D054	AW5	SB_D054
M_B_D055	AY5	SB_D055
M_B_D056	AV4	SB_D056
M_B_D057	AR5	SB_D057
M_B_D058	AK3	SB_D058
M_B_D059	AK3	SB_D059
M_B_D060	AT4	SB_D060
M_B_D061	AK5	SB_D061
M_B_D062	AJ5	SB_D062
M_B_D063	AJ3	SB_D063

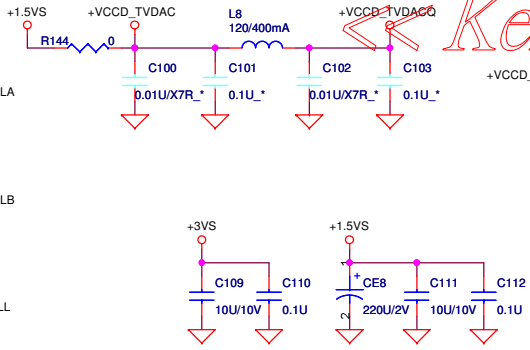
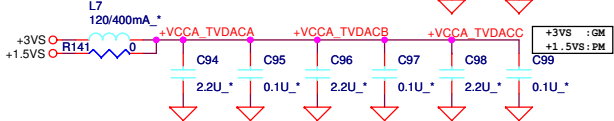
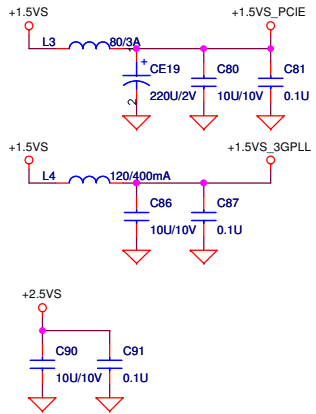
QG82945PM

DDR SYSTEM MEMORY B

SB_BS_0	AT24
SB_BS_1	AV23
SB_BS_2	AY28
SB_CAS#	AR24
SB_DM_0	AK36
SB_DM_1	AR38
SB_DM_2	BA31
SB_DM_3	AL17
SB_DM_4	AH8
SB_DM_5	BA5
SB_DM_6	AN4
SB_DM_7	
SB_DQS_0	AM39
SB_DQS_1	AT39
SB_DQS_2	AU35
SB_DQS_3	AR29
SB_DQS_4	AR16
SB_DQS_5	AR10
SB_DQS_6	AR7
SB_DQS_7	AN5
SB_DQS#_0	AM40
SB_DQS#_1	AU39
SB_DQS#_2	AT35
SB_DQS#_3	AP29
SB_DQS#_4	AP16
SB_DQS#_5	AT10
SB_DQS#_6	AT7
SB_DQS#_7	AP5
SB_MA_0	AY23
SB_MA_1	AW24
SB_MA_2	AY24
SB_MA_3	AR28
SB_MA_4	AT27
SB_MA_5	AT28
SB_MA_6	AU27
SB_MA_7	AV28
SB_MA_8	AV27
SB_MA_9	AW27
SB_MA_10	AV24
SB_MA_11	BA27
SB_MA_12	AY27
SB_MA_13	AR23
SB_RAS#	AU23
SB_RCVENIN#	AK16
SB_RCVENOUT#	AK18
SB_WE#	AR27

M_B_BS#0	15	M_B_BS#0
M_B_BS#1	15	M_B_BS#1
M_B_BS#2	15	M_B_BS#2
M_B_CAS#	15,16	M_B_CAS#
M_B_DM[0..7]	15	M_B_DM[0..7]
M_B_DQS[0..7]	15	M_B_DQS[0..7]
M_B_DQS#[0..7]	15	M_B_DQS#[0..7]
M_B_A[0..13]	15	M_B_A[0..13]
M_B_RAS#	15,16	M_B_RAS#
M_B_WE#	15,16	M_B_WE#

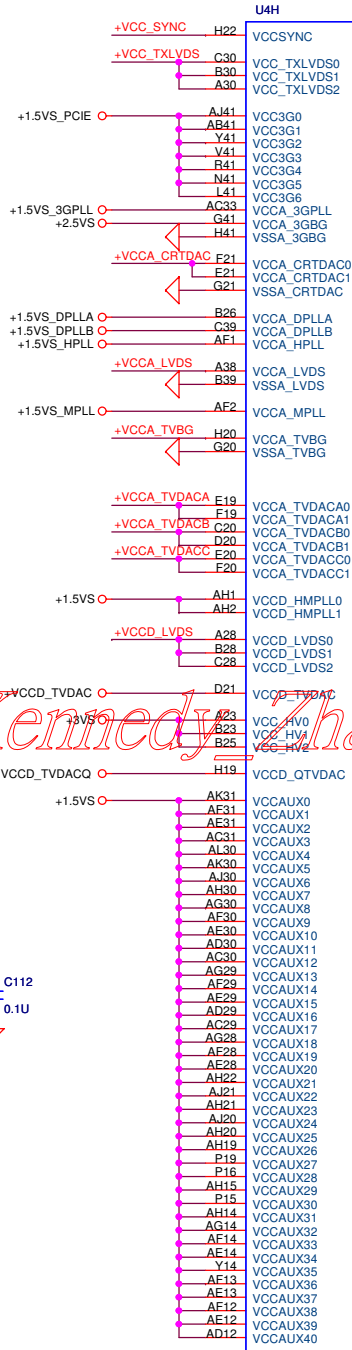
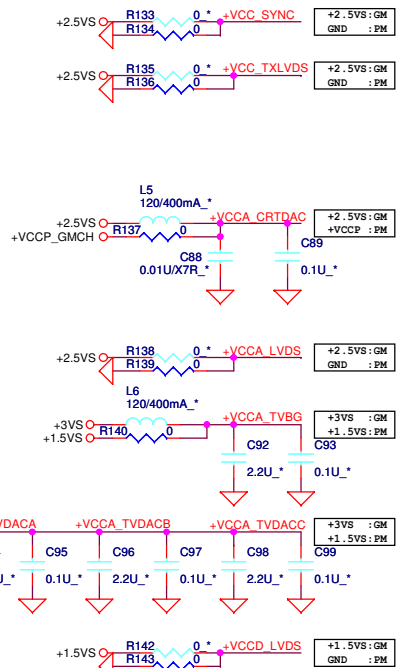
Kennedy_Zhao



NOTE: 0.1uF caps in 1.5SxPLL need to be located as edge caps within 200 mils.

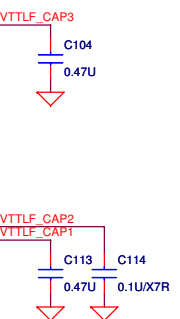
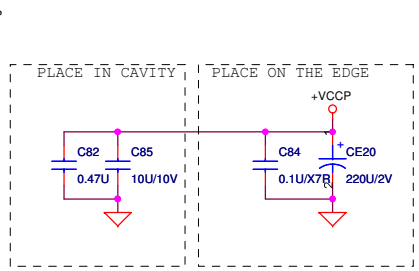
NOTE: 0.1uF CAPS USED IN +1.5VS, +3.3VS +2.5VS should be placed within 200 mils of edge.

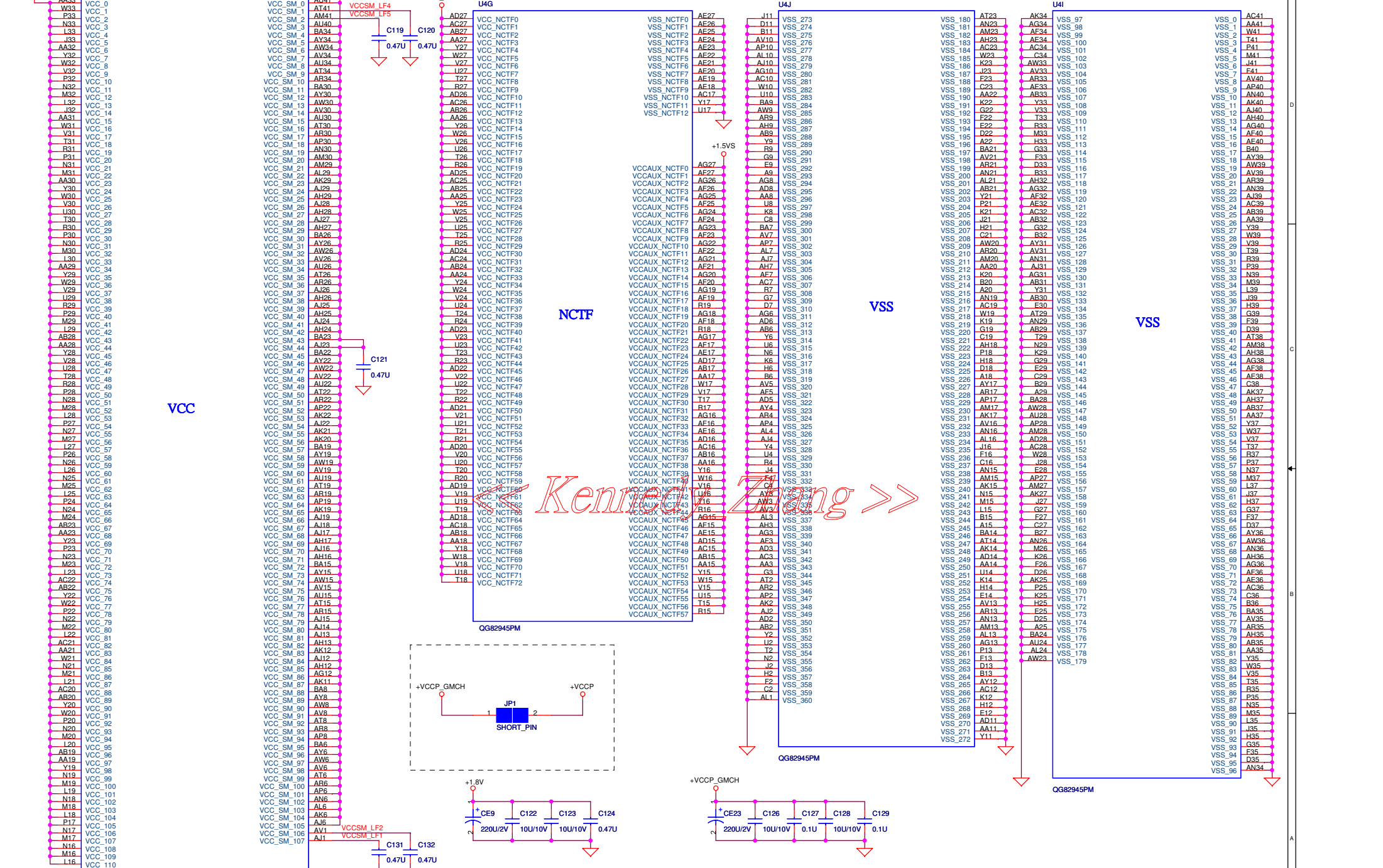
+1.5VS	+1.5VS	5, 9, 12, 17, 23, 31, 32, 38, 52
+2.5VS	+2.5VS	17, 19, 38, 54
+3VS	+3VS	6, 7, 9, 13, 14, 15, 17, 18, 19, 22, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 36, 37, 38, 39, 41, 50, 52, 60, 61
+VCCP	+VCCP	4, 5, 6, 8, 12, 20, 23, 52

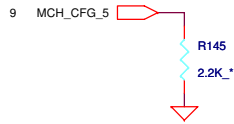


POWER

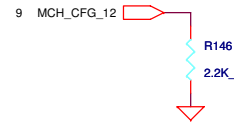
<< Kennedy Zhang >>



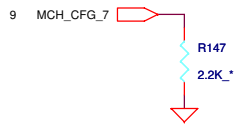




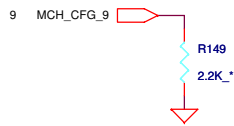
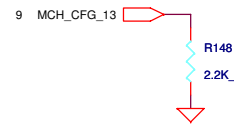
CFG5 : DMI STRAP
 LOW = DMI X 2
HIGH = DMI X 4 (Default)



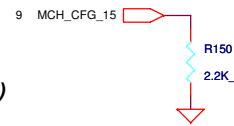
CFG[13:12] : GMCH TEST MODE SELECT
 00 = Partial CLK gating disable
 01 = XOR Mode Enable
 10 = ALL Z Mode Enable
11 = NORMAL OPERATION (Default)



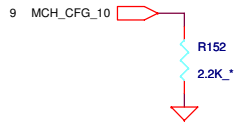
CFG7 : CPU STRAP
 LOW = RESERVED
HIGH = Mobile Yonah CPU (Default)



CFG9 : PCIE GRAPHIC LANE
 LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



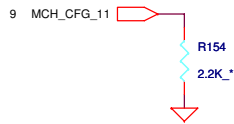
CFG15 : ICH RESET Disable
 LOW = ICH RESET Disabled
HIGH = Normal Operation (Default)



CFG10 : HOST PLL VCO SELECT
 LOW = RESERVED
HIGH = MOBILITY (Default)



CFG16 : FSB Dynamic ODT
 LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)

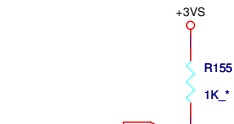


CFG11 : PSB 4x CLK ENABLE
 LOW = 4X ENABLED
HIGH = 8X ENABLED (Default)



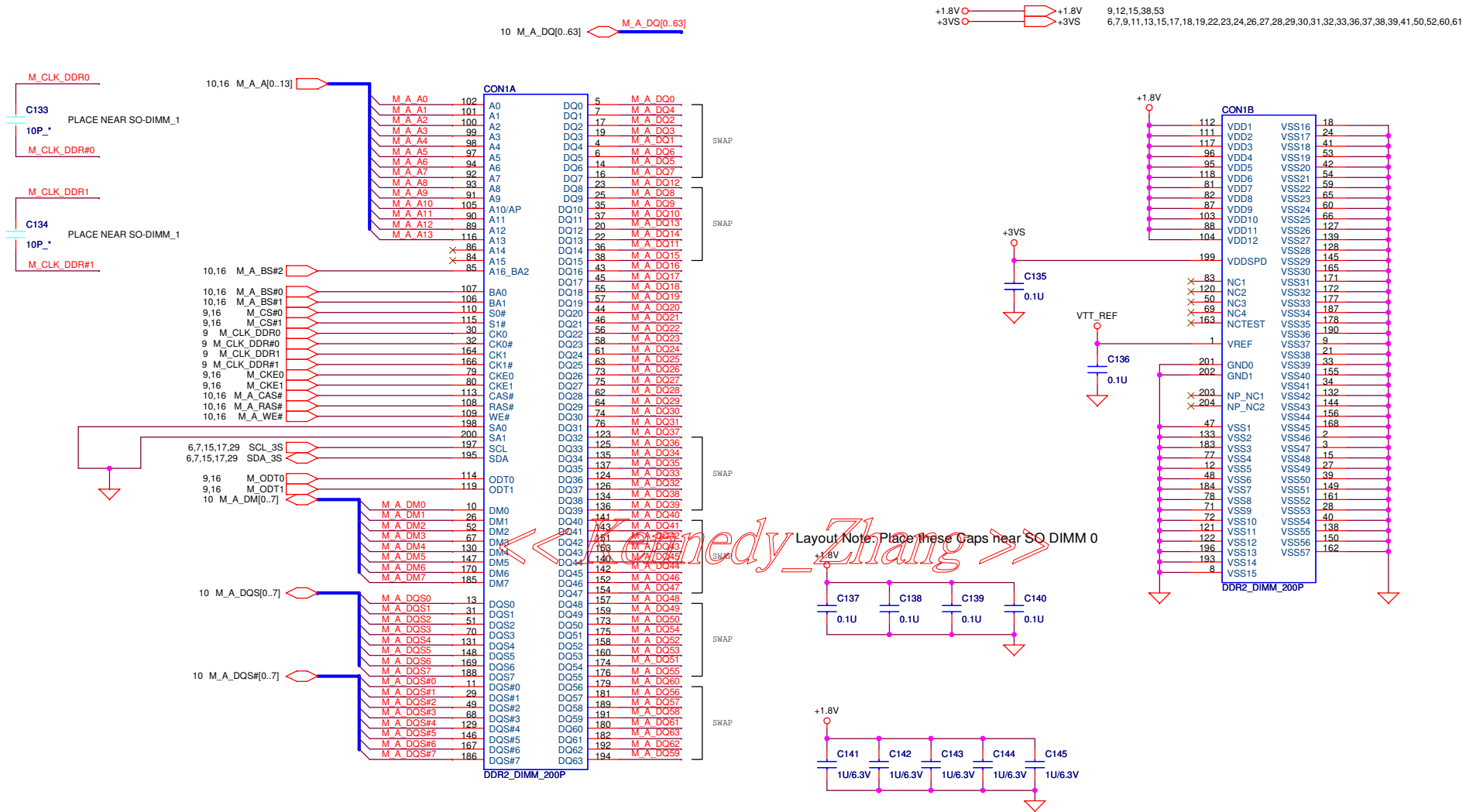
CFG18 : GMCH Core Voltage Level
LOW = 1.05V (Default)
 HIGH = 1.5V

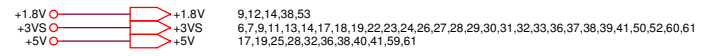
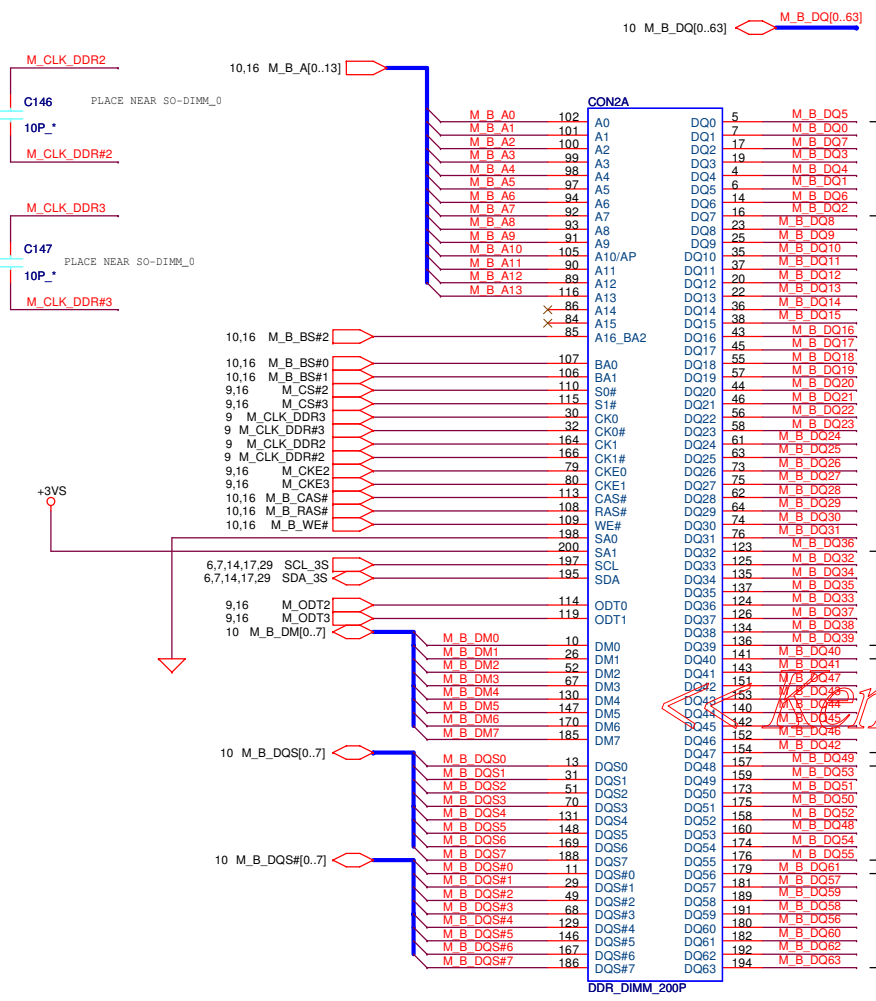
CFG[17..3] have internal pullup resistors.
 CFG[19..18] have internal pulldown resistors.
 SDVOCRTL_DATA has internal pulldown resistors.



CFG19 : DMI LANE REVERSAL
LOW = NORMAL (Default)
 HIGH = LANES REVERSED

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SWAP

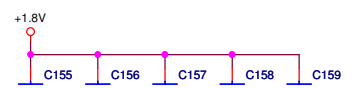
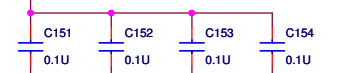
SWAP

SWAP

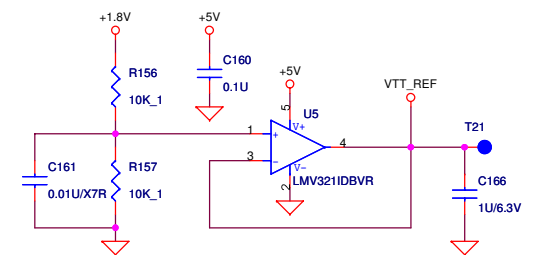
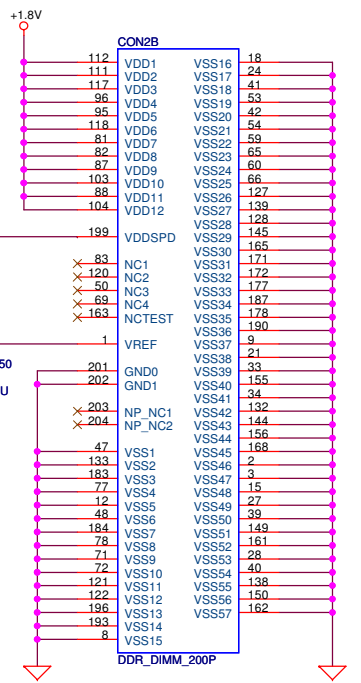
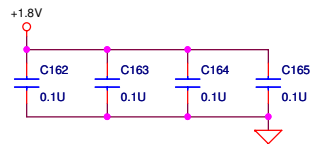
SWAP

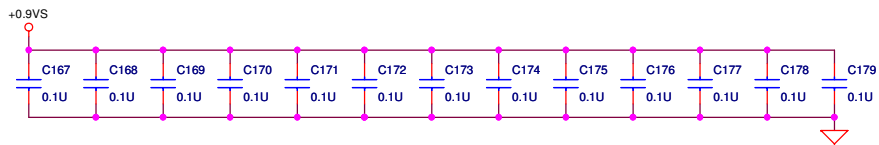
Kennedy Zhang

Layout Note: Place these Caps near SO DIMM 0

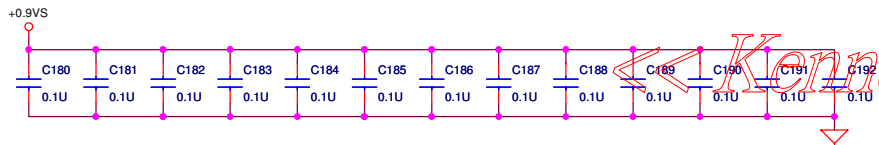


Layout Note: Place these High-Freq decoupling Caps near the GMCH



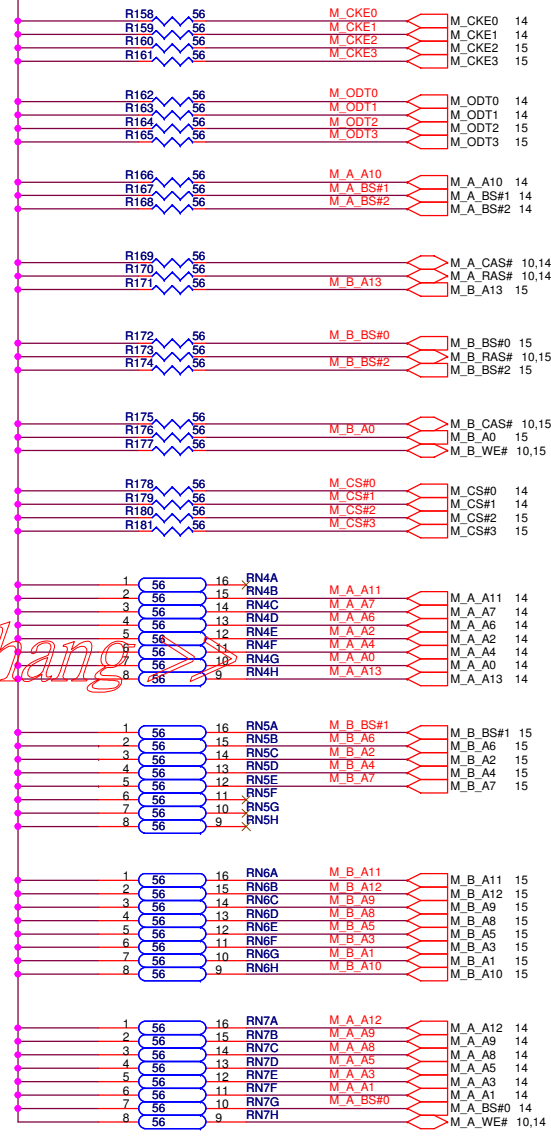


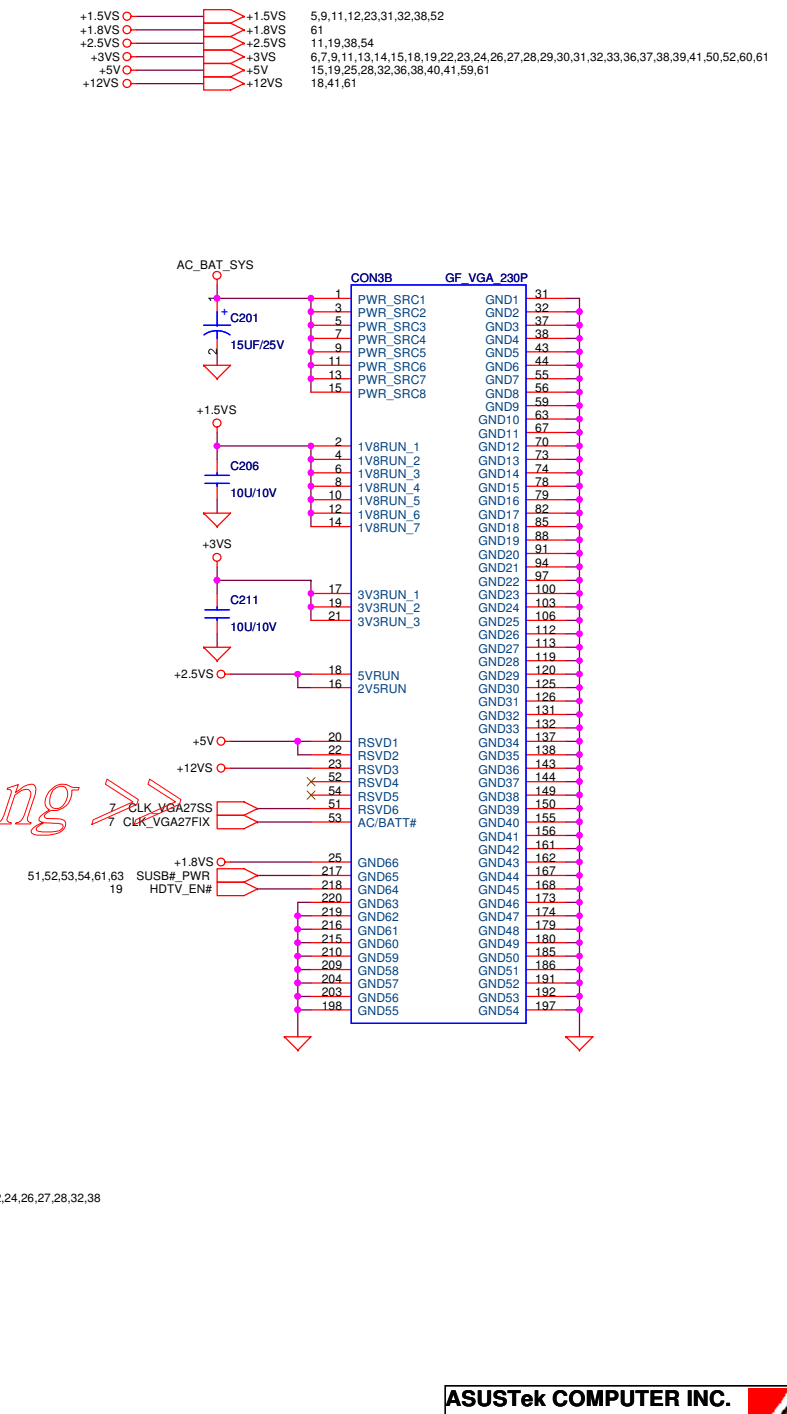
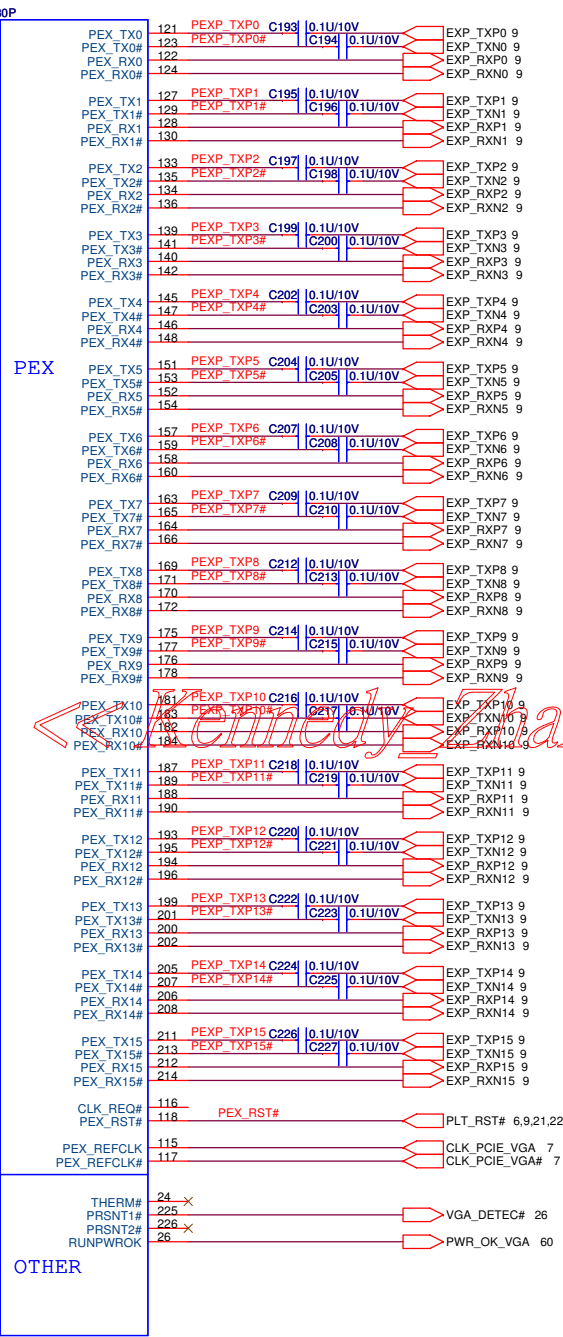
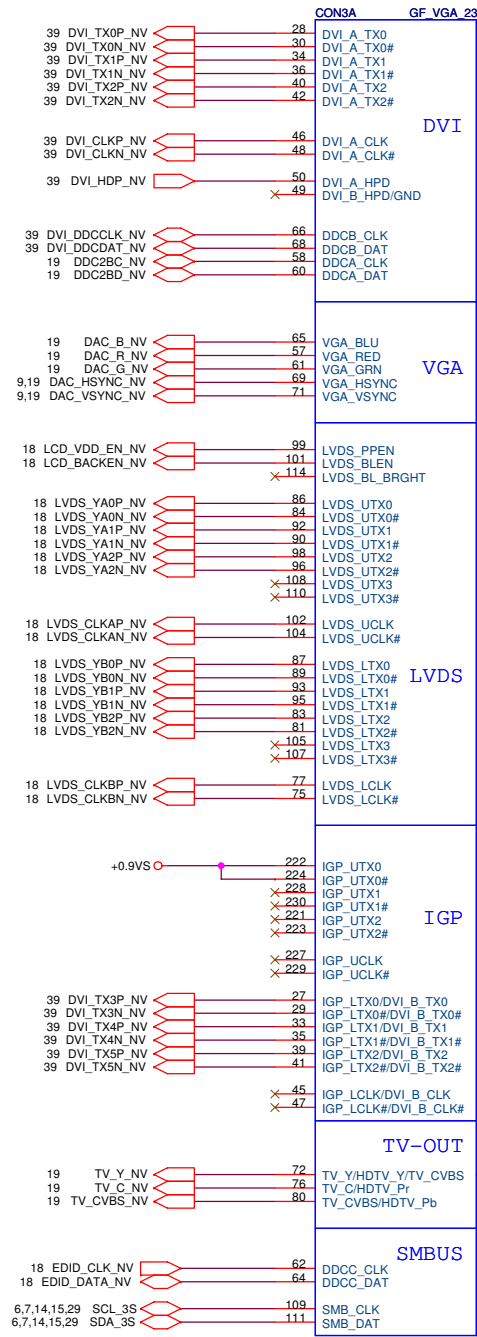
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



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+0.9VS **SWAPPED** +0.9VS 17.53





ASUSTek Computer Inc. Logo

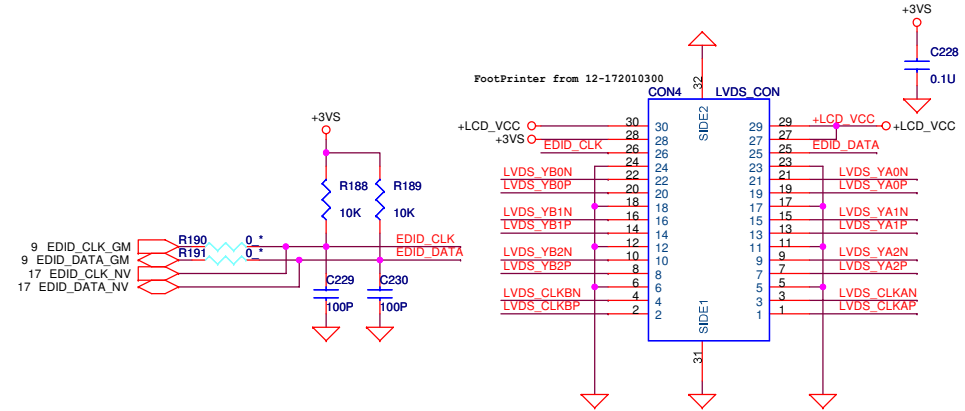
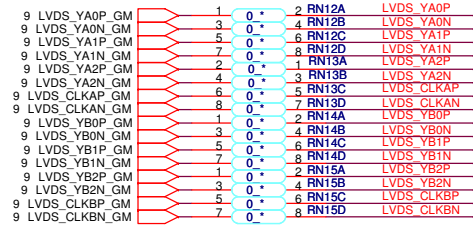
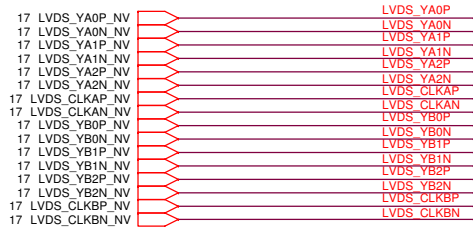
ASUSTek COMPUTER INC.

4 FL., No.150, Li-Te Rd., Pailou, Taipei, Taiwan, ROC

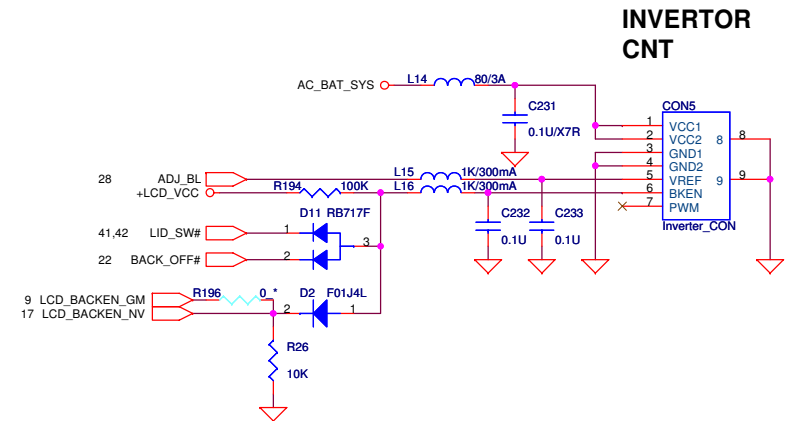
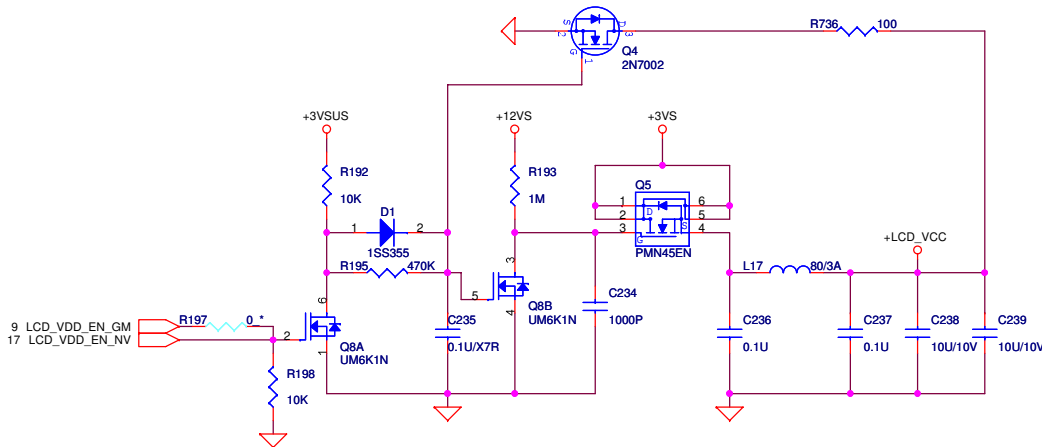
VGA CONN

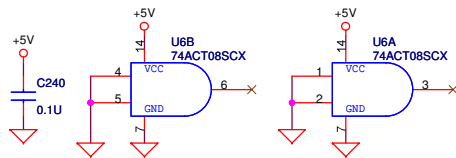
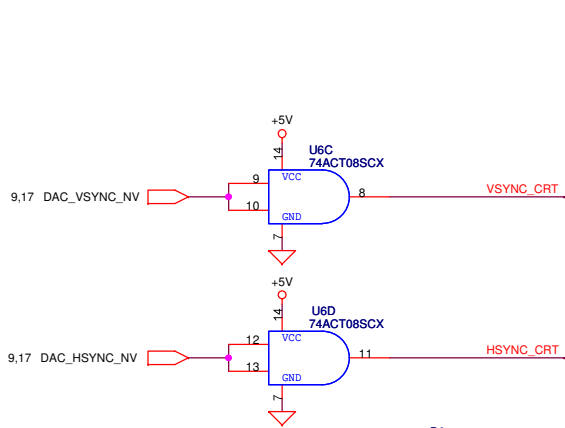
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 Date: Thursday, September 07, 2006
 Sheet: 17 of 63
 Rev: 2.0

+3VS ○ → +3VS 6,7,9,11,13,14,15,17,19,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61
 +3VSUS ○ → +3VSUS 21,22,23,28,29,30,42,51
 +12VS ○ → +12VS 17,41,61

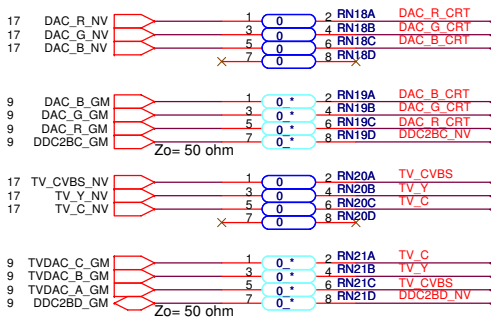
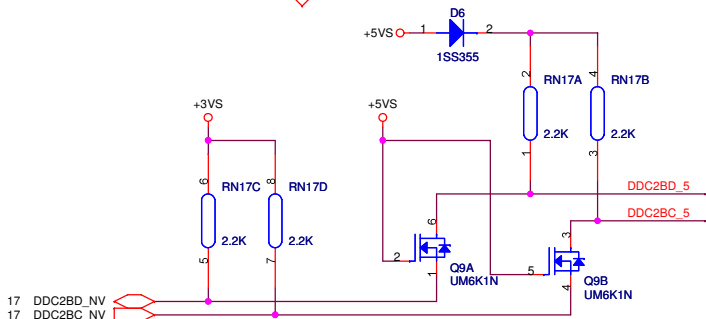
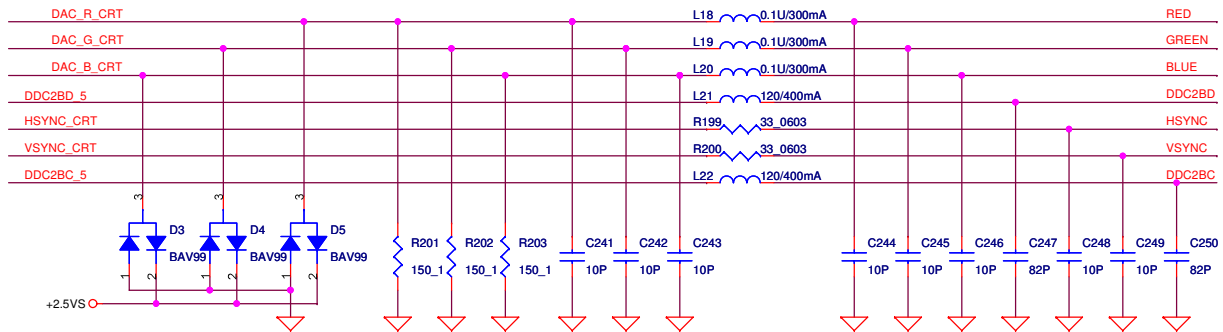


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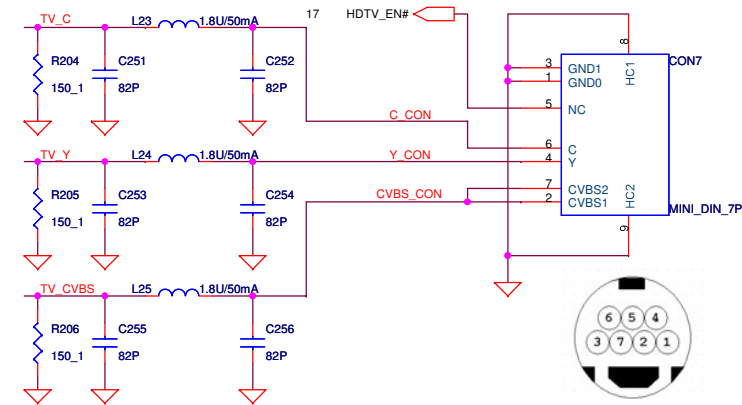
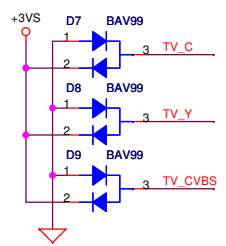
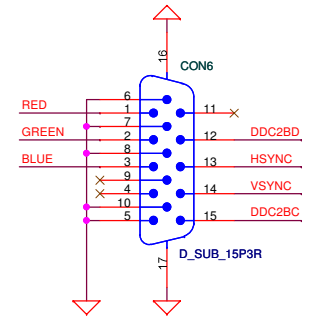




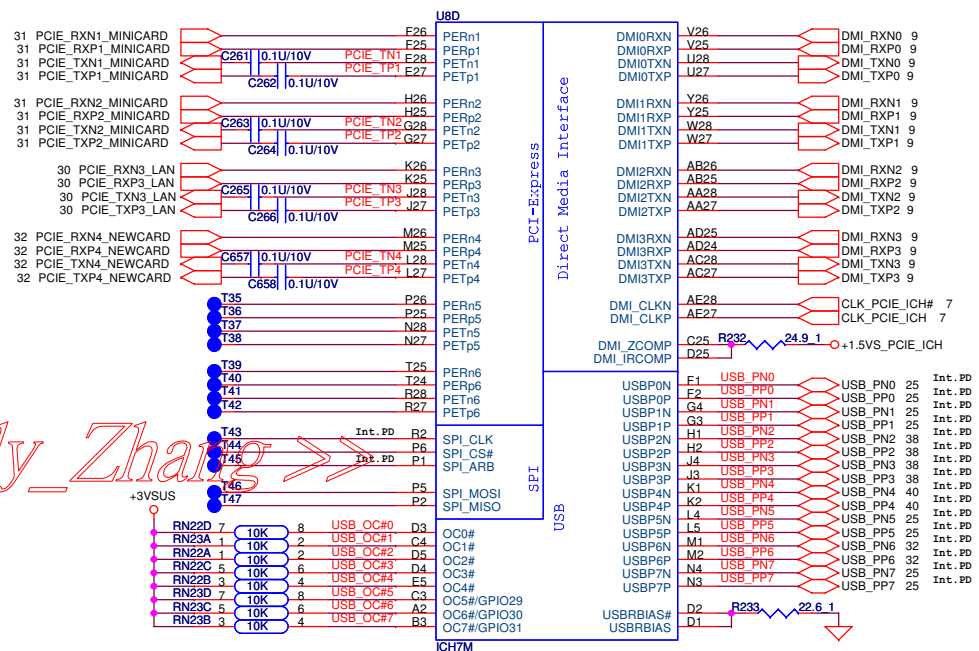
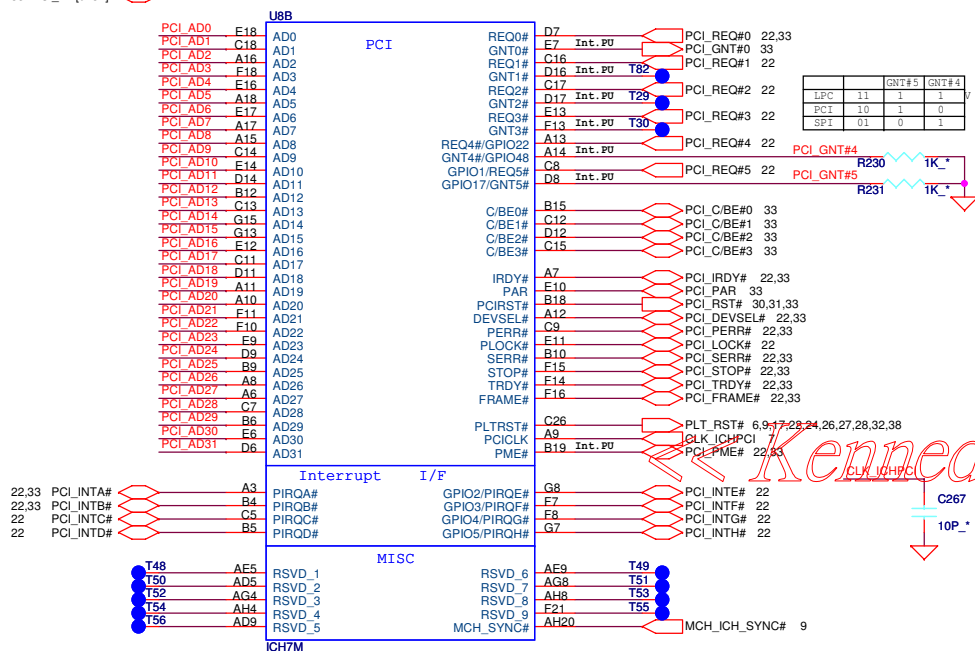
+2.5VS	11, 17, 38, 54
+3VS	6, 7, 9, 11, 13, 14, 15, 17, 18, 22, 23, 24, 26, 27, 28, 29, 30, 31, 32, 33, 36, 37, 38, 39, 41, 50, 52, 60, 61
+5V	15, 17, 25, 28, 32, 36, 38, 40, 41, 59, 61
+5VS	22, 23, 24, 28, 29, 36, 37, 38, 39, 40, 41, 50, 61



<< Kennedy_Zhang >>



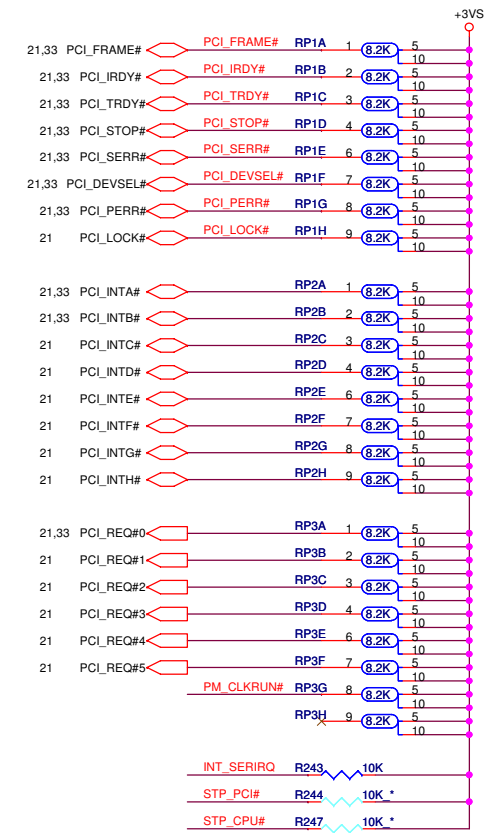
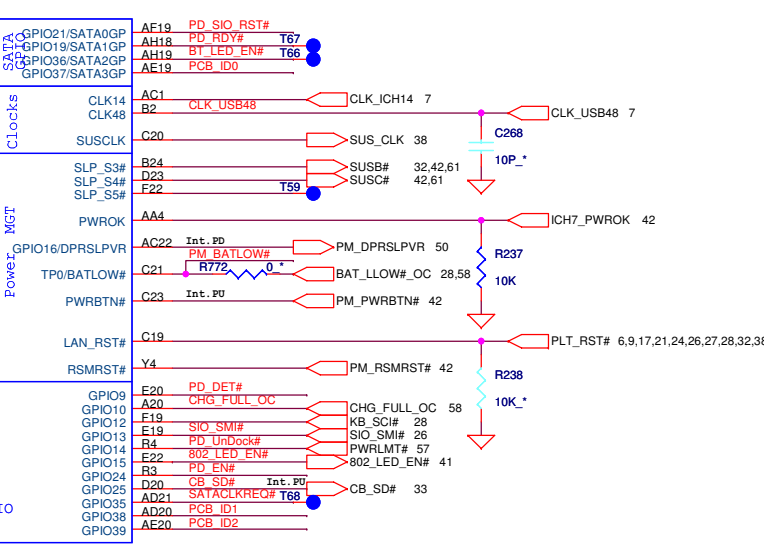
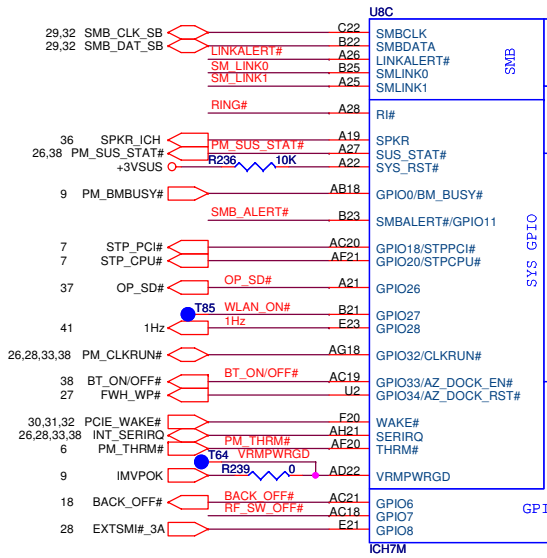
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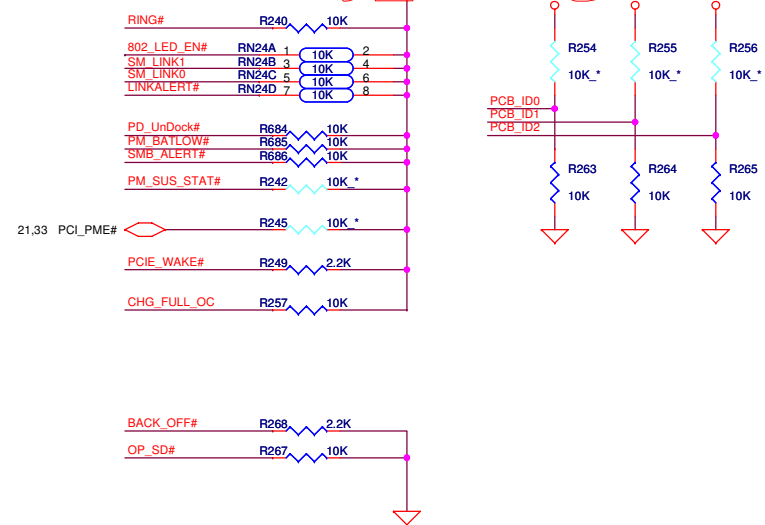
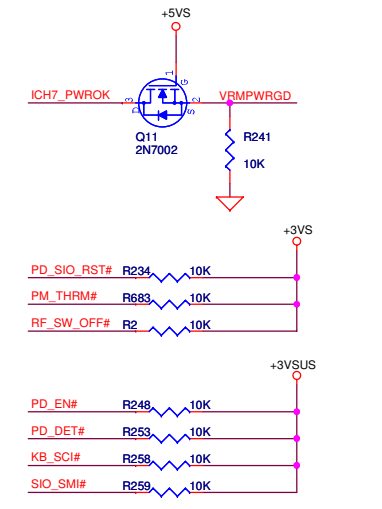
Kennedy_Zhang

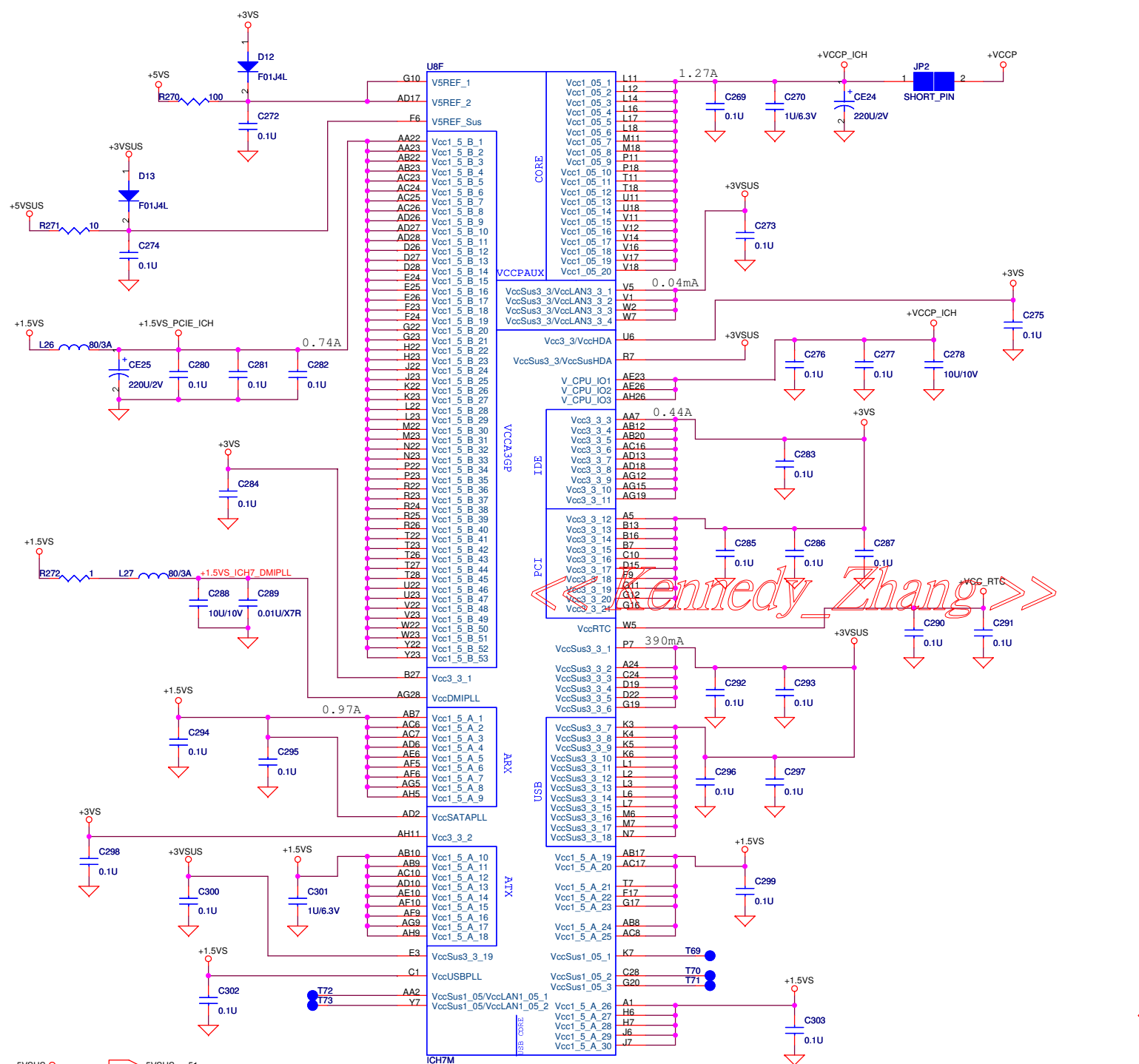
+3VSUS <--> +3VSUS 18,22,23,28,29,30,42,51

+3VS ○ → +3VS 6,7,9,11,13,14,15,17,18,19,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61
 +5VS ○ → +5VS 19,23,24,28,29,36,37,38,39,40,41,50,61
 +3VSUS ○ → +3VSUS 18,21,23,28,29,30,42,51



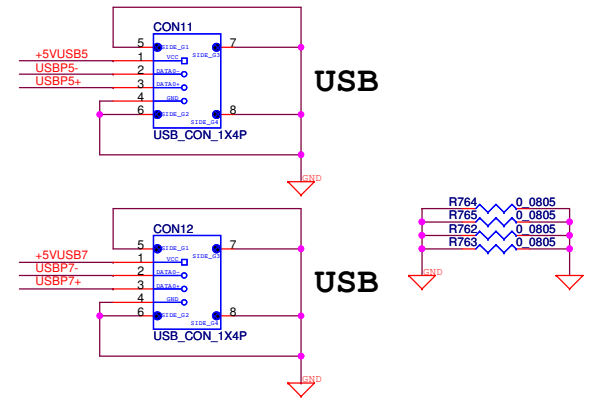
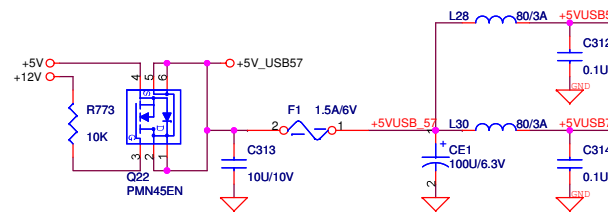
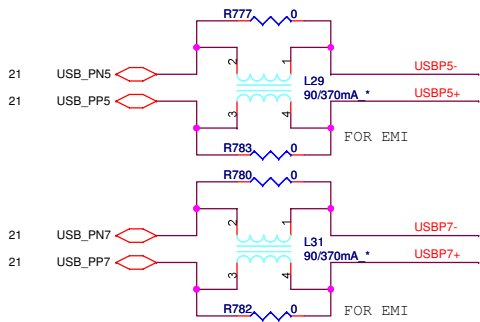
<< Kennedy Zhang >>



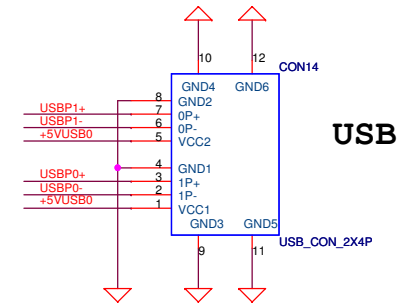
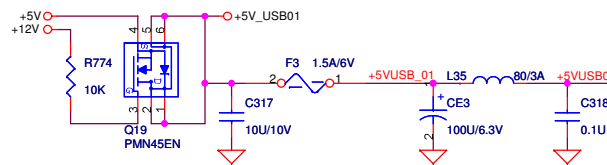
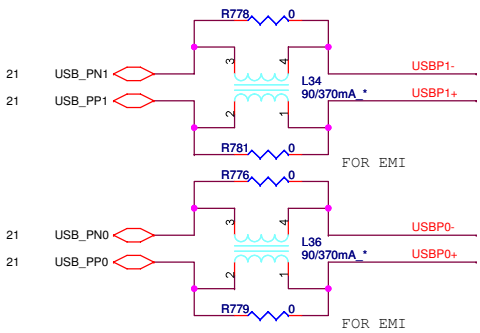


U8E	P28
A4	Vss1
A23	Vss2
B1	Vss3
B8	Vss4
B14	Vss5
B17	Vss6
B20	Vss7
B26	Vss8
B28	Vss9
C2	Vss10
C6	Vss11
C27	Vss12
D10	Vss13
D13	Vss14
D18	Vss15
D21	Vss16
D24	Vss17
E1	Vss18
E2	Vss19
E4	Vss20
E8	Vss21
F15	Vss22
F3	Vss23
F4	Vss24
F5	Vss25
F12	Vss26
F27	Vss27
F28	Vss28
G1	Vss29
G2	Vss30
G5	Vss31
G6	Vss32
G9	Vss33
G14	Vss34
G18	Vss35
G21	Vss36
G24	Vss37
G25	Vss38
G26	Vss39
H3	Vss40
H4	Vss41
H5	Vss42
H24	Vss43
H27	Vss44
H28	Vss45
J1	Vss46
J2	Vss47
J5	Vss48
J24	Vss49
J25	Vss50
J26	Vss51
K24	Vss52
K27	Vss53
K28	Vss54
L13	Vss55
L15	Vss56
L24	Vss57
L25	Vss58
L26	Vss59
M3	Vss60
M4	Vss61
M5	Vss62
M12	Vss63
M13	Vss64
M14	Vss65
M15	Vss66
M16	Vss67
M17	Vss68
M24	Vss69
M27	Vss70
N1	Vss71
N2	Vss72
N5	Vss73
N6	Vss74
N11	Vss75
N12	Vss76
N13	Vss77
N14	Vss78
N15	Vss79
N16	Vss80
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Vss194	Vss194

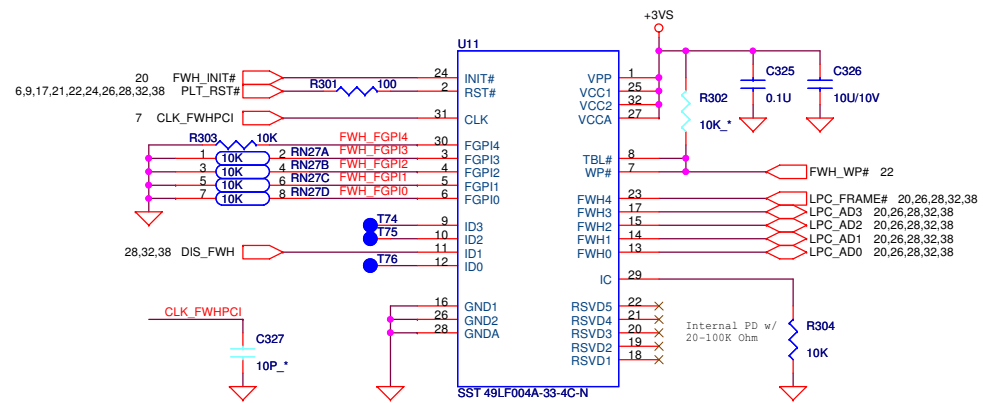
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+3VSUS	18,21,22,28,29,30,42,51
+5VS	19,22,24,28,29,36,37,38,39,40,41,50,61
+3VS	6,7,9,11,13,14,15,17,18,19,22,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61
+1.5VS	5,9,11,12,17,31,32,38,52
+VCCP	4,5,6,8,11,12,20,52



<< Kennedy_Zhang >>

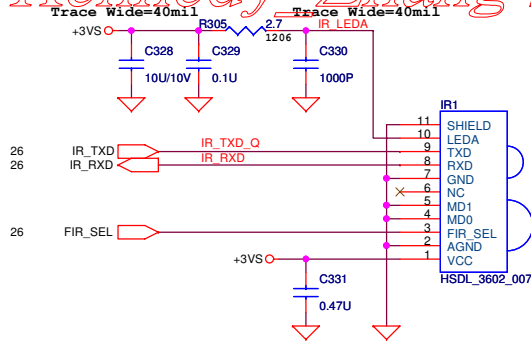


+5V +5V 15,17,19,28,32,36,38,40,41,59,61



PLCC32 Socket Part Number :
12G043400324
Graphics from:
05-001005111

<< Kennedy Zhang >>

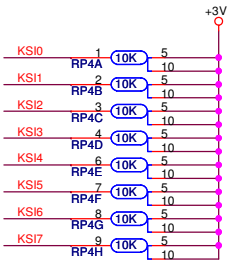
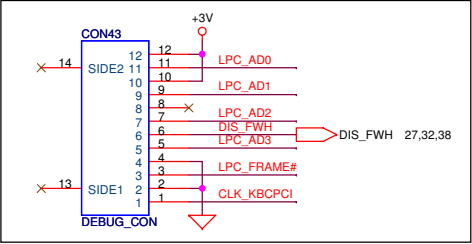


+3VS +3VS 6,7,9,11,13,14,15,17,18,19,22,23,24,26,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61

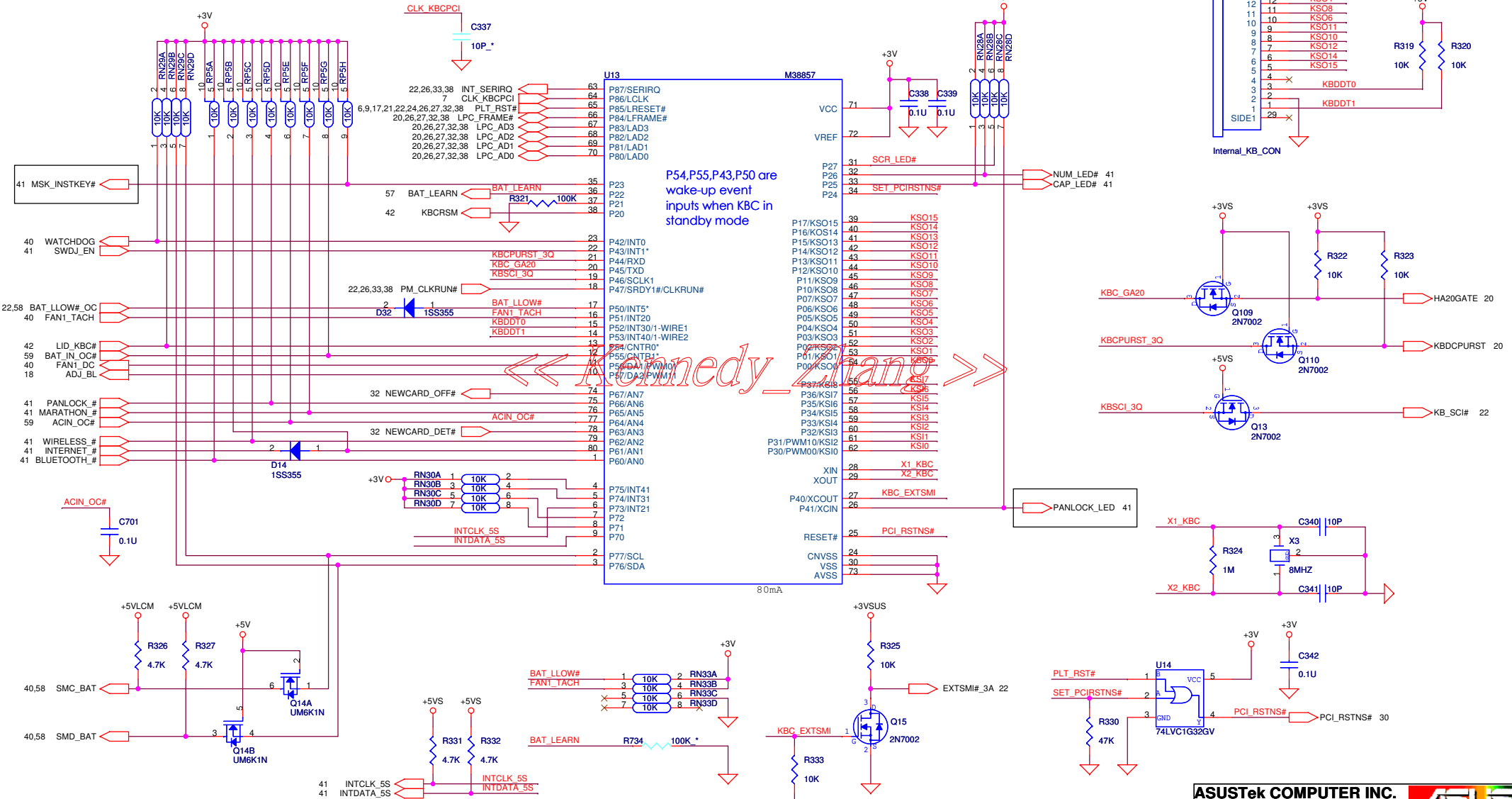
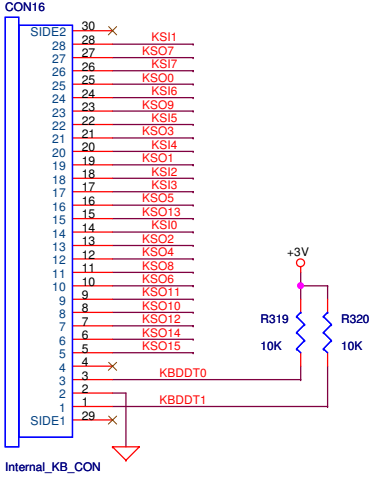
P2.1 Low : Power Button Override disable
Input Event only at P54, P55, P60 - P67

P50, P43, P54, P55 are wake-up event inputs when KBC in standby mode

EC should set OP_SD low in S3, keep from leakage.



KBDDT1	KBDDT0	Matrix
1	1	US
1	0	UK
0	1	JP



P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode

« Annedy /iang »

+3V	+3V	30,31,32,34,37,38,42,54,61
+3VS	+3VS	6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,29,30,31,32,33,36,37,38,39,41,50,52,60,61
+3VSUS	+3VSUS	18,21,22,23,29,30,42,51
+5V	+5V	15,17,19,25,32,36,38,40,41,59,61
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+5VLCM	+5VLCM	57,58,59,60

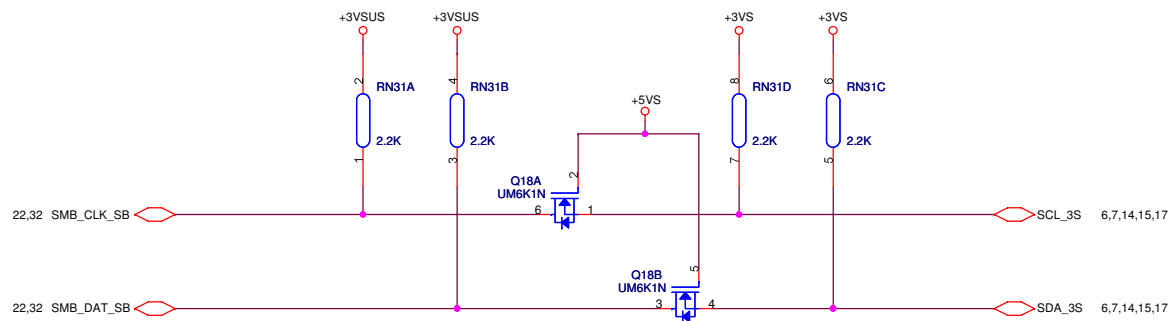
ASUSTeK COMPUTER INC.

4 FL.No.150, Li-Te Rd.,Pailou, Taipei,Taiwan, ROC

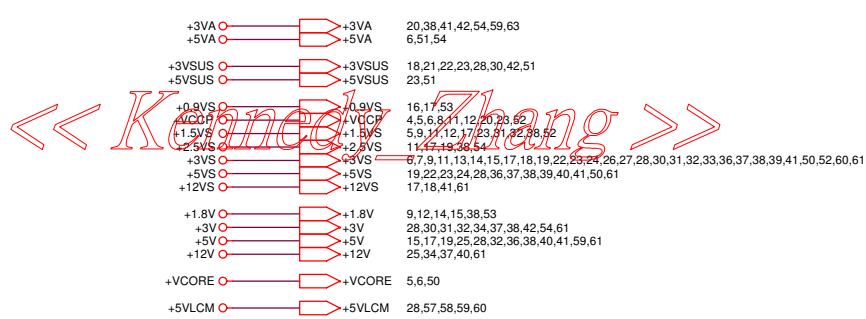
Title: **KBC 38857**

Size Custom	Document Number A8J/F	Rev 2.0
Date: Thursday, September 07, 2006	Sheet 28 of 63	

ICH7-M



Termal Sensor,
Clock Generator
DDR2 SO-DIMM
TPM



ASUSTek COMPUTER INC.



4 FL_No.150, Li-Te Rd., Peitou, Taipei, Taiwan, ROC

Title

SM BUS & POWER PORT

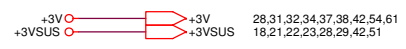
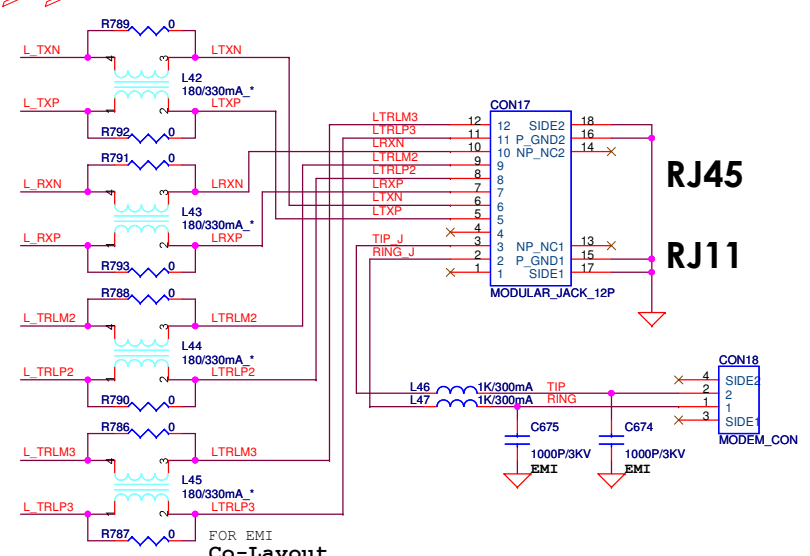
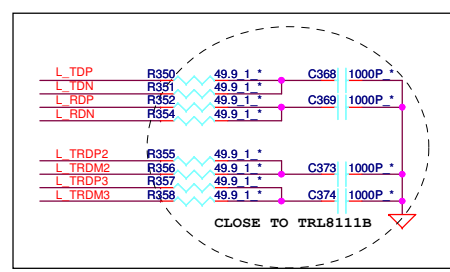
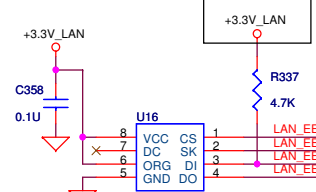
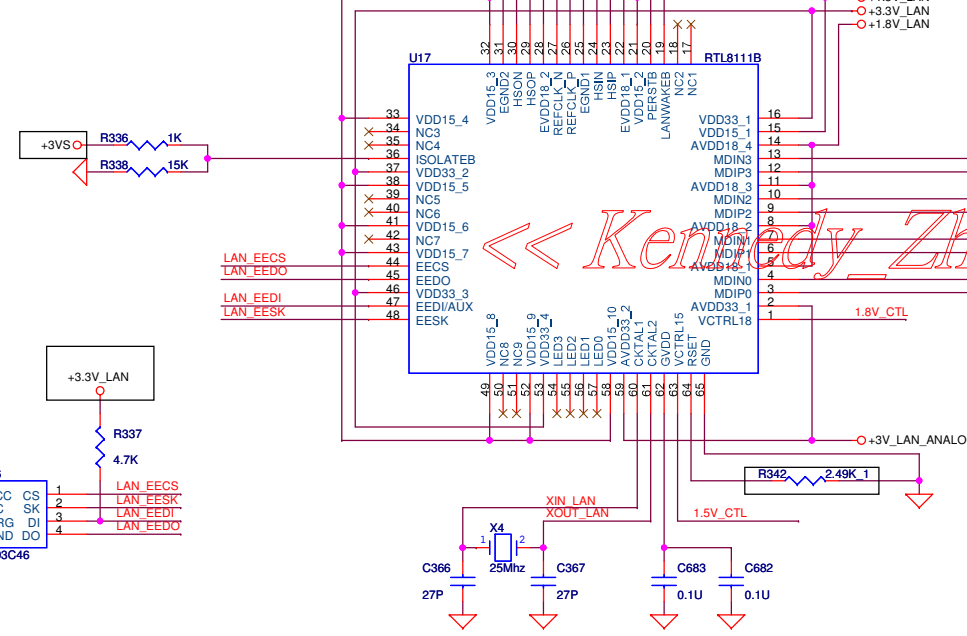
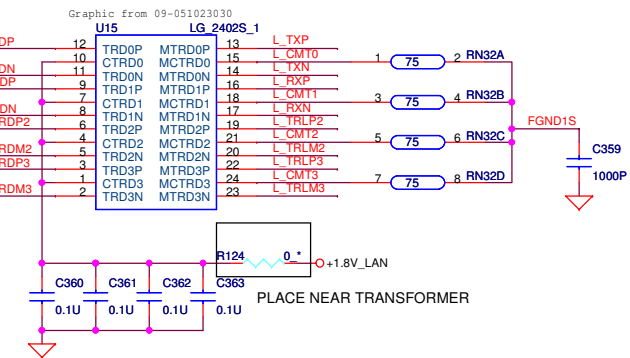
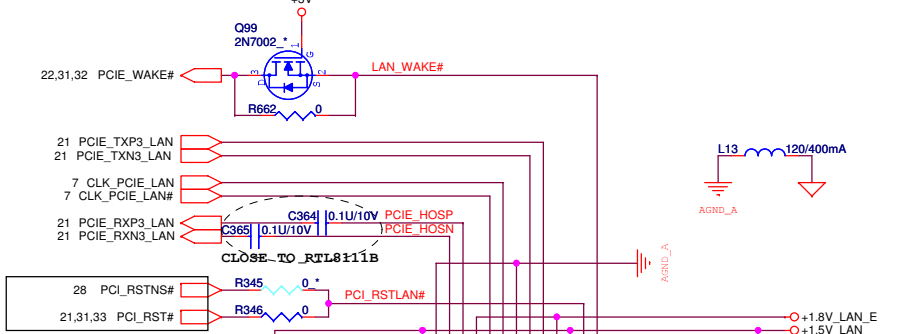
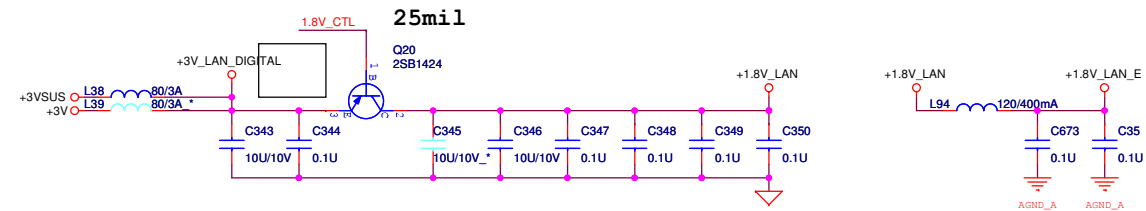
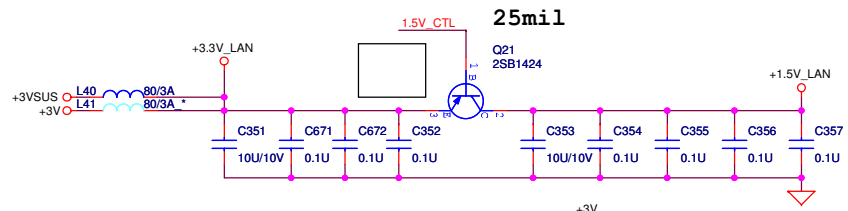
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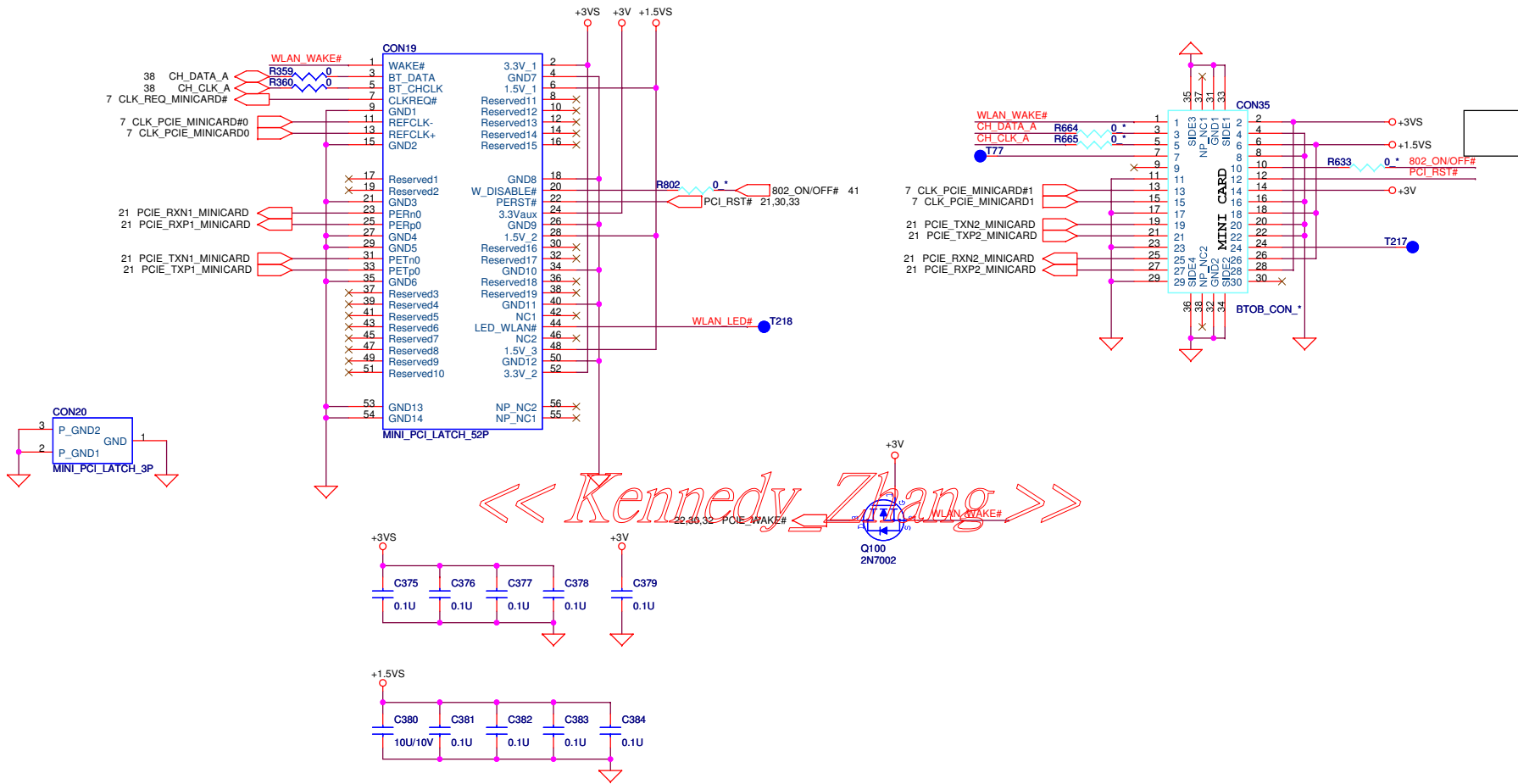
Rev
2.0

Date: Thursday, September 07, 2006

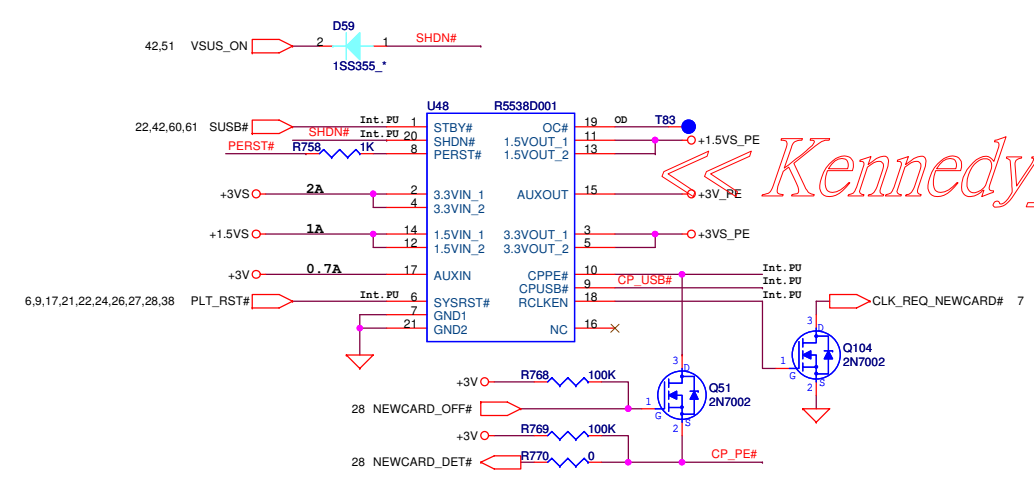
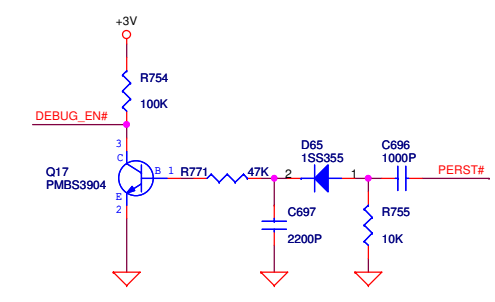
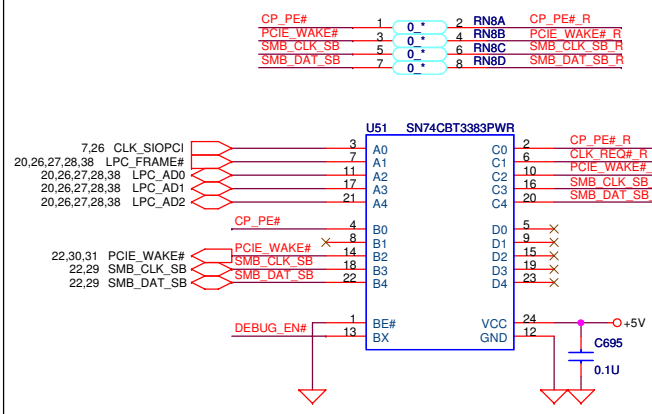
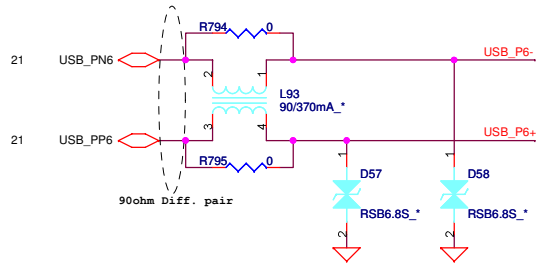
Sheet 29 of 63



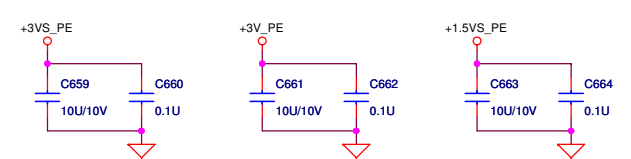
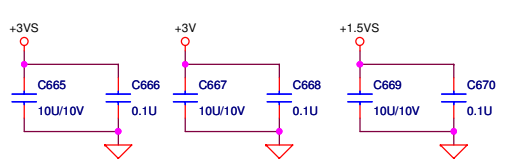
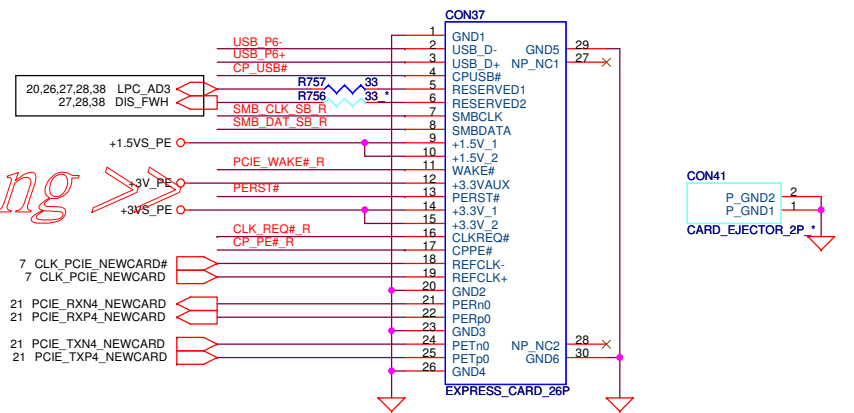
<< Kennedy_Zhang >>



+1.5VS ○ → +1.5VS 5,9,11,12,17,23,32,38,52
 +3V ○ → +3V 28,30,32,34,37,38,42,54,61
 +3VS ○ → +3VS 6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,32,33,36,37,38,39,41,50,52,60,61

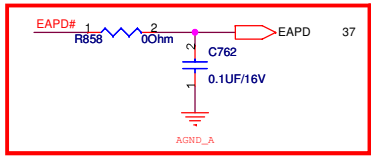
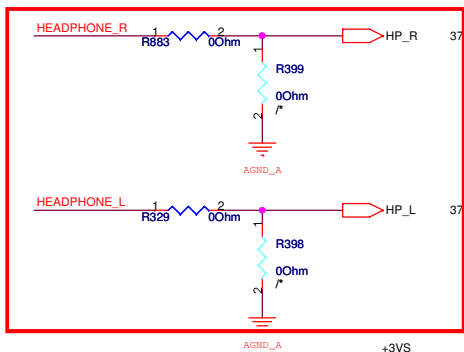


<< Kennedy_Zhang >>



- +1.5VS → 5,9,11,12,17,23,31,38,52
- +3VS → 6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,33,36,37,38,39,41,50,52,60,61
- +3V → 28,30,31,34,37,38,42,54,61

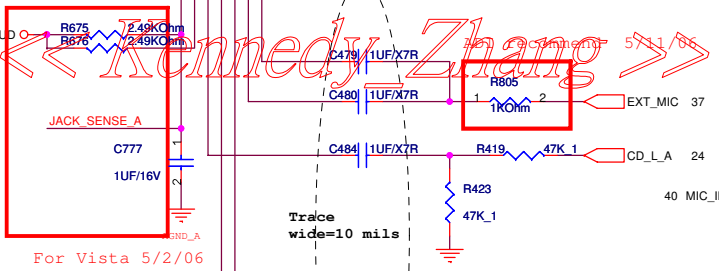
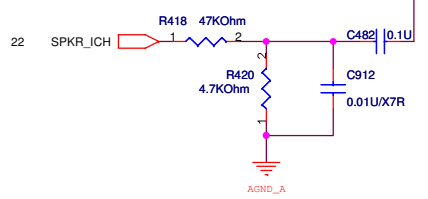
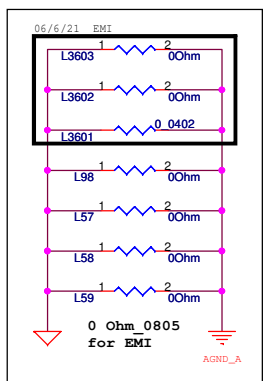
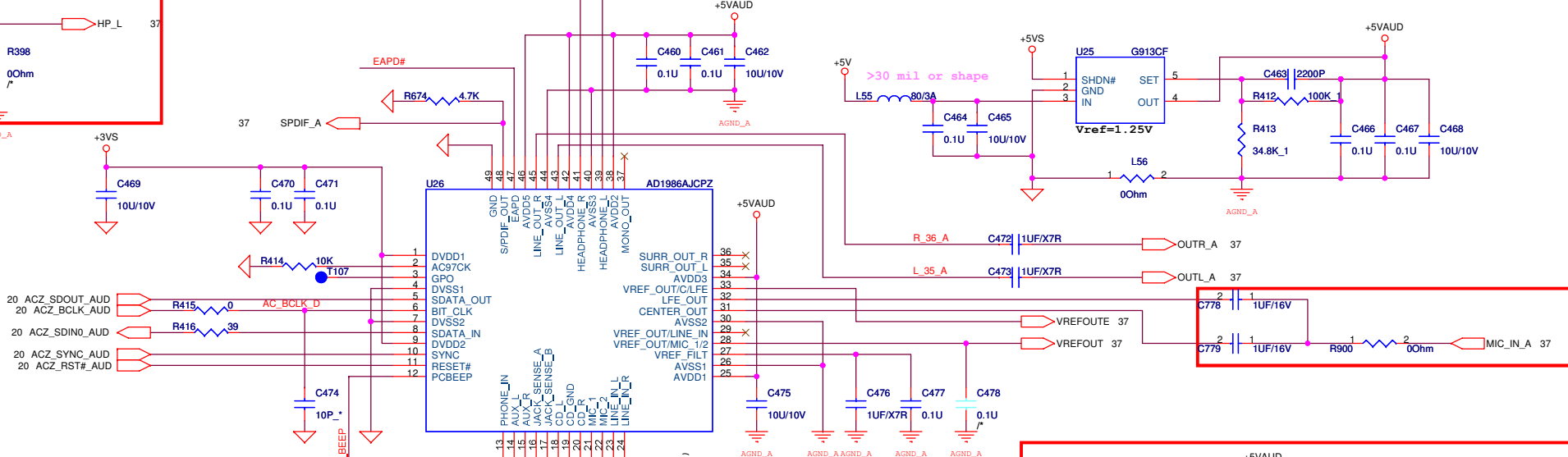
<< Kennedy_Zhang >>



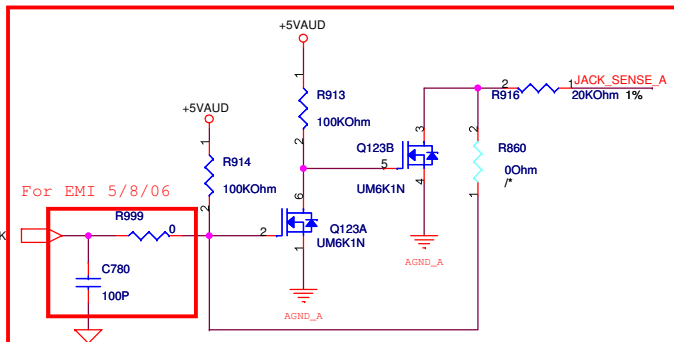
For Vista 5/2/06



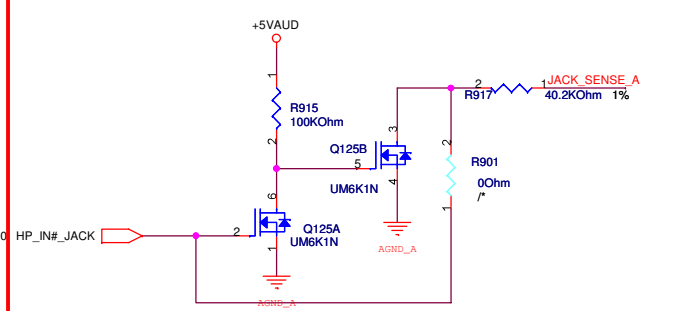
For Vista 5/2/06



For Vista 5/2/06



For EMI 5/8/06

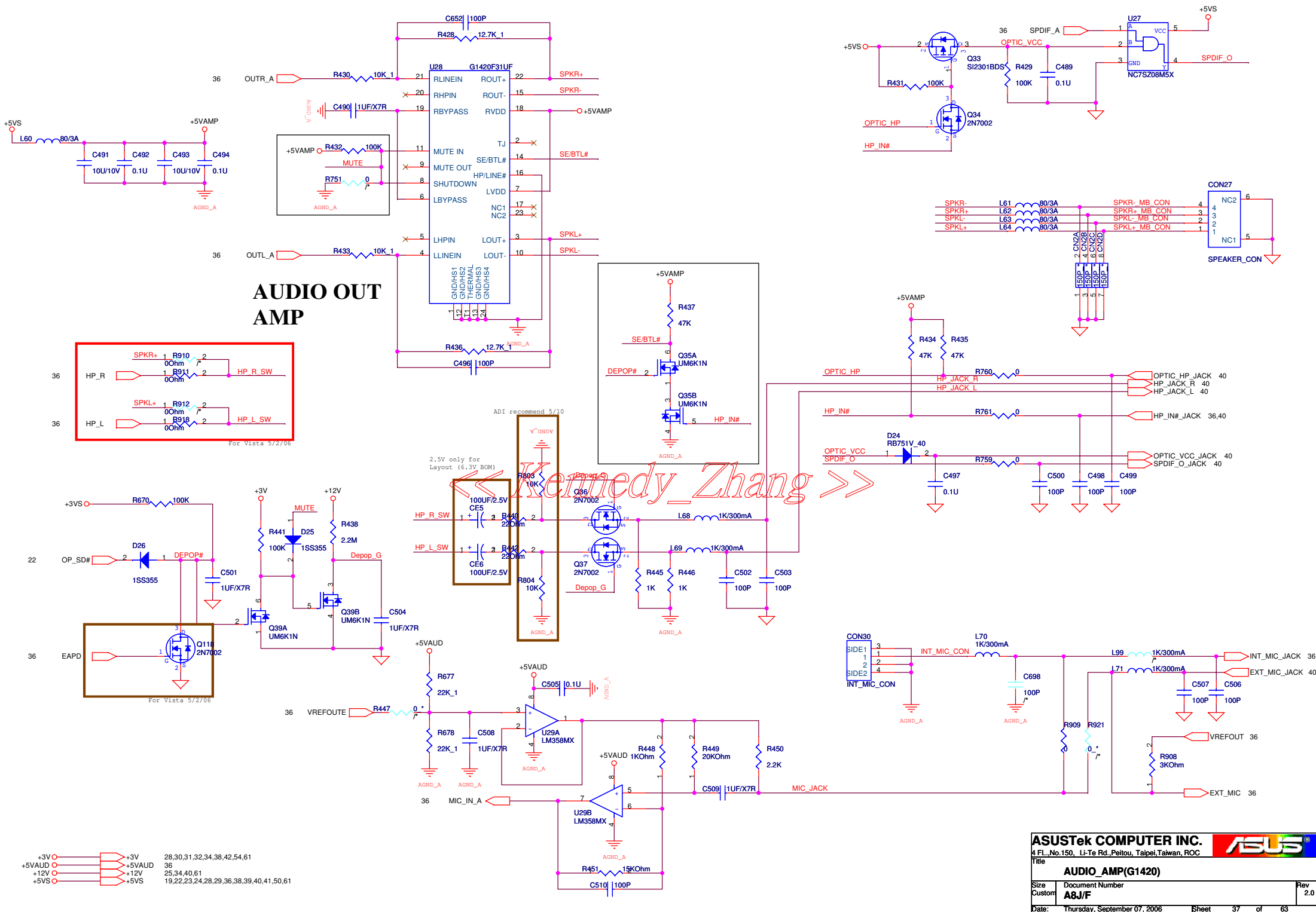


For Vista 5/2/06

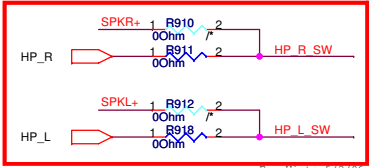
- +3VS ○ → +3VS 6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,37,38,39,41,50,52,60,61
- +5V ○ → +5V 15,17,19,25,28,32,38,40,41,59,61
- +5VS ○ → +5VS 19,22,23,24,28,29,37,38,39,40,41,50,61
- +5VAUD ○ → +5VAUD 37

« Kennedy Zhang »

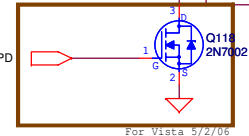
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AUDIO OUT AMP

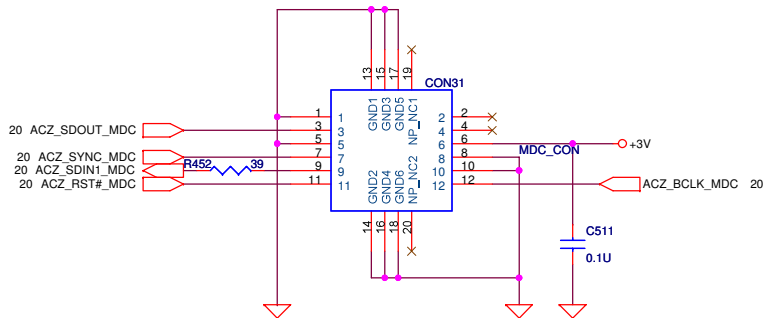


For Vista 5/2/06

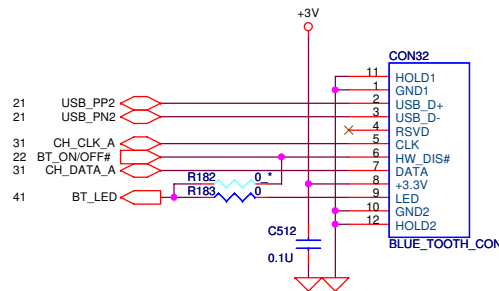


For Vista 5/2/06

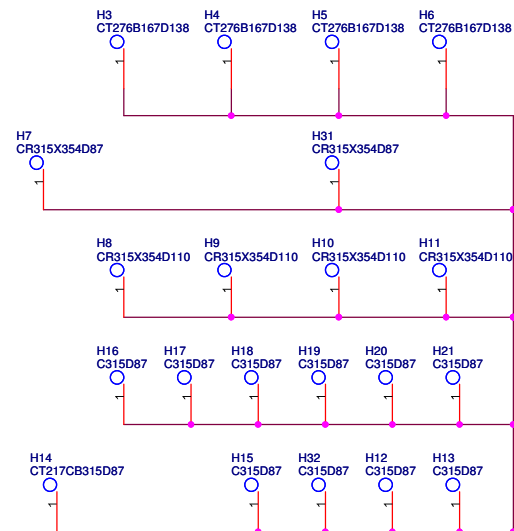
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ASUS		
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Size Custom	Document Number A8J/F	Rev 2.0
Date: Thursday, September 07, 2006	Sheet 37 of 63	



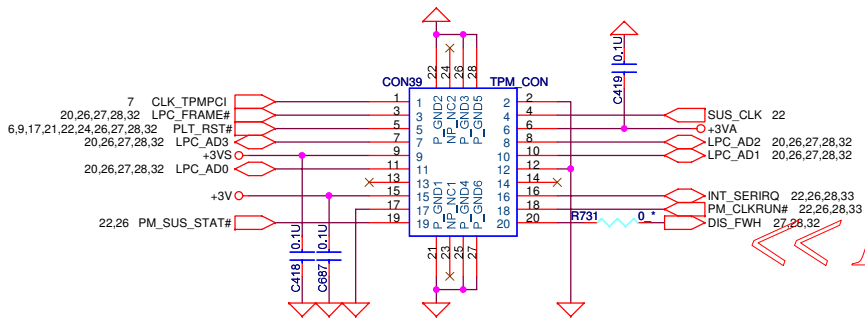
Azalia MDC MODEM CON



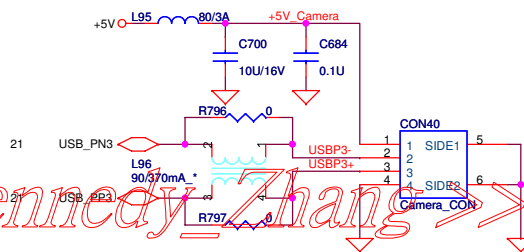
Bluetooth Module CON



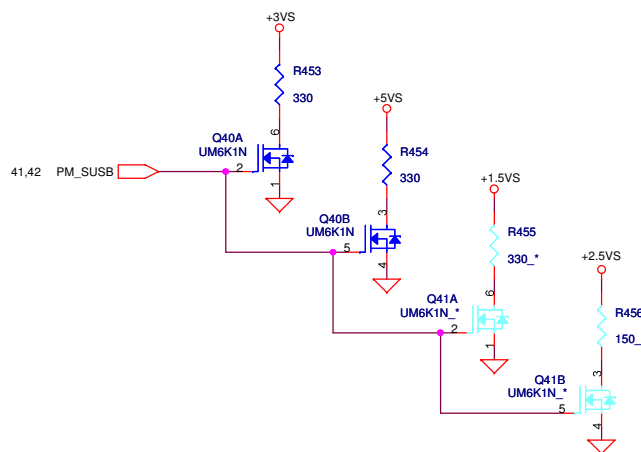
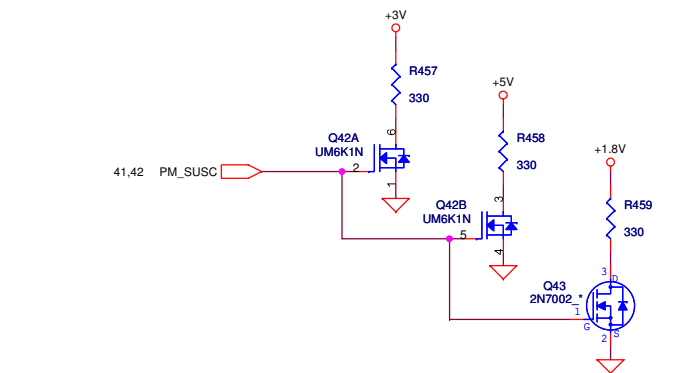
- CPU
- SCREW
- U HOLE
- SCREW
- IO Board
- MDC_NUT
- TPM_NUT
- VGA_NUT
- KB_NUT
- KEYBOARD
- FIXED HOLE



TPM Module CON

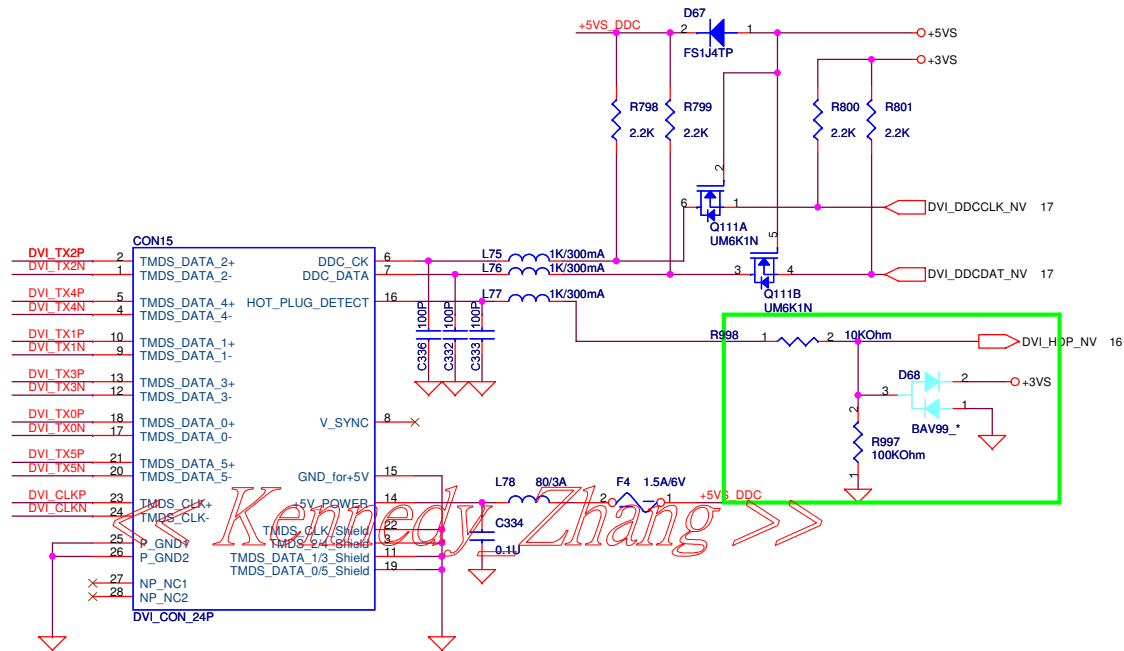
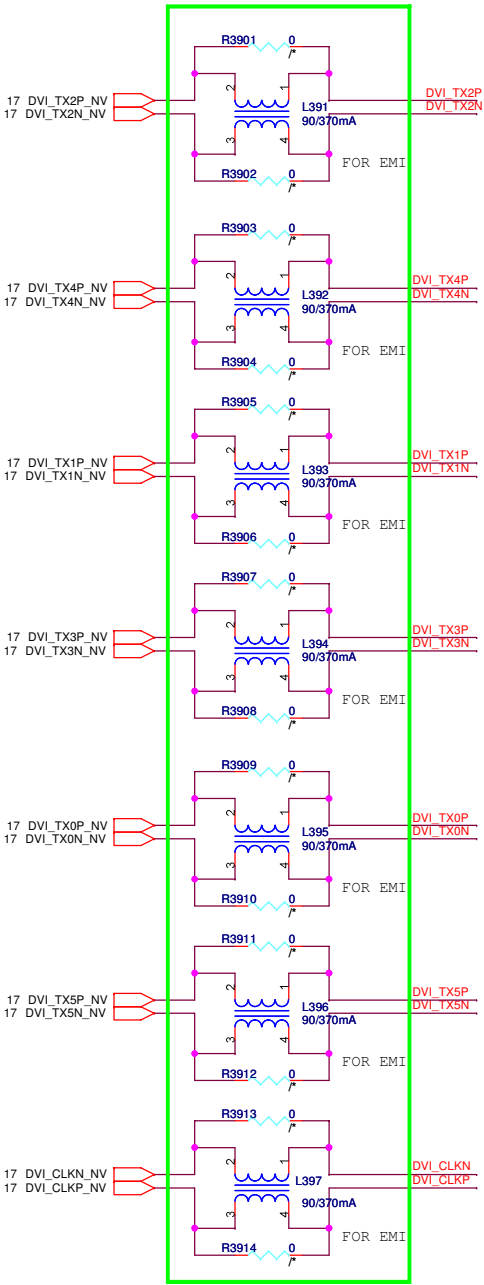


Camera Module CON



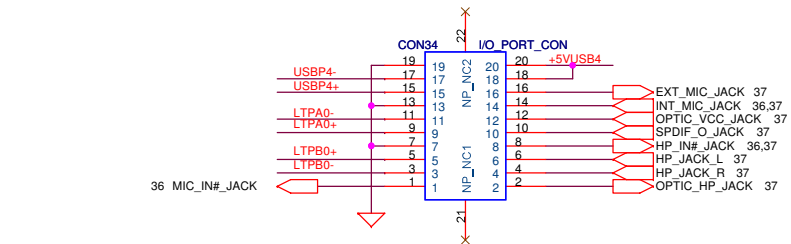
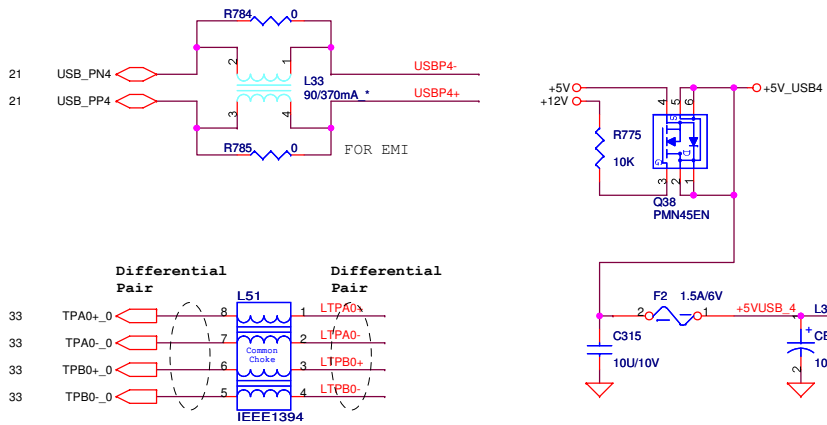
+1.5V	+1.5V	5,9,11,12,17,23,31,32,52
+1.8V	+1.8V	9,12,14,15,53
+2.5V	+2.5V	11,17,19,54
+3V	+3V	28,30,31,32,34,37,42,54,61
+3VS	+3VS	6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,39,41,50,52,60,61
+5V	+5V	15,17,19,25,28,32,36,40,41,59,61
+5VS	+5VS	19,22,23,24,28,29,36,37,39,40,41,50,61

Add DVI Choke 09G092145000
for EMI issue 2006.08.04

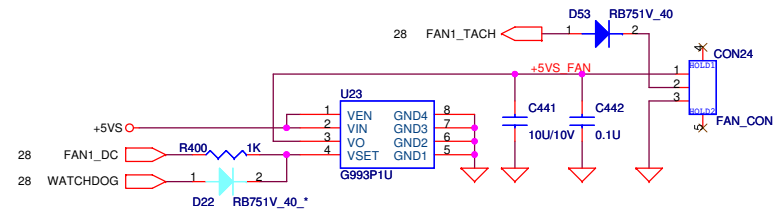
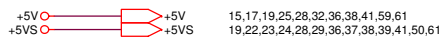


+5VS +5VS 19,22,23,24,28,29,36,37,38,40,41,50,61

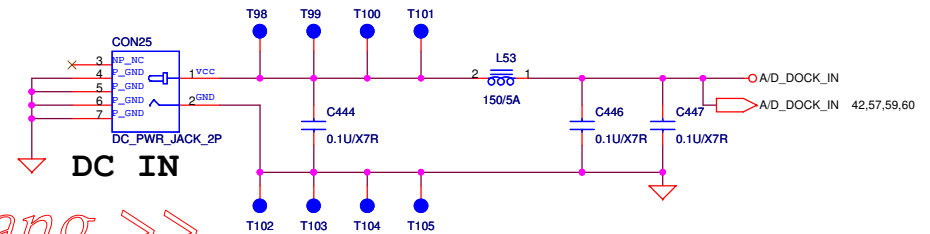
Kennedy Zhang >>



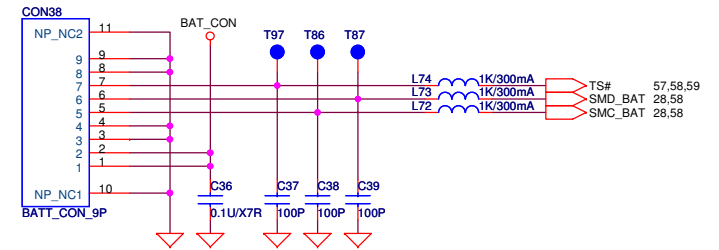
I/O PORT



FAN CONTROL

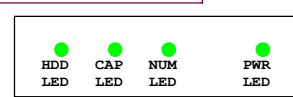
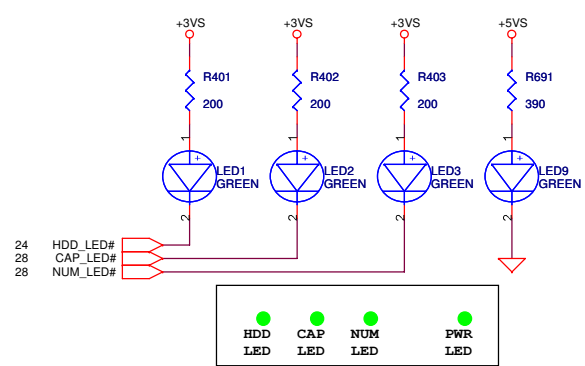
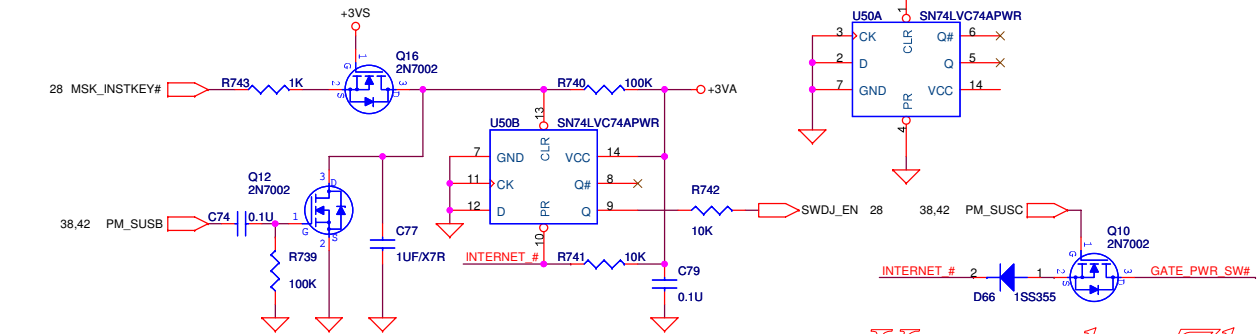
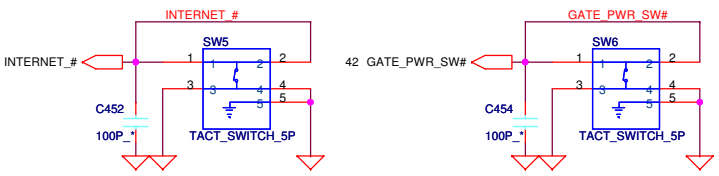
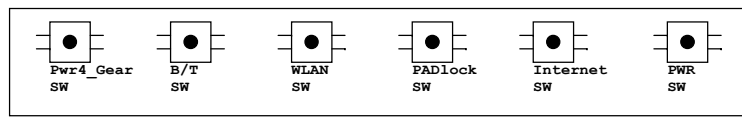
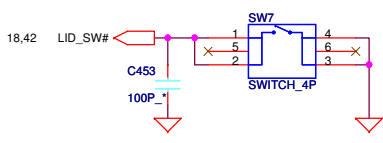
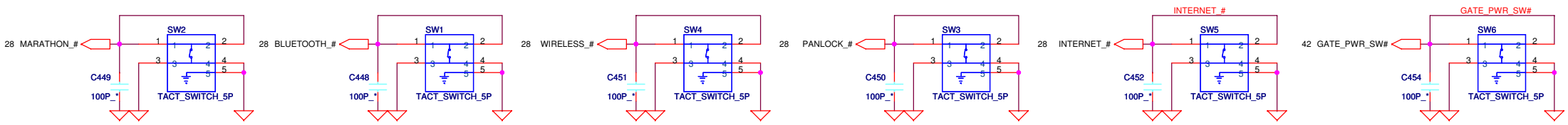


ACIN_CONN

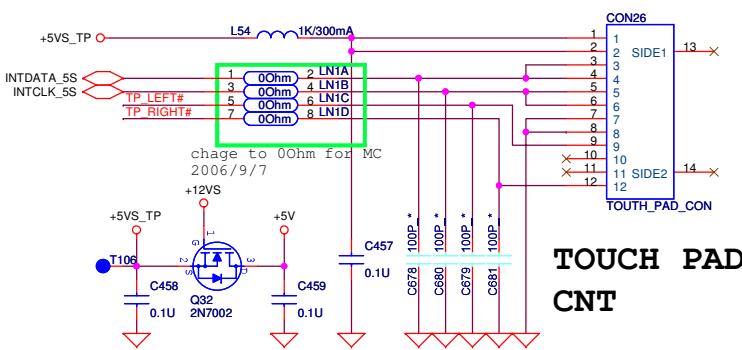
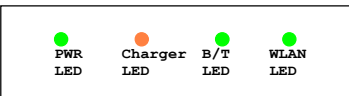
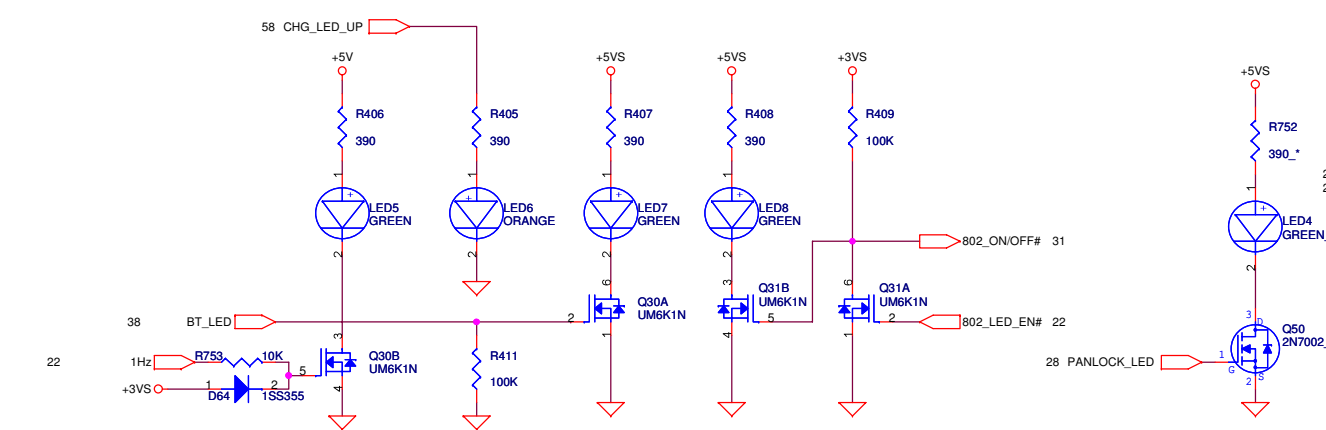
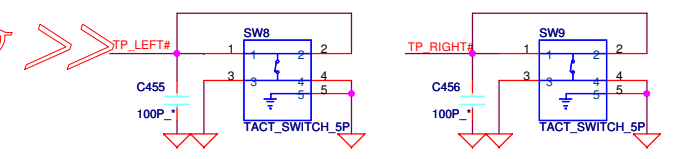


BAT_CONN

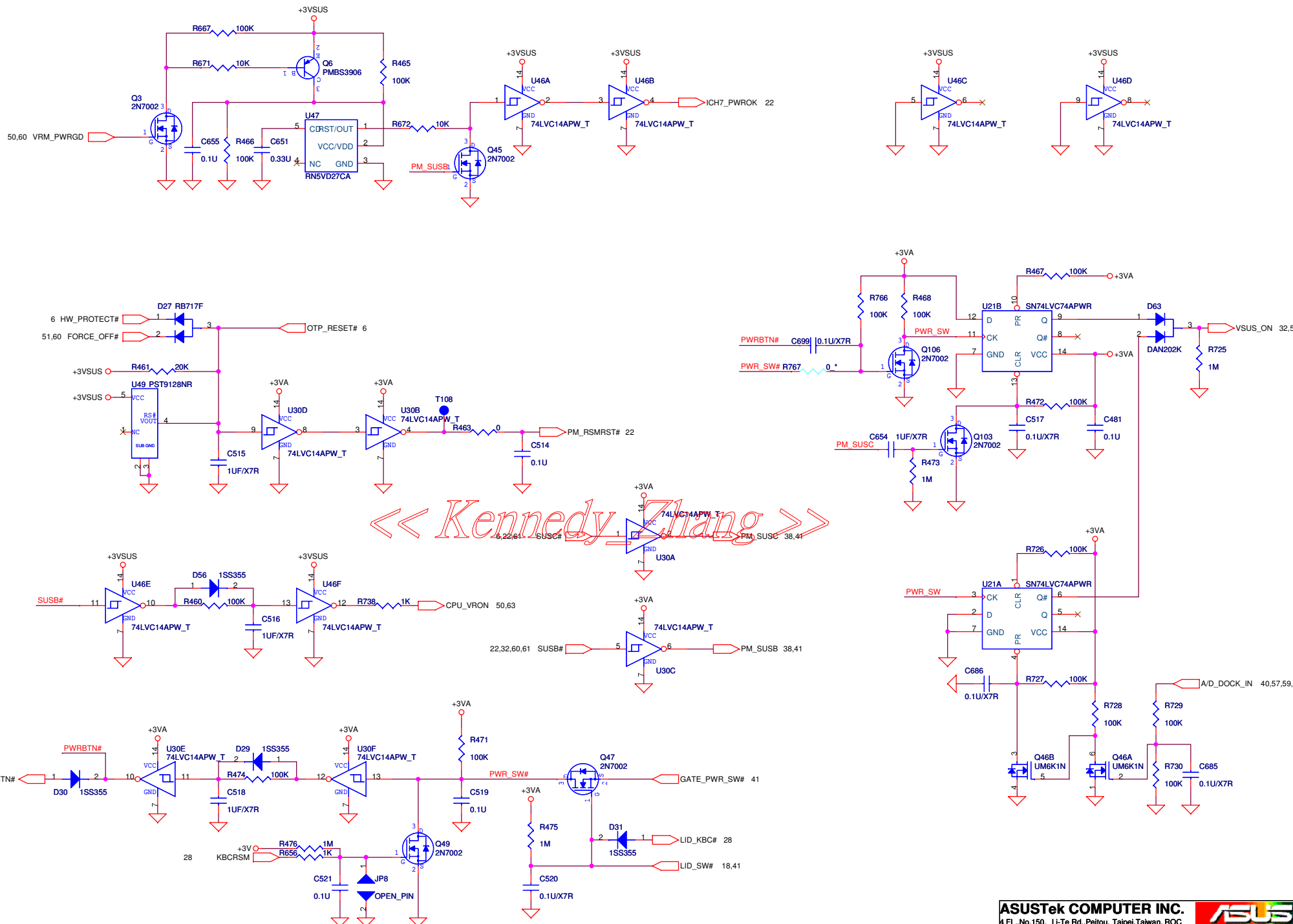
<< Kennedy_Zhang >>



<< Kennedy_Zhang >>



- +3VS → +3VS 6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,50,52,60,61
- +5V → +5V 15,17,19,25,28,32,36,38,40,59,61
- +5VS → +5VS 19,22,23,24,28,29,36,37,38,39,40,50,61
- +12VS → +12VS 17,18,61



<< Kennedy Zhang >>

- +3V ○ → +3V 28,30,31,32,34,37,38,54,61
- +3VA ○ → +3VA 20,38,41,54,59,63
- +3VSUS ○ → +3VSUS 18,21,22,23,28,29,30,51

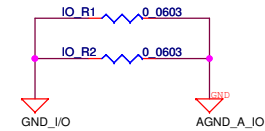
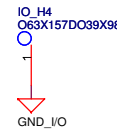
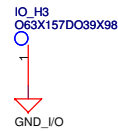
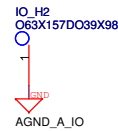
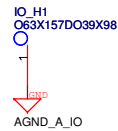
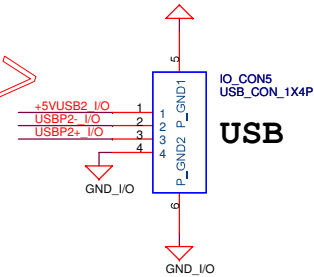
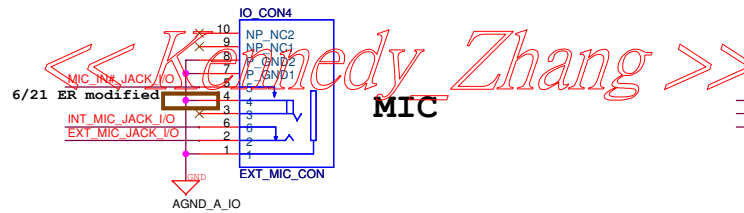
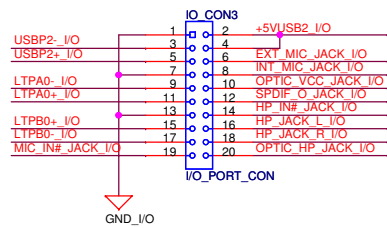
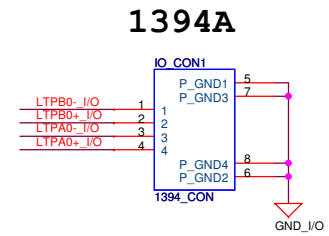
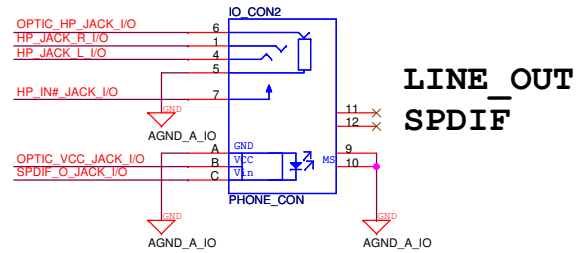
ASUSTEK COMPUTER INC.			
4 FL No.150, Li-Te Rd., Paitou, Taipei, Taiwan, ROC			
Title			
POWER-ON SEQUENCE			
Size Custom	Document Number A8J/F	Rev 2.0	
Date: Thursday, September 07, 2006	Sheet 42 of 63		

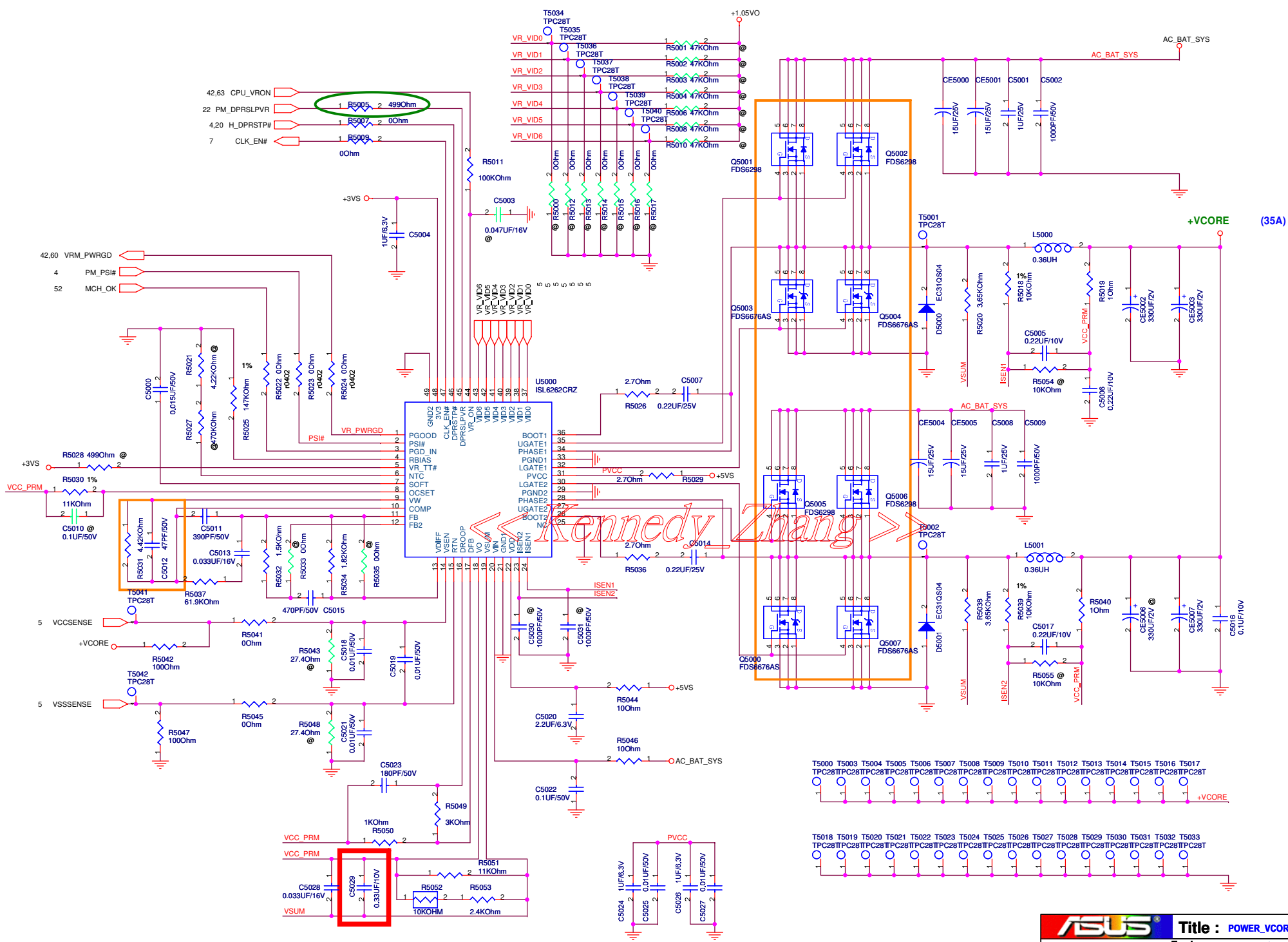
Revision History

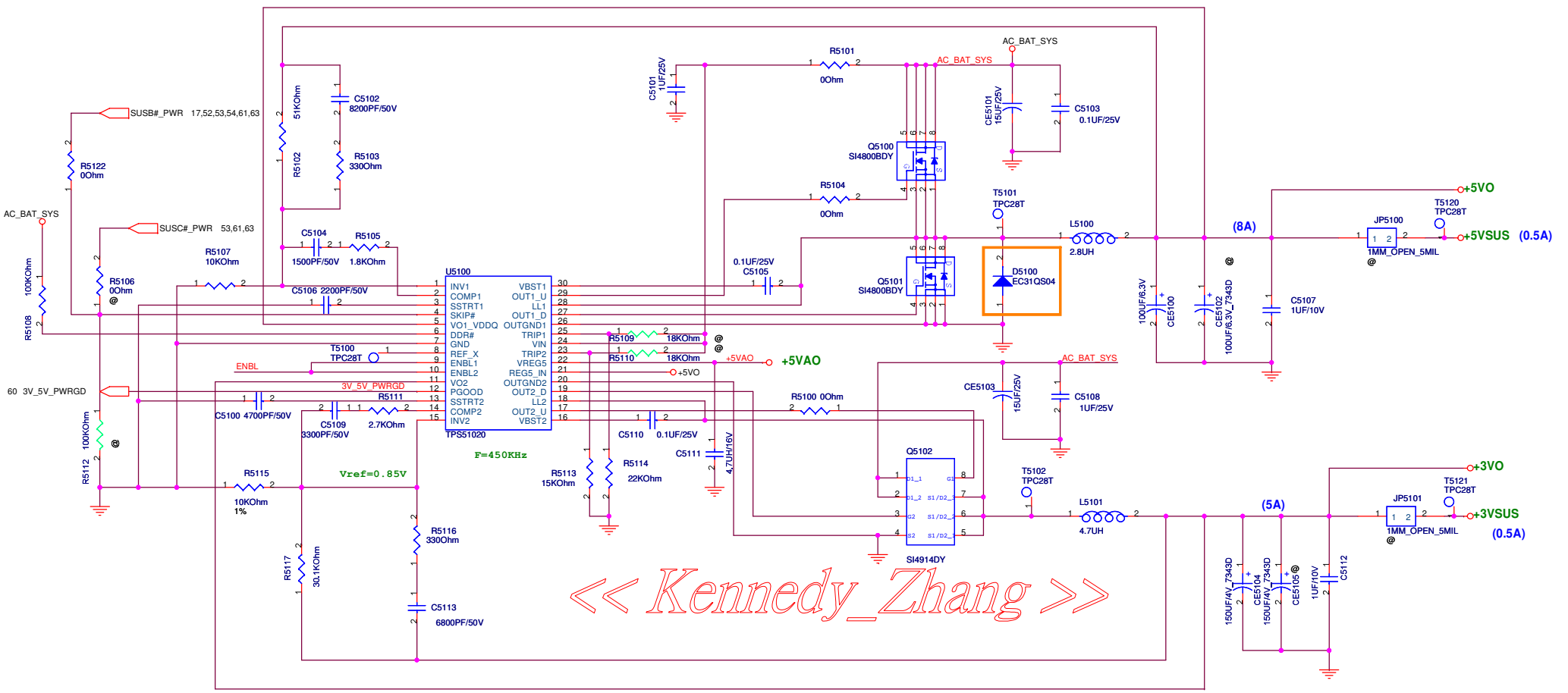
Power:

System:

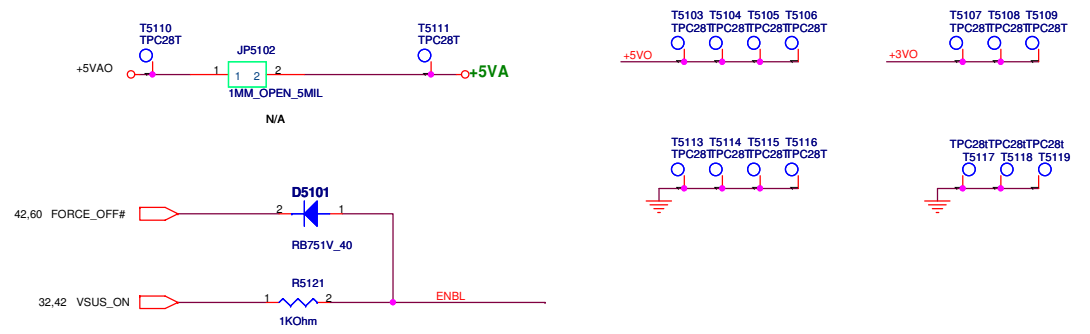
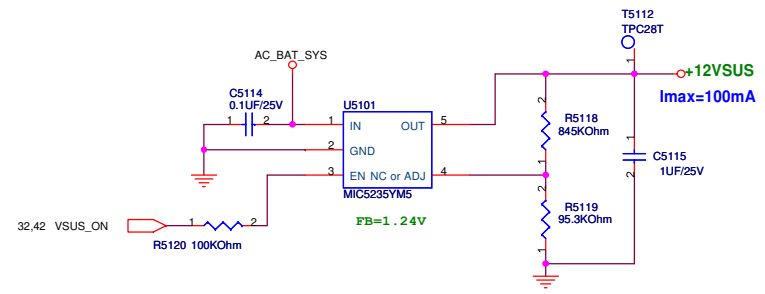
<< Kennedy_Zhang >>

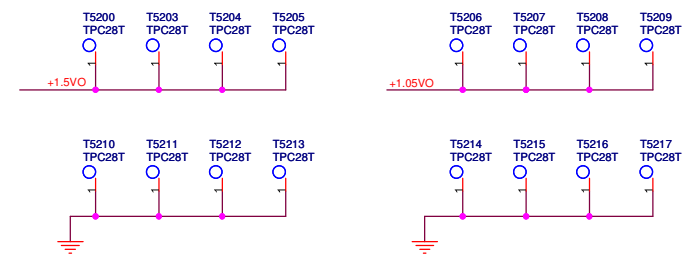
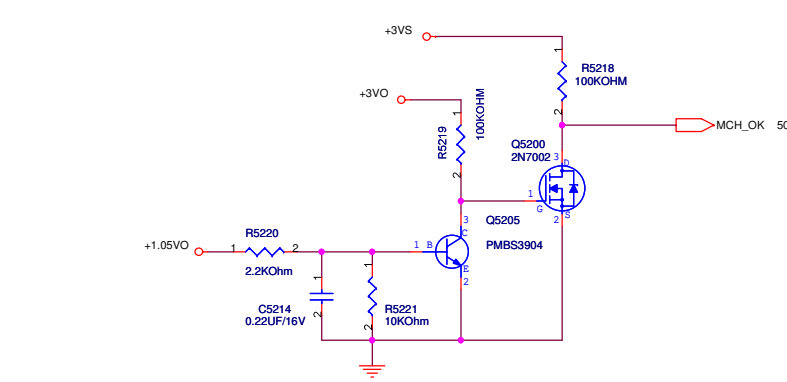
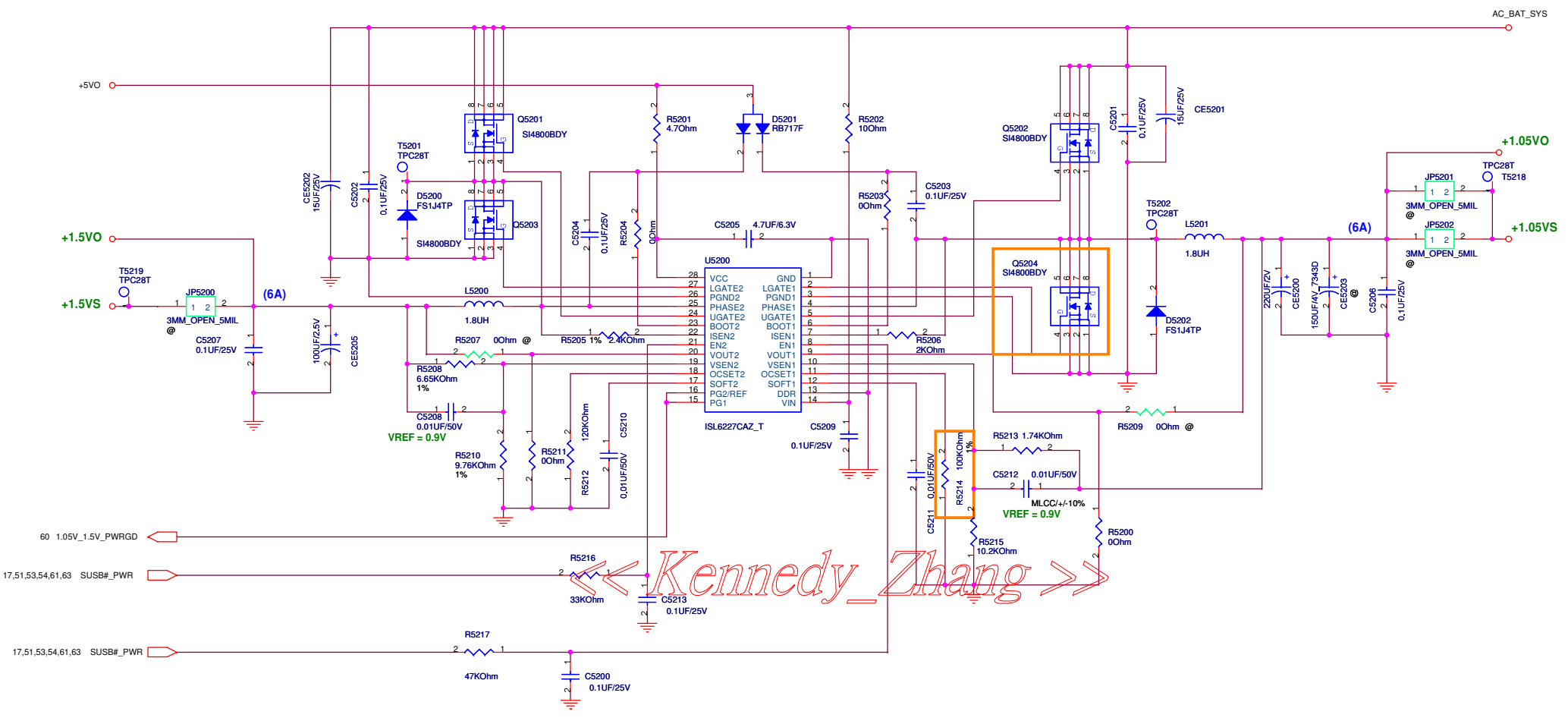




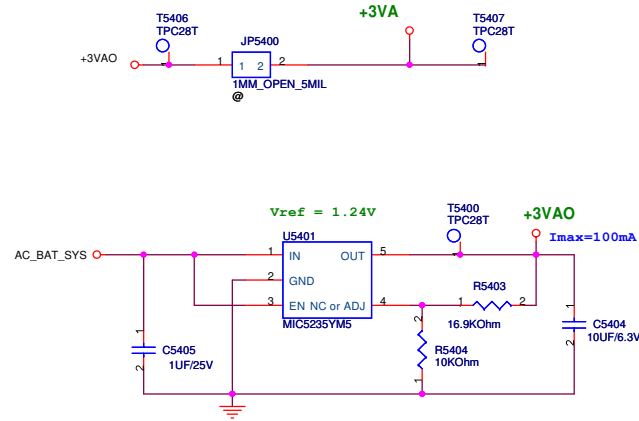


+12VSUS



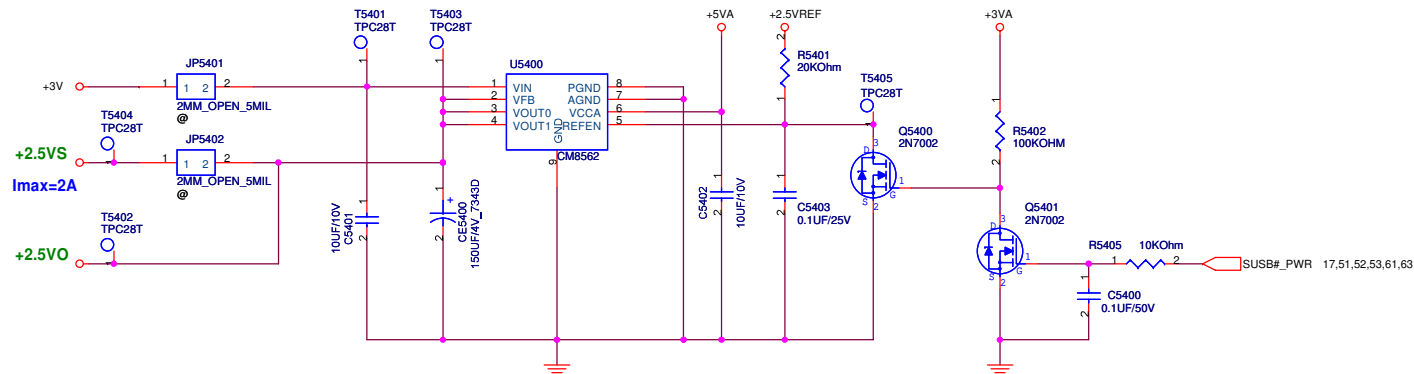


+3VAO

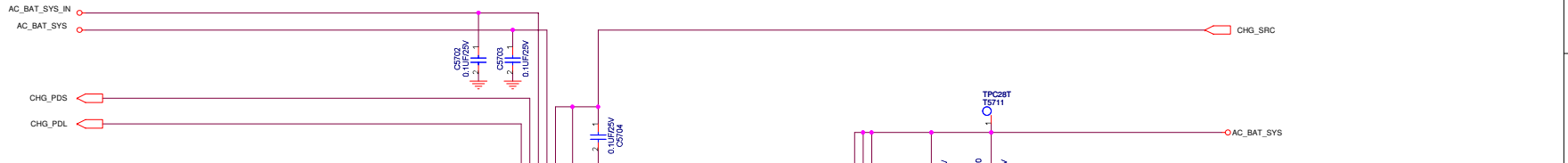
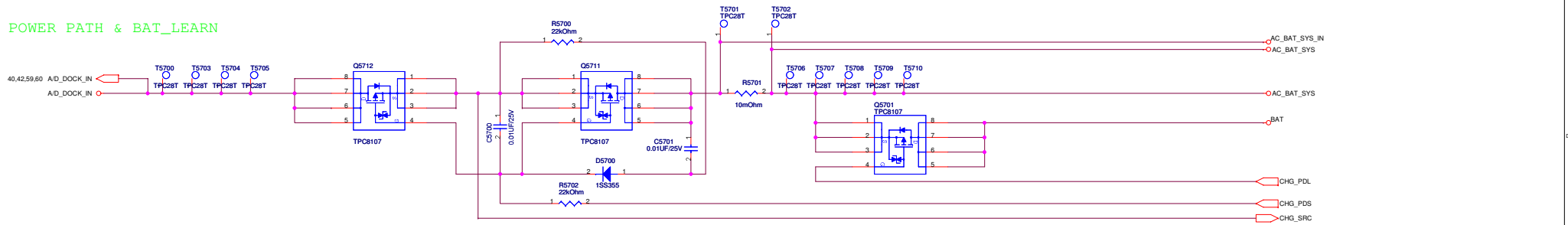


+2.5VS

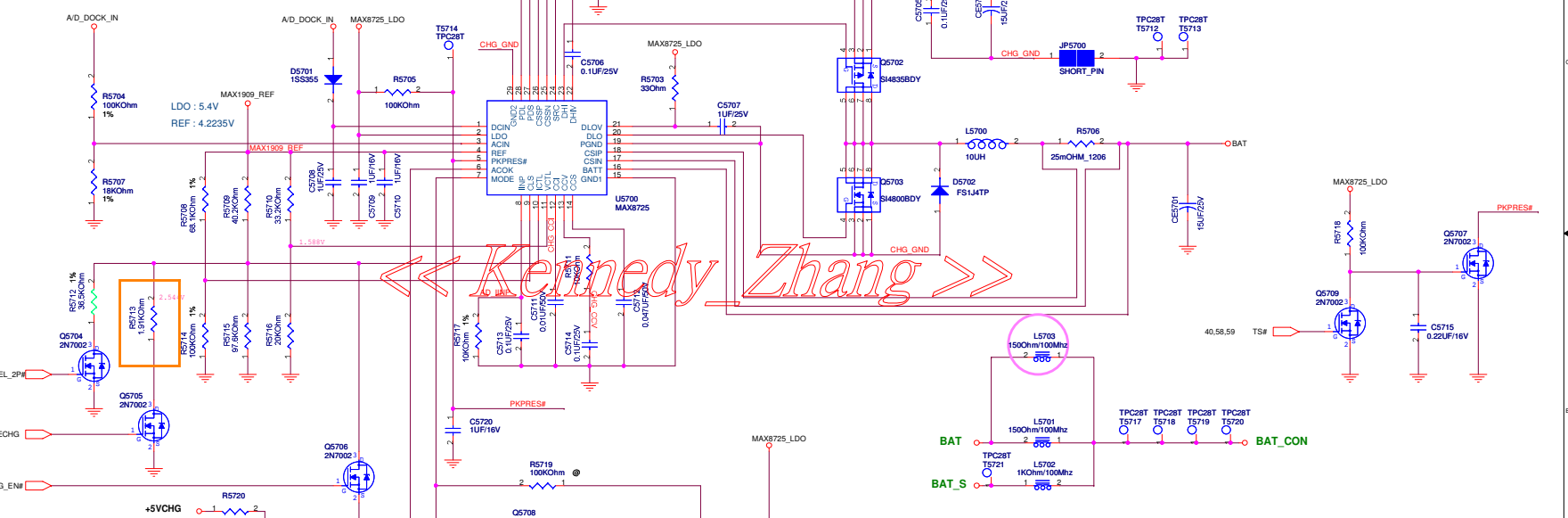
<< Kennedy_Zhang >>



POWER PATH & BAT_LEARN



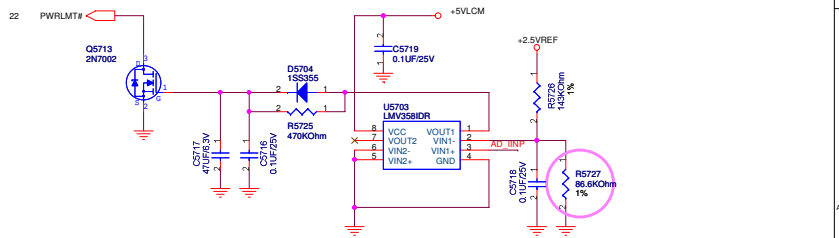
AC_IN Threshold 2.048Vmax A/D_DOCK_IN
 > 17.44V active
 Adapter In(max) = (0.075V/Rsense(ADn))*[VCLS-VREF]
 Rsense(ADn)=0.01 ohm
 VCLS= 1.86V(62.76W), 2.514V(84.82W)
 => R5708=68.1K, R5714=100K (84.82W)
 => R5708=127K, R5714=100K (82.76W)
 Charge Current Ichg = (0.075V/Rsense(CHG))*[VCTLU3.6V]
 Rsense(CHG)=0.025 ohm
 VCTLU= 3V => Ichg = 2.5A
 VCTL= 1.65V => Ichg = 1.4A
 Vbat = Cell * [Vref + (VCTL-1.8V) / 9.52]
 VCTL= 1.588V
 => Vbat = 4.2V
 Mode pin : Vmode > 2.8V (tie to LDO pin) ----> 4 Cells
 2.0 > Vmode > 1.6V (floating) ----> 3 Cells
 0.8 > Vmode (tie to GND) ----> Learning mode
 VCTL< 0.8V, or DCIN < 7V ---->Charger Disable
 Precharge current=150mA



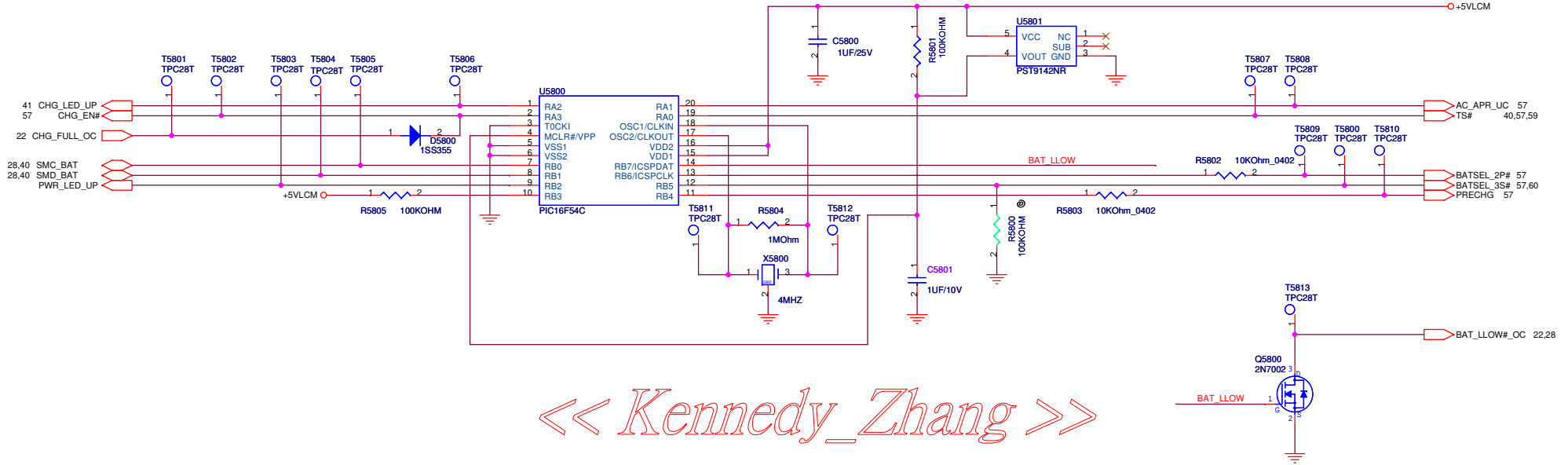
« Kennedy Zhang »

Power Limit Circuit

VINP=Input"RS"Glmg"R5717
 ABF input current=3.158A, R5727=86.6K
 WJA input current=4.316A, R5727=150K

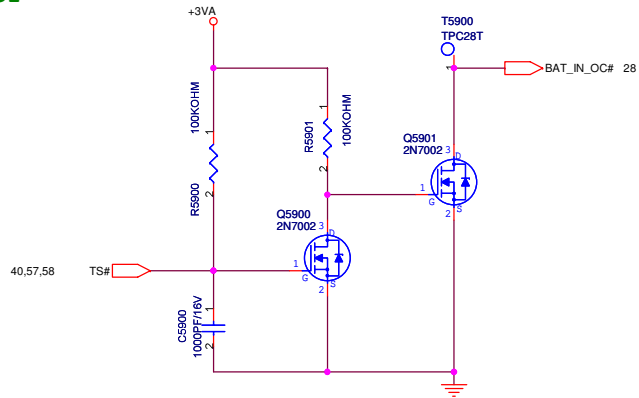


PIC16F54C

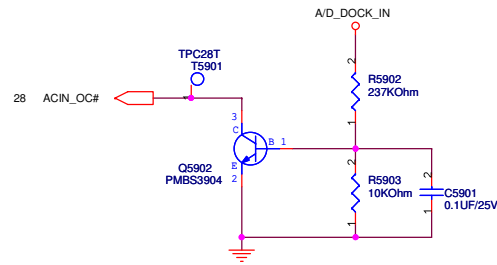


<< Kennedy_Zhang >>

BATTERY IN DETECT

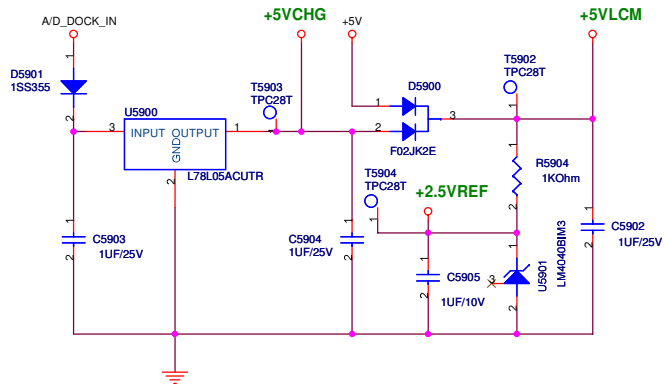


ADAPTER IN DETECT

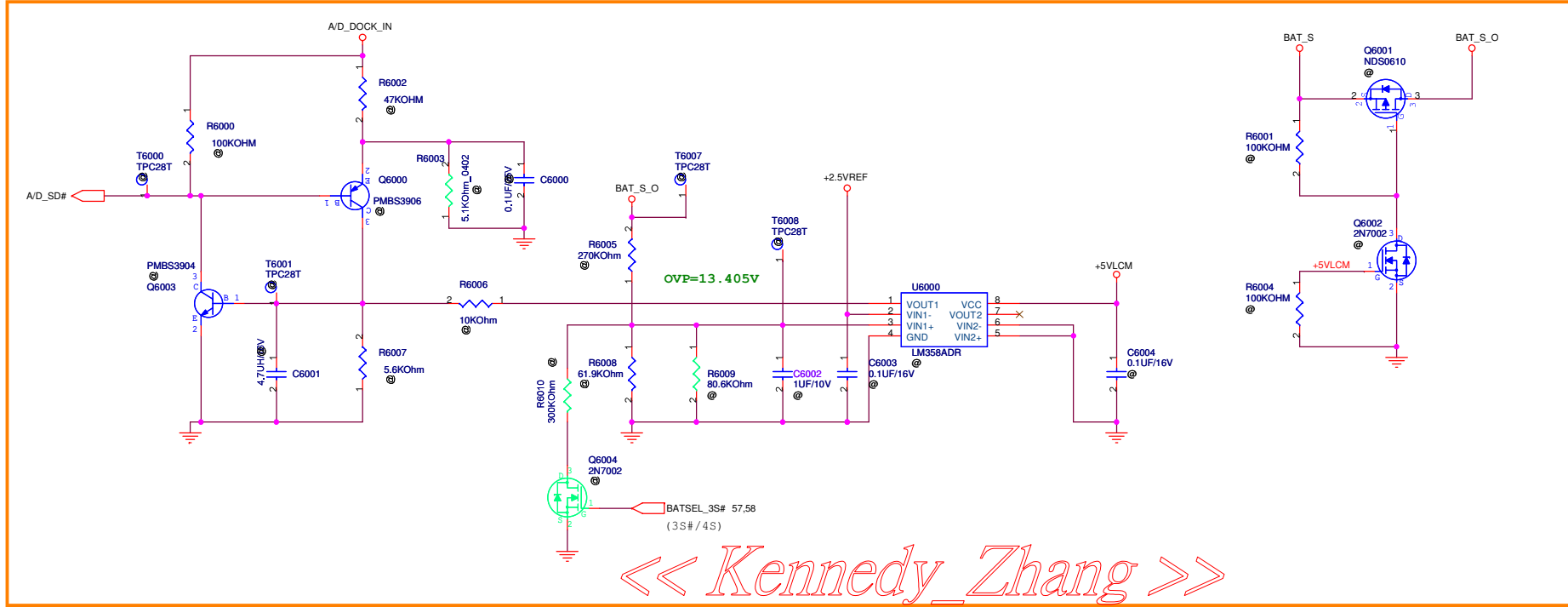


<< Kennedy_Zhang >>

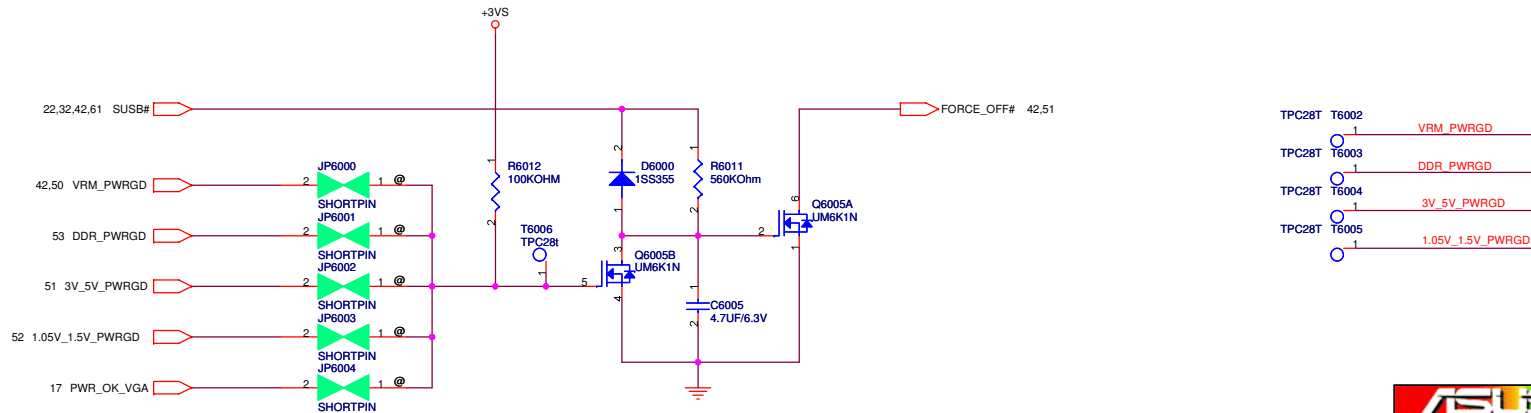
+5VLCM, +5VCHG & +2.5VREF



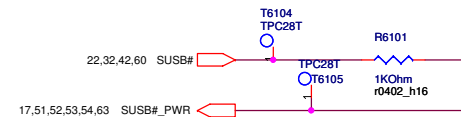
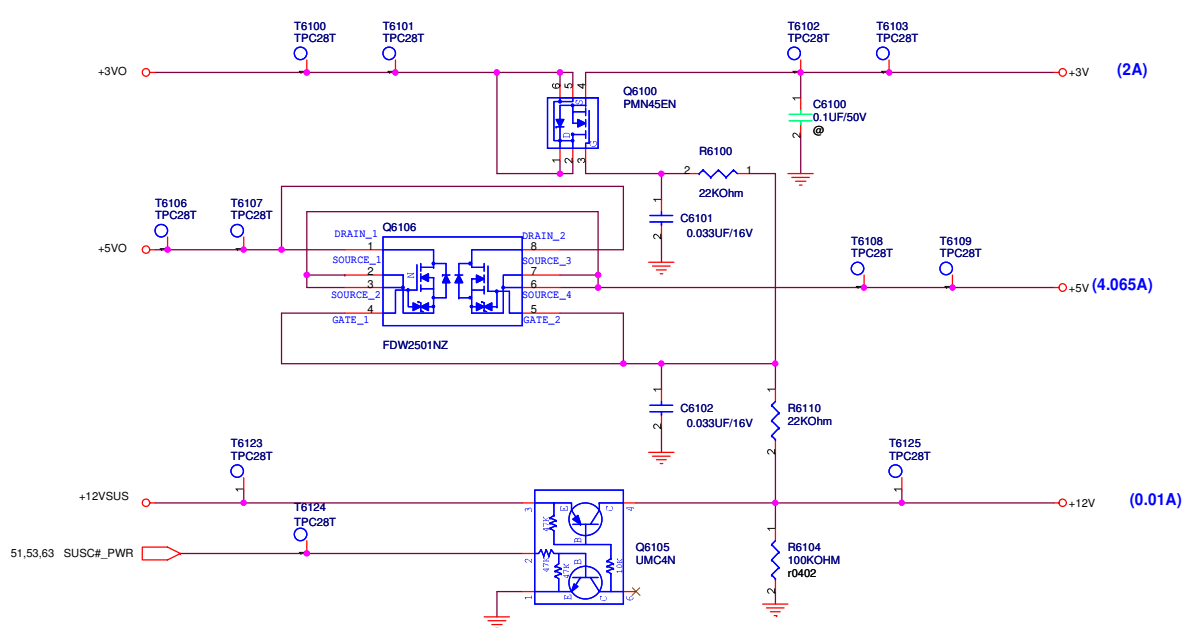
BATTERY A/D_SD# (OVP)



POWER GOOD DETECTOR

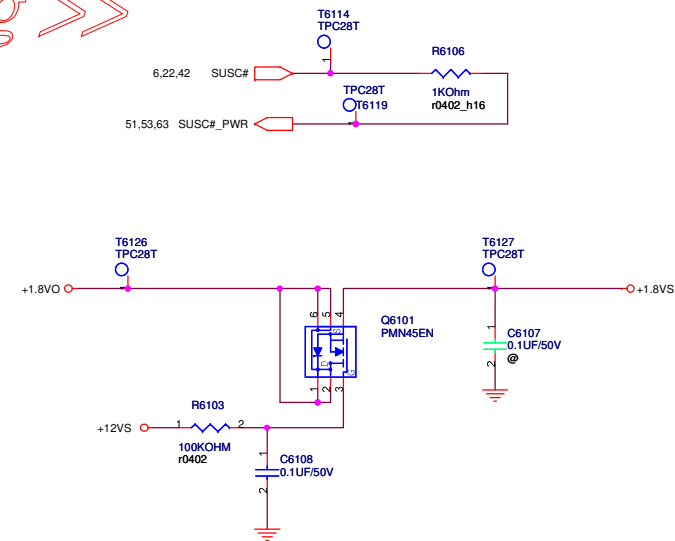
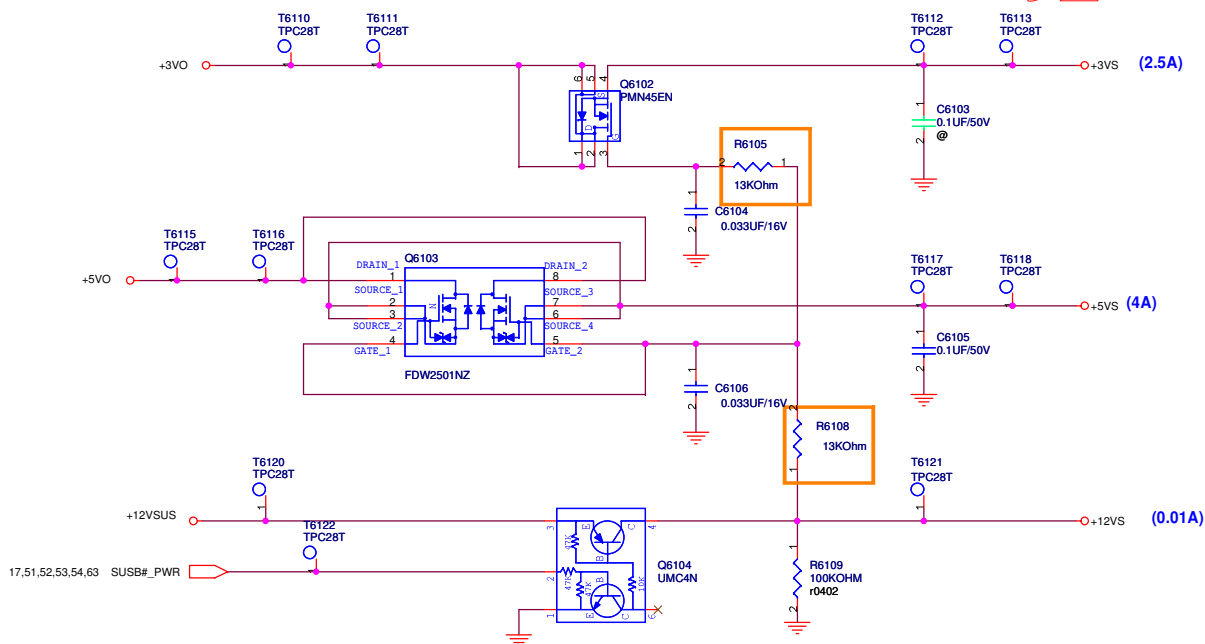


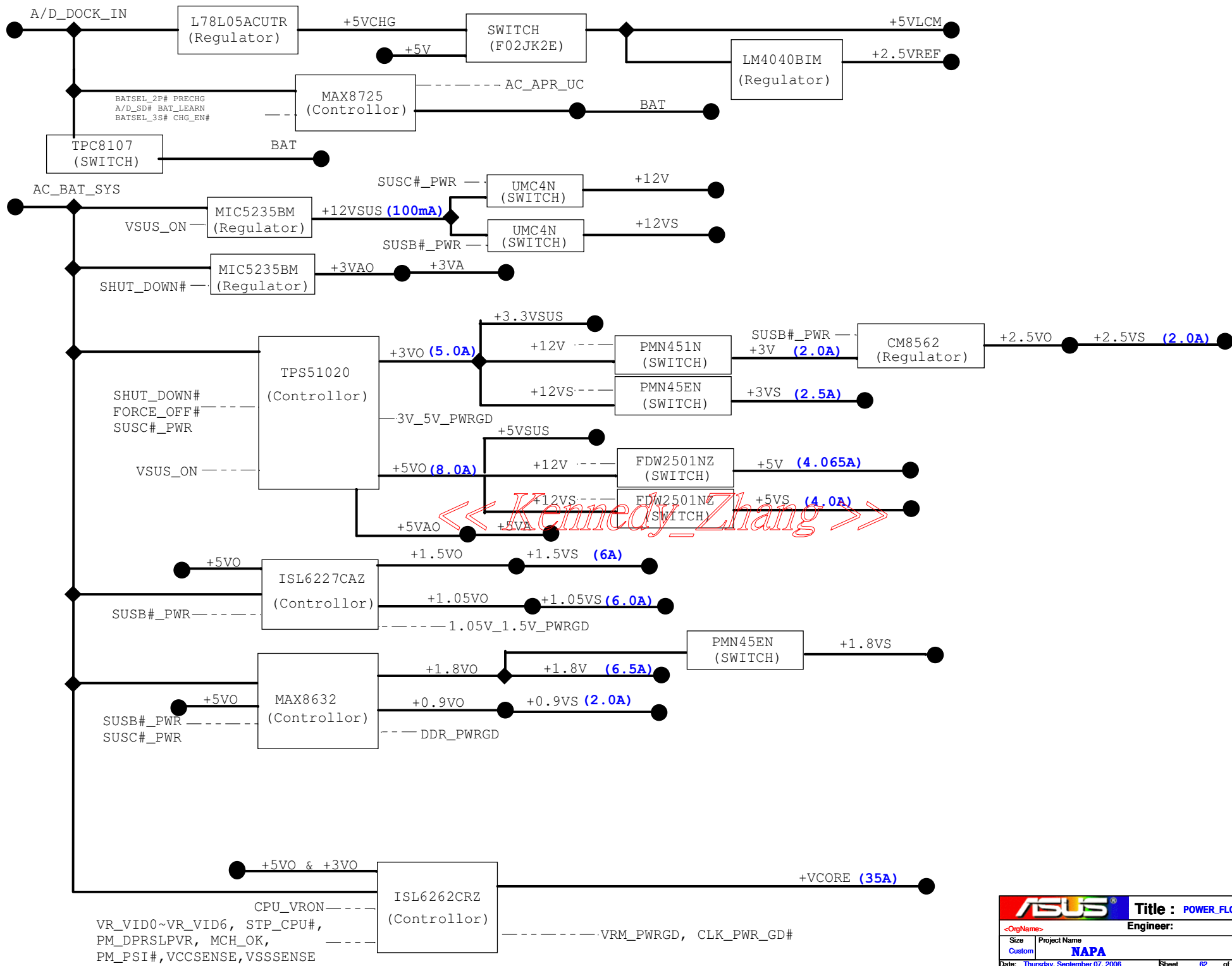
SUSC#_PWR POWER



SUSB#_PWR POWER

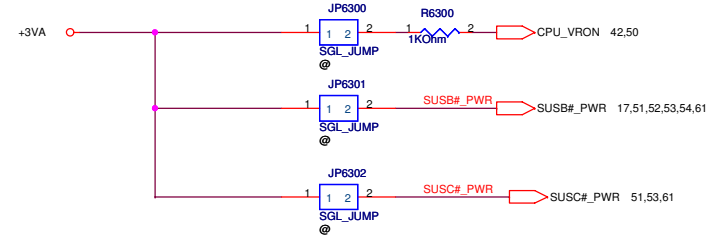
<< Kennedy_Zhang >>





AC_BAT_SYS	○	→	AC_BAT_SYS	17,18,50,51,52,53,54,57
+3VA	○	→	+3VA	20,38,41,42,54,59
+5VA	○	→	+5VA	6,51,54
+5VO	○	→	+5VO	51,52,53,61
+3VO	○	→	+3VO	51,52,61
+3V	○	→	+3V	28,30,31,32,34,37,38,42,54,61
+3VS	○	→	+3VS	6,7,9,11,13,14,15,17,18,19,22,23,24,26,27,28,29,30,31,32,33,36,37,38,39,41,50,52,60,61
+12VSUS	○	→	+12VSUS	51,61
+12V	○	→	+12V	25,34,37,40,61
+12VS	○	→	+12VS	17,18,41,61
+5V	○	→	+5V	15,17,19,25,28,32,36,38,40,41,59,61
+5VS	○	→	+5VS	19,22,23,24,28,29,36,37,38,39,40,41,50,61
+2.5VO	○	→	+2.5VO	54
+2.5VS	○	→	+2.5VS	11,17,19,38,54
+1.8VO	○	→	+1.8VO	53,61
+1.8V	○	→	+1.8V	9,12,14,15,38,53
+1.8VS	○	→	+1.8VS	17,61
+0.9VS	○	→	+0.9VS	16,17,53
BAT	○	→	BAT	57
+5VCHG	○	→	+5VCHG	57,59
+5VLCM	○	→	+5VLCM	28,57,58,59,60
+2.5VREF	○	→	+2.5VREF	54,57,59,60
+VCORE	○	→	+VCORE	5,6,50
+VGA_VCORE	○	→	+VGA_VCORE	
+VRAM	○	→	+VRAM	
+1.2VSP	○	→	+1.2VSP	

FOR POWER TEST



<< Kennedy_Zhang >>