- **Low Supply Voltage Range 1.8 V to 3.6 V**
- **Ultralow Power Consumption**
  - **Active Mode: 220 µA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.5 µA**
  - **Off Mode (RAM Retention): 0.1 µA**
- **Five Power-Saving Modes**
- **Ultrafast Wake-Up From Standby Mode in Less Than 1 µs**
- **16-Bit RISC Architecture, 62.5 ns Instruction Cycle Time**
- **Basic Clock Module Configurations:**
  - **Internal Frequencies up to 16 MHz With One Calibrated Frequency**
  - **Internal Very Low Power LF Oscillator**
  - **32-kHz Crystal**
  - **External Digital Clock Source**
- **16-Bit Timer_A With Two Capture/Compare Registers**
- **Universal Serial Interface (USI) Supporting SPI and I2C (See Table 1)**
- **Brownout Detector**
- **10-Bit 200-ksps A/D Converter With Internal Reference, Sample-and-Hold, and Autoscan (See Table 1)**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **On-Chip Emulation Logic With Spy-Bi-Wire Interface**
- **Family Members Details See Table 1**
- **Available in a 14-Pin Plastic Small-Outline Thin Package (TSSOP), 14-Pin Plastic Dual Inline Package (PDIP), and 16-Pin QFN**
- **For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide***

description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1µs.

The MSP430G2x21/31 series is an ultralow-power mixed signal microcontroller with a built-in 16-bit timer and ten I/O pins. The MSP430G2x31 family members have a 10-bit A/D converter and built-in communication capability using synchronous protocols (SPI or I2C). For configuration details, see Table 1.

Typical applications include low-cost sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system.

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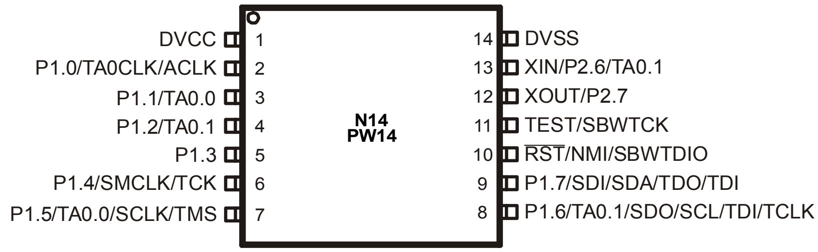
Table 1. Available Options – MSP430G2x21 and MSP430G2x31

Device	BSL	EEM	Flash (KB)	RAM (B)	Timer_A	USI	ADC10 Channel	CLOCK	I/O	Package Type
MSP430G2231IRSA16 MSP430G2231IPW14 MSP430G2231IN14	-	1	2	128	1x TA2	1	8	LF, DCO, VLO	10	16-QFN 14-TSSOP 14-PDIP
MSP430G2221IRSA16 MSP430G2221IPW14 MSP430G2221IN14	-	1	2	128	1x TA2	1	-	LF, DCO, VLO	10	16-QFN 14-TSSOP 14-PDIP
MSP430G2131IRSA16 MSP430G2131IPW14 MSP430G2131IN14	-	1	1	128	1x TA2	1	8	LF, DCO, VLO	10	16-QFN 14-TSSOP 14-PDIP
MSP430G2121IRSA16 MSP430G2121IPW14 MSP430G2121IN14	-	1	1	128	1x TA2	1	-	LF, DCO, VLO	10	16-QFN 14-TSSOP 14-PDIP

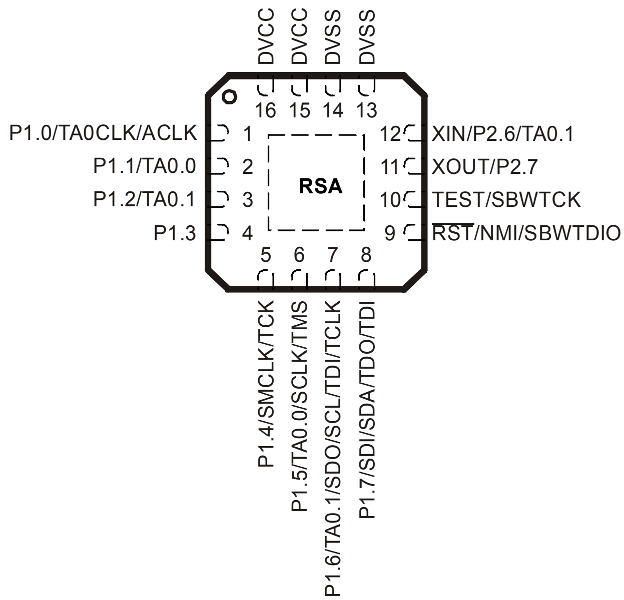
† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PRODUCT PREVIEW

device pinout, MSP430G2x21



NOTE: See port schematics section for detailed I/O information.



NOTE: See port schematics section for detailed I/O information.

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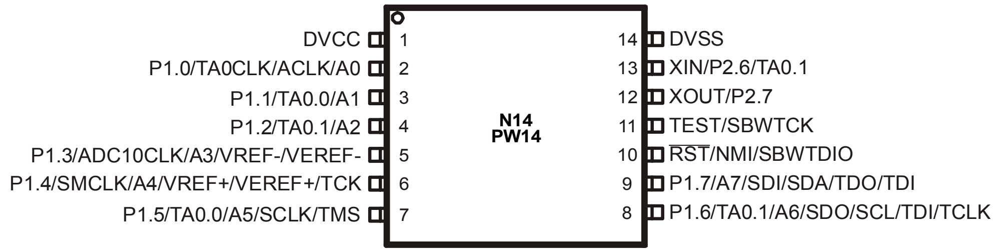
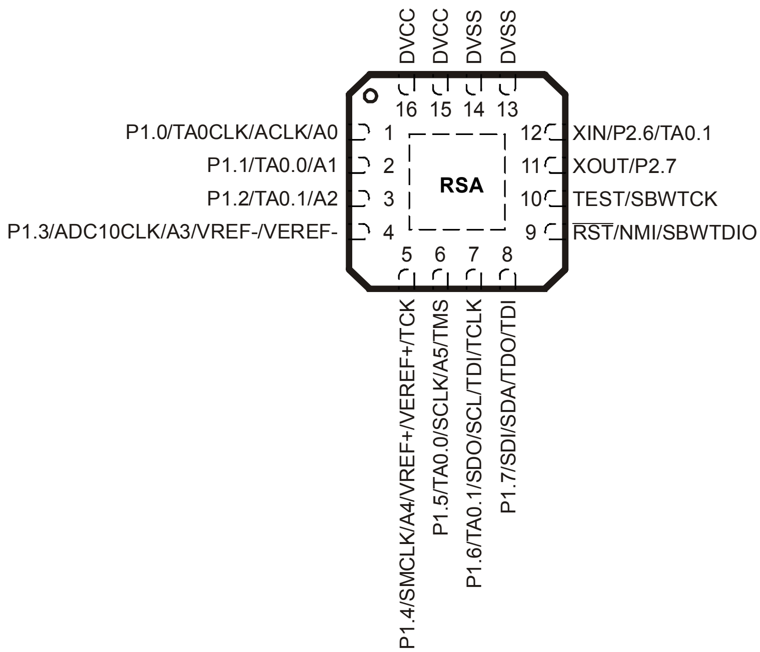
device pinout, MSP430G2x31



NOTE: See port schematics section for detailed I/O information.



NOTE: See port schematics section for detailed I/O information.

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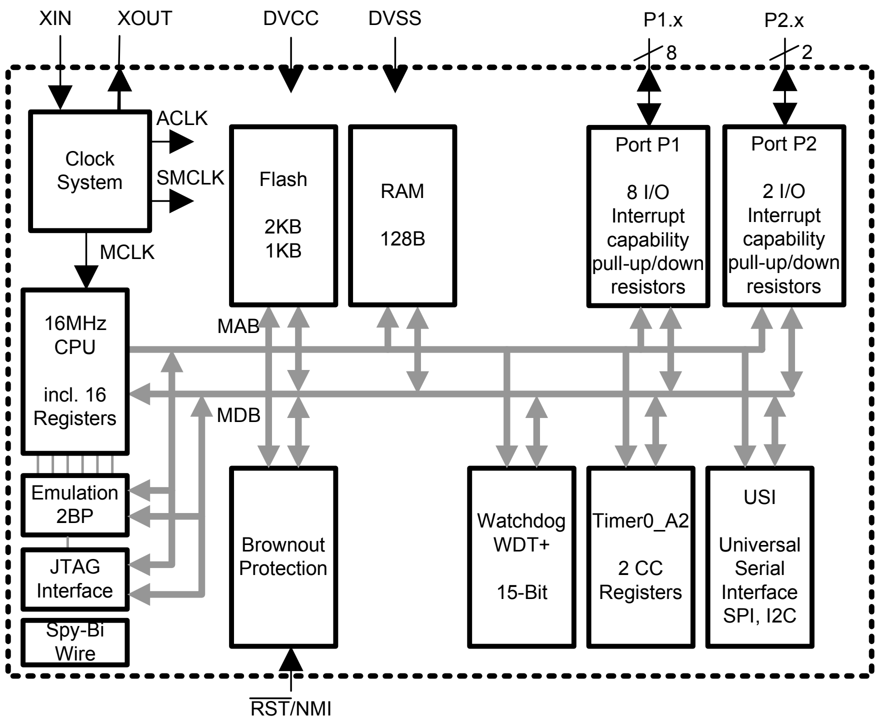
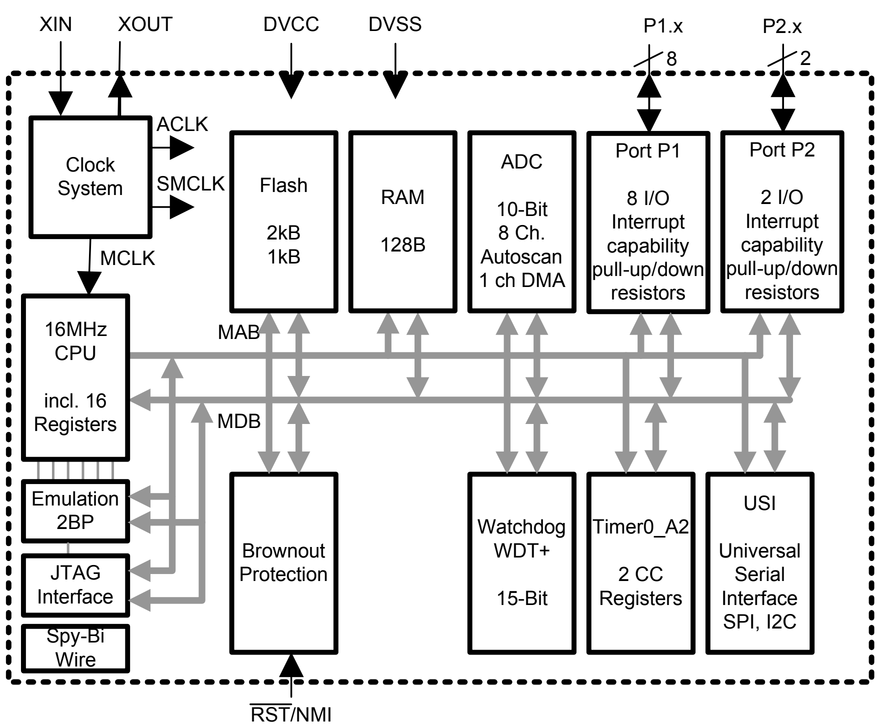
functional block diagram, MSP430G2x21



functional block diagram, MSP430G2x31



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Terminal Functions, MSP430G2x21 and MSP430G2x31

TERMINAL				DESCRIPTION
NAME	14 N, PW NO.	16 RSA NO.	I/O	
P1.0/ TA0CLK/ ACLK/ A0	2	1	I/O	General-purpose digital I/O pin Timer0_A, clock signal TACLK input ACLK signal ouput ADC10 analog input A0 (see Note 1)
P1.1/ TA0.0/ A1	3	2	I/O	General-purpose digital I/O pin Timer0_A, capture: CCI0A input, compare: Out0 output ADC10 analog input A1 (see Note 1)
P1.2/ TA0.1/ A2/	4	3	I/O	General-purpose digital I/O pin Timer0_A, capture: CCI1A input, compare: Out1 output ADC10 analog input A2 (see Note 1)
P1.3/ ADC10CLK/ A3/ VREF−/VEREF/	5	4	I/O	General-purpose digital I/O pin ADC10, conversion clock output (see Note 1) ADC10 analog input A3 (see Note 1) ADC10 negative reference voltage (see Note 1)
P1.4/ SMCLK/ A4/ VREF+/VEREF+/ TCK	6	5	I/O	General-purpose digital I/O pin SMCLK signal output ADC10 analog input A4 (see Note 1) ADC10 positive reference voltage (see Note 1) JTAG test clock, input terminal for device programming and test
P1.5/ TA0.0/ A5/ SCLK/ TMS	7	6	I/O	General-purpose digital I/O pin Timer0_A, compare: Out0 output ADC10 analog input A5 (see Note 1) USI: clk input in I2C mode; clk in/output in SPI mode JTAG test mode select, input terminal for device programming and test
P1.6/ TA0.1/ A6/ SDO/ SCL/ TDI/ TCLK	8	7	I/O	General-purpose digital I/O pin Timer0_A, compare: Out1 output ADC10 analog input A6 (see Note 1) USI: Data output in SPI mode USI: I2C clock in I2C mode JTAG test data input or test clock input during programming and test
P1.7/ A7/ SDI/ SDA/ TDO/ TDI	9	8	I/O	General-purpose digital I/O pin ADC10 analog input A7 (see Note 1) USI: Data input in SPI mode USI: I2C data in I2C mode JTAG test data output terminal or test data input during programming and test

NOTES: 1. MSP430G2x31 only

Terminal Functions, MSP430G2x21 and MSP430G2x31 (continued)

TERMINAL				DESCRIPTION
NAME	14 N, PW NO.	16 RSA NO.	I/O	
XIN/ P2.6/ TA0.1	13	12	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin Timer0_A, compare: Out1 output
XOUT/ P2.7	12	11	I/O	Output terminal of crystal oscillator (see Note 1) General-purpose digital I/O pin
$\overline{RST}$/ NMI/ SBWTDIO	10	9	I	Reset Nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/ SBWTCK	11	10	I	Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
DVCC	1	16 15	NA	Supply voltage
DVSS	14	14 13	NA	Ground reference
NC	–	–	NA	Not connected
QFN Pad	–	Pad	NA	QFN package pad connection to V_{SS} recommended.

NOTES: 1. If XOUT/P2.7 is used as an input, excess current will flow until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

† TDO or TDI is selected via JTAG instruction.

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short-form description

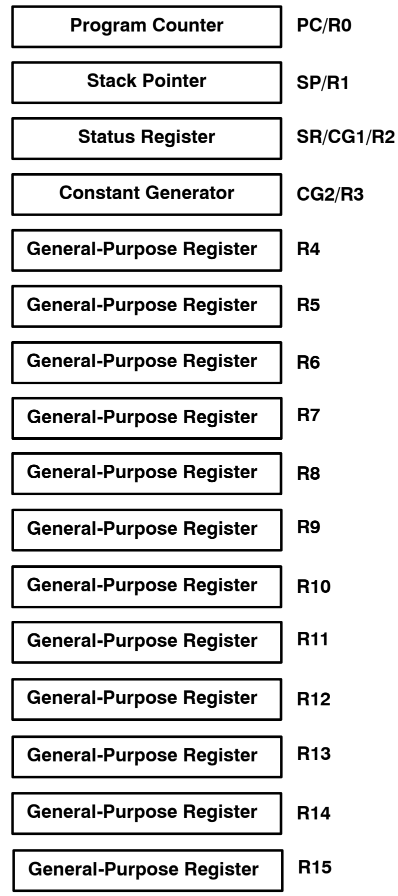
CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 2 shows examples of the three types of instruction formats; Table 3 shows the address modes.

Table 2. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4,R5	R4 + R5 −−−> R5
Single operands, destination only	e.g., CALL R8	PC −−>(TOS), R8−−> PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 3. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 −−> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)−−> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) −−> M(TONI)
Absolute	●	●	MOV &MEM,&TCDAT		M(MEM) −−> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) −−> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) −−> R11 R10 + 2−−> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 −−> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active. MCLK is disabled
  - DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc-generator is disabled
  - Crystal oscillator is stopped

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interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (e.g., flash is not programmed) the CPU will go into LPM4 immediately after power-up.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Timer+ Flash key violation PC out-of-range (see Note 1)	PORIFG RSTIFG WDTIFG KEYV (see Note 2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (see Notes 2 and 5)	(non)-maskable, (non)-maskable, (non)-maskable	0FFFCh	30
			0FFFAh	29
			0FFF8h	28
			0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer_A2	TACCR0 CCIFG (see Note 3)	maskable	0FFF2h	25
Timer_A2	TACCR1 CCIFG. TAIFG (see Notes 2 and 3)	maskable	0FFF0h	24
			0FFEEh	23
			0FFECh	22
ADC10 (see Note 4)	ADC10IFG (see Note 3 and 4)	maskable	0FFEAh	21
USI	USIIFG, USISTTIFG (see Notes 2, 3)	maskable	0FFE8h	20
I/O Port P2 (two flags)	P2IFG.6 to P2IFG.7 (see Notes 2 and 3)	maskable	0FFE6h	19
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 2 and 3)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
(see Note 6)			0FFDEh ... 0FFC0h	15 ... 0, lowest

NOTES:
1. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
2. Multiple source flags
3. Interrupt flags are located in the module
4. MSP430G2x31 only.
5. (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
6. The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE: Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
OFIE: Oscillator fault enable
NMIIE: (Non)maskable interrupt enable
ACCVIE: Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h								

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG: Set on Watchdog Timer overflow (in watchdog mode) or security key violation.
Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.
OFIFG: Flag set on oscillator fault
RSTIFG: External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power-up
PORIFG: Power-On Reset interrupt flag. Set on V_{CC} power-up.
NMIIFG: Set via $\overline{RST}$/NMI-pin

Address	7	6	5	4	3	2	1	0
03h								

Legend

rw:	Bit can be read and written.
rw-0,1:	Bit can be read and written. It is Reset or Set by PUC.
rw-(0,1):	Bit can be read and written. It is Reset or Set by POR.
(shaded box)	SFR bit is not present in device

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memory organization

		MSP430G2021 MSP430G2031	MSP430G2121 MSP430G2131	MSP430G2221 MSP430G2231
Memory Main: interrupt vector Main: code memory	Size Flash Flash	512B 0xFFFF to 0xFFC0 0xFFFF to 0xFE00	1kB 0xFFFF to 0xFFC0 0xFFFF to 0xFC00	2kB 0xFFFF to 0xFFC0 0xFFFF to 0xF800
Information memory	Size Flash	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h
RAM	Size	128B 027Fh − 0200h	128B 027Fh − 0200h	128B 027Fh − 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h

flash memory

The flash memory can be programmed via the Spy-Bi-Wire/JTAG port, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory.*
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.

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peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide.*

oscillator and system clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator and an internal digitally controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 μs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

DCO CALIBRATION DATA (PROVIDED FROM FACTORY IN FLASH INFO MEMORY SEGMENT A)			
DCO FREQUENCY	CALIBRATION REGISTER	SIZE	ADDRESS
1 MHz	CALBC1_1MHZ	byte	010FFh
	CALDCO_1MHZ	byte	010FEh

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brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

digital I/O

There is one 8-bit I/O port implemented—port P1—and two bits of I/O port P2:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and the two bits of port P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pull-up/pull-down resistor.

WDT+ watchdog timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Timer_A2

Timer_A2 is a 16-bit timer/counter with two capture/compare registers. Timer_A2 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_A2 Signal Connections – Device with ADC10

Input Pin Number		Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number	
PW, N	RSA					PW, N	RSA
2 - P1.0	1 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
2 - P1.0	1 - P1.0	$\overline{\text{TACLK}}$	INCLK				
3 - P1.1	2 - P1.1	TA0	CCI0A	CCR0	TA0	3 - P1.1	2 - P1.1
7 - P1.5	6 - P1.5	ACLK (internal)	CCI0B			7 - P1.5	6 - P1.5
		V_{SS}	GND				
		V_{CC}	V_{CC}				
4 - P1.2	3 - P1.2	TA1	CCI1A	CCR1	TA1	4 - P1.2	3 - P1.2
8 - P1.6	7 - P1.6	TA1	CCI1B			8 - P1.6	7 - P1.6
		V_{SS}	GND			13 - P2.6	12 - P2.6
		V_{CC}	V_{CC}				

USI

The universal serial interface (USI) module is used for serial data communication and provides the basic hardware for synchronous communication protocols like SPI and I2C.

ADC10 (MSP430G2x31 only)

The ADC10 module supports fast, 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator and data transfer controller, or DTC, for automatic conversion result handling, allowing ADC samples to be converted and stored without any CPU intervention.

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peripheral file map

PERIPHERALS WITH WORD ACCESS			
ADC10 (MSP430G2x31 only)	ADC control 0 ADC control 1 ADC memory	ADC10CTL0 ADC10CTL0 ADC10MEM	01B0h 01B2h 01B4h
Timer_A	Capture/compare register Capture/compare register Timer_A register Capture/compare control Capture/compare control Timer_A control Timer_A interrupt vector	TACCR1 TACCR0 TAR TACCTL1 TACCTL0 TACTL TAIV	0174h 0172h 0170h 0164h 0162h 0160h 012Eh
Flash Memory	Flash control 3 Flash control 2 Flash control 1	FCTL3 FCTL2 FCTL1	012Ch 012Ah 0128h
Watchdog Timer+	Watchdog/timer control	WDTCTL	0120h
PERIPHERALS WITH BYTE ACCESS			
ADC10 (MSP430G2x31 only)	Analog enable	ADC10AE	04Ah
USI	USI control 0 USI control 1 USI clock control USI bit counter USI shift register	USICTL0 USICTL1 USICKCTL USICNT USISR	078h 079h 07Ah 07Bh 07Ch
Basic Clock System+	Basic clock system control 3 Basic clock system control 2 Basic clock system control 1 DCO clock frequency control	BCSCTL3 BCSCTL2 BCSCTL1 DCOCTL	053h 058h 057h 056h
Port P2	Port P2 resistor enable Port P2 selection Port P2 interrupt enable Port P2 interrupt edge select Port P2 interrupt flag Port P2 direction Port P2 output Port P2 input	P2REN P2SEL P2IE P2IES P2IFG P2DIR P2OUT P2IN	02Fh 02Eh 02Dh 02Ch 02Bh 02Ah 029h 028h
Port P1	Port P1 resistor enable Port P1 selection Port P1 interrupt enable Port P1 interrupt edge select Port P1 interrupt flag Port P1 direction Port P1 output Port P1 input	P1REN P1SEL P1IE P1IES P1IFG P1DIR P1OUT P1IN	027h 026h 025h 024h 023h 022h 021h 020h
Special Function	SFR interrupt flag 2 SFR interrupt flag 1 SFR interrupt enable 2 SFR interrupt enable 1	IFG2 IFG1 IE2 IE1	003h 002h 001h 000h

absolute maximum ratings†

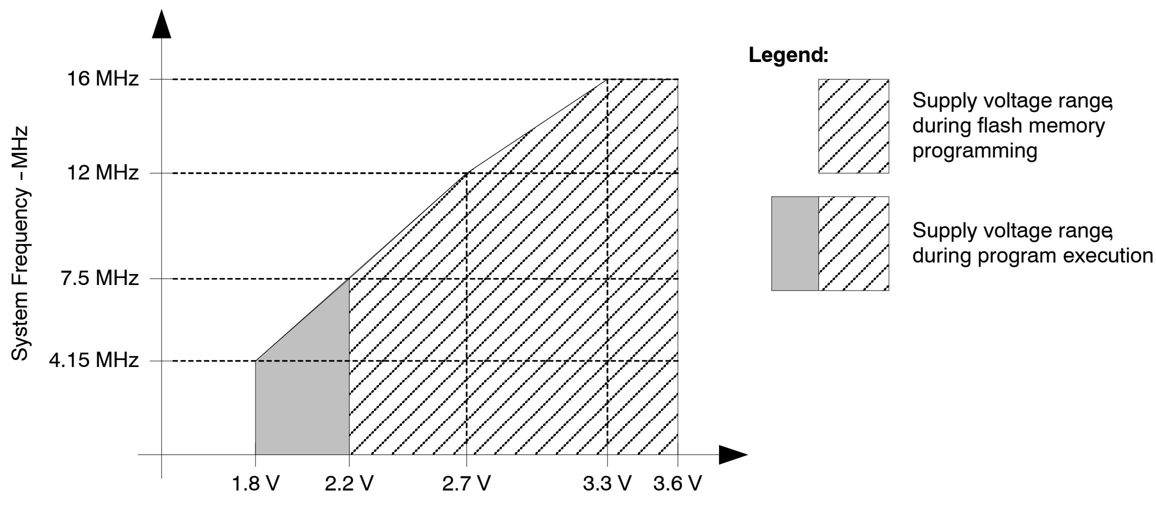
Voltage applied at V_{CC} to V_{SS} . . . . –0.3 V to 4.1 V
Voltage applied to any pin (see Note 2) . . . . –0.3 V to V_{CC}+0.3 V
Diode current at any device terminal . . . . ±2 mA
Storage temperature, T_{stg} (unprogrammed device, see Note 3) . . . . –55°C to 150°C
Storage temperature, T_{stg} (programmed device, see Note 3) . . . . –40°C to 85°C

NOTES: 1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
3. Higher temperature may be applied during board soldering process according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage during program execution, V_{CC}		1.8		3.6	V
Supply voltage during program/erase flash memory, V_{CC}		2.2		3.6	V
Supply voltage, V_{SS}			0		V
Operating free-air temperature range, T_A	I Version	–40		85	°C
Processor frequency f_{SYSTEM} (Maximum MCLK frequency)	V_{CC} = 1.8 V, Duty Cycle = 50% ±10%	dc		4.15	MHz
	V_{CC} = 2.7 V, Duty Cycle = 50% ±10%	dc		12	MHz
	V_{CC} ≥ 3.3 V, Duty Cycle = 50% ±10%	dc		16	MHz

NOTES: 1. The MSP430 CPU is clocked directly with MCLK.
Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
2. Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Save Operating Area

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

active mode supply current (into V_{CC}) excluding external current (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,\ 1MHz}$	Active mode (AM) current (1MHz)	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1MHz, f_{ACLK} = 32,768Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		220		µA
				3 V		300	370	

NOTES: 1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
2. The currents are characterized with a Micro Crystal CC4V–T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9pF.

typical characteristics – active mode supply current (into V_{CC})

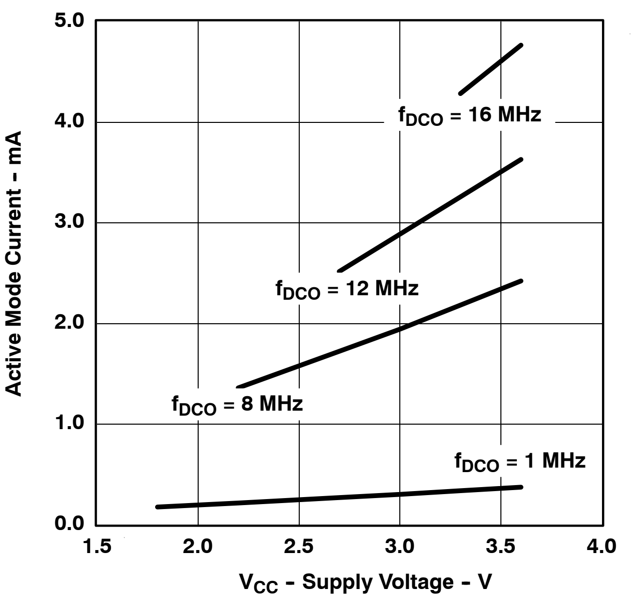

Figure 2. Active mode current vs V_{CC}, T_A = 25°C

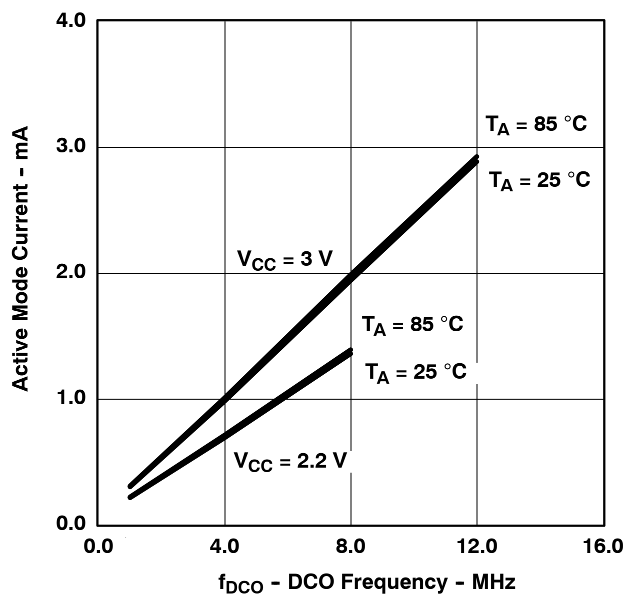

Figure 3. Active mode current vs DCO frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

low-power mode supply currents (into V_{CC}) excluding external current (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0, 1MHz}$	Low-power mode 0 (LPM0) current, see Note 3	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	25°C	2.2 V		65		μA
I_{LPM2}	Low-power mode 2 (LPM2) current, see Note 4	f_{MCLK} = f_{SMCLK} = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32,768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		22		μA
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current, see Note 4	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32,768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		0.7	1.5	μA
$I_{LPM3,VLO}$	Low-power mode 3 current, (LPM3) see Note 4	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		0.5	0.7	μA
I_{LPM4}	Low-power mode 4 (LPM4) current, see Note 5	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	25°C	2.2 V		0.1	1.5	μA
			85°C	2.2 V		0.8	1.5	μA

NOTES:
1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
2. The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF.
3. Current for brownout and WDT clocked by SMCLK included.
4. Current for brownout and WDT clocked by ACLK included.
5. Current for brownout included.

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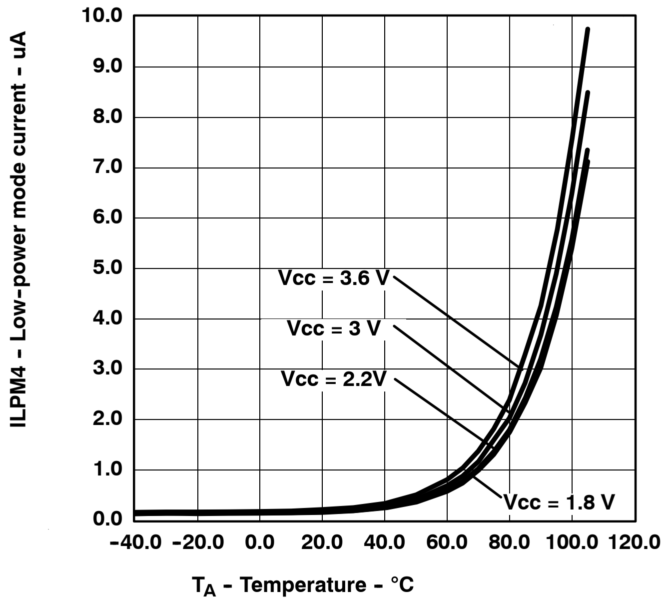
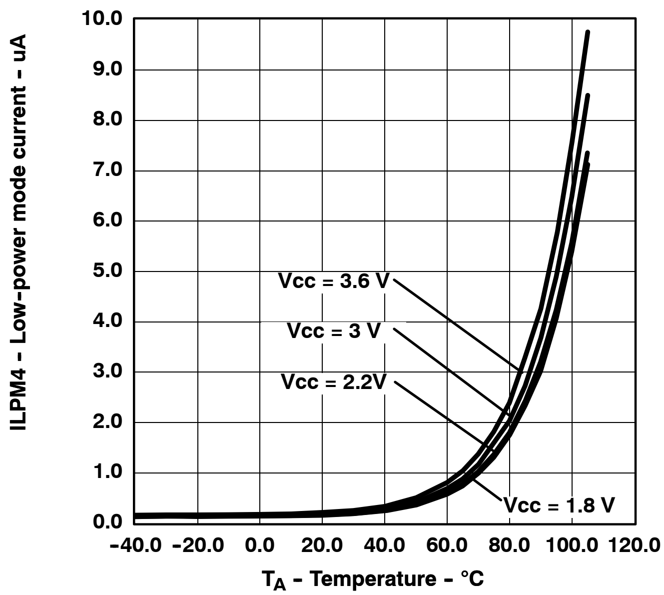
electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – LPM3 current



typical characteristics – LPM4 current



PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs − Ports Px

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45		0.75	V_{CC}
			3 V	1.35		2.25	V
V_{IT-}	Negative-going input threshold voltage			0.25		0.55	V_{CC}
			3 V	0.75		1.65	V
V_{hys}	Input voltage hysteresis (V_{IT+} − V_{IT-})		3 V	0.3		1.0	V
R_{Pull}	Pull-up/pull-down resistor	For pullup: $V_{IN} = V_{SS}$; For pulldown: $V_{IN} = V_{CC}$	3V	20	35	50	kΩ
C_I	Input Capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

NOTES: 1. An external signal sets the interrupt flag every time the minimum interrupt puls width $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.

leakage current − Ports Px

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	see Notes 1 and 2	3 V			±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The leakage of the digital port pins is measured individually. The port pin is selected for input and the pull-up/pull-down resistor is disabled.

outputs − Ports Px

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = −6 mA (see Notes 2)	3 V		V_{CC}−0.3		V
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 6 mA (see Notes 2)	3 V		V_{SS}+0.3		V

NOTES: 1. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
2. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

output frequency − Ports Px

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	Px.y, C_L = 20 pF, R_L = 1 kOhm (see Note 1 and 2)	3 V		12		MHz
f_{Port_CLK}	Clock output frequency	Px.y, C_L = 20 pF (see Note 2)	3 V		16		MHz

NOTES: 1. A resistive divider with 2 times 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
2. The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – outputs

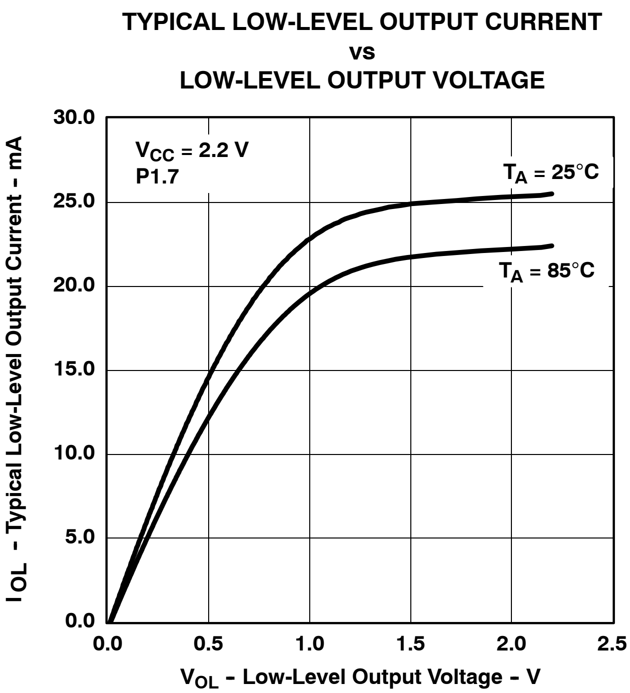

Figure 4

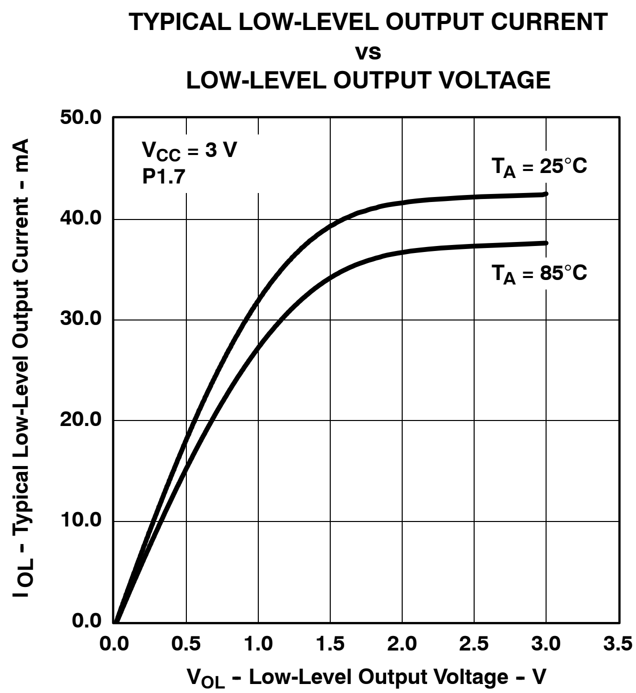

Figure 5

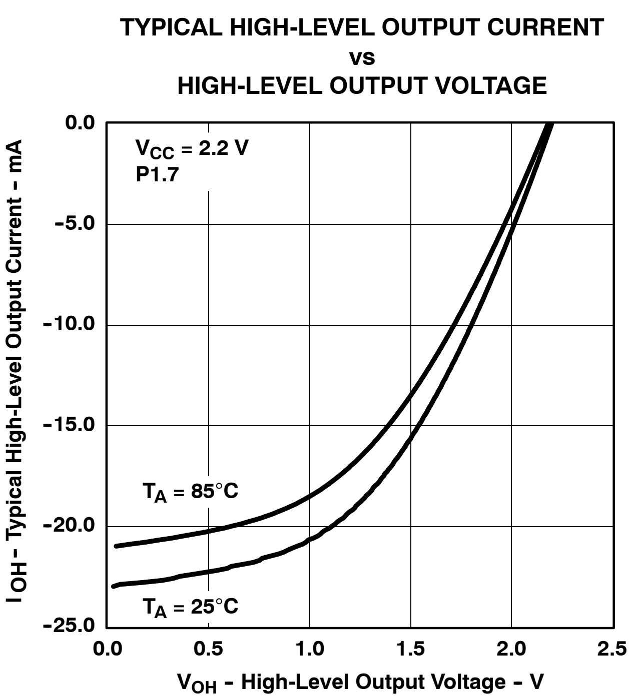

Figure 6

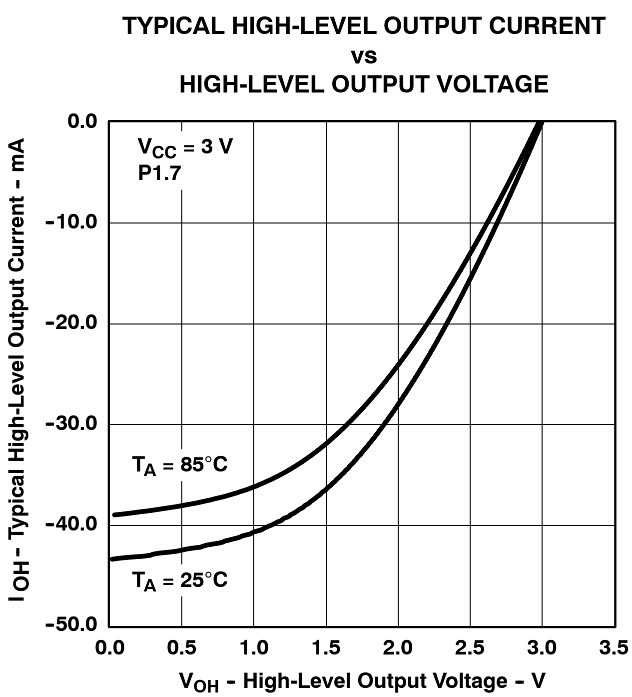

Figure 7

NOTE: One output loaded at a time.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

POR/brownout reset (BOR) (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	(see Figure 8)	$dV_{CC}/dt \leq 3$ V/s			$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	(see Figure 8 through Figure 10)	$dV_{CC}/dt \leq 3$ V/s			1.35		V
$V_{hys(B\_IT-)}$	(see Figure 8)	$dV_{CC}/dt \leq 3$ V/s			140		mV
$t_{d(BOR)}$	(see Figure 8)					2000	µs
$t_{(reset)}$	Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally		2.2 V/3 V	2			µs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is $\leq$ 1.8V.
2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \geq V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

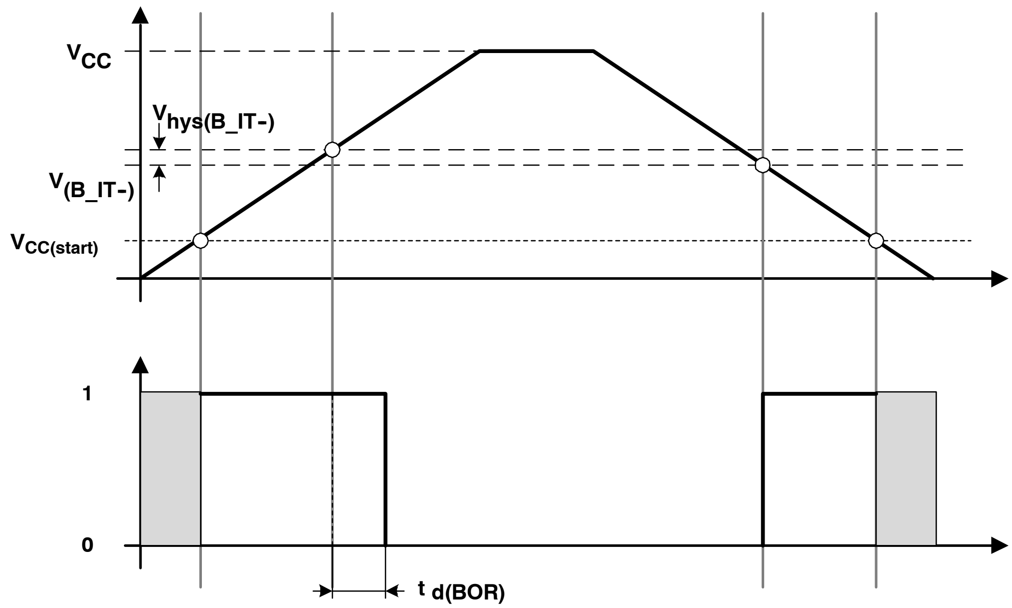

Figure 8. POR/Brownout Reset (BOR) vs Supply Voltage

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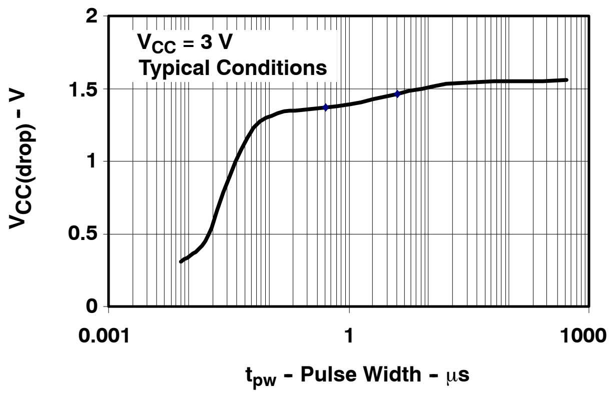
electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics – POR/brownout reset (BOR)



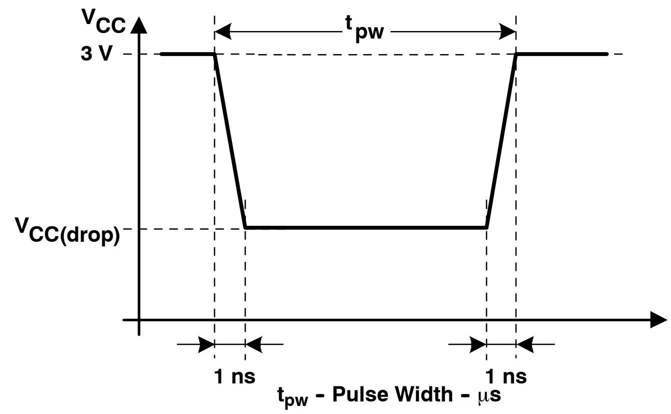
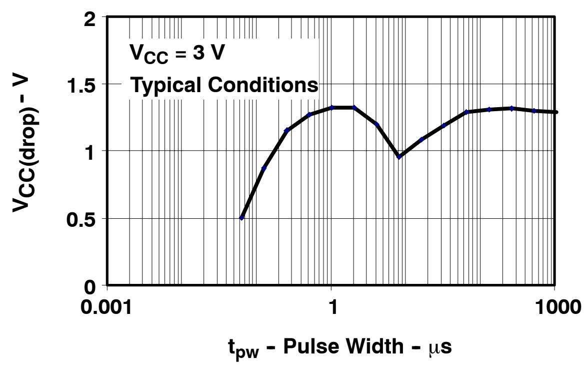


Figure 9. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal



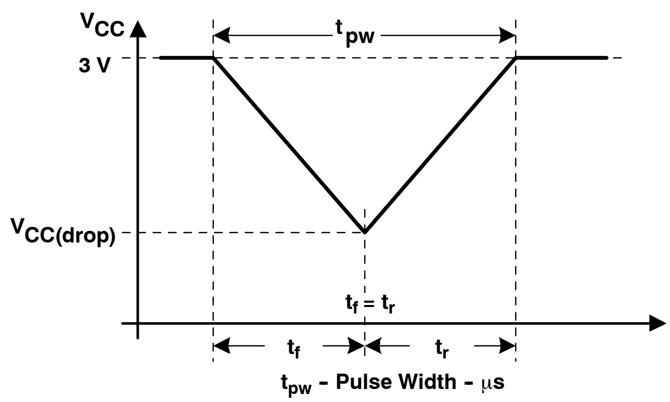


Figure 10. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

DCO frequency

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Vcc	Supply voltage range	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	V
		RSELx = 15		3.0		3.6	V
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	3 V		0.12		MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	3 V		0.15		MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	3 V		0.21		MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	3 V		0.30		MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	3 V		0.41		MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	3 V		0.58		MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	3 V		0.80		MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	3 V		1.60		MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	3 V		2.30		MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	3 V		3.40		MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	3 V		4.25		MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	3 V	4.30		7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	3 V		7.80		MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	3 V	8.60		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V		15.25		MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V		21.00		MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	3 V		1.35		ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	3 V		1.08		ratio
Duty Cycle		Measured at SMCLK output	3 V		50		%

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

calibrated DCO frequencies – tolerance

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1 MHz tolerance over temperature (see Note 1)	BCSCTL1= CALBC1_1MHz DCOCTL = CALDCO_1MHz calibrated at 30°C and 3.0V	0°C to 85°C	3.0 V	−3	±0.5	+3	%
1 MHz tolerance over V_{CC}	BCSCTL1= CALBC1_1MHz DCOCTL = CALDCO_1MHz calibrated at 30°C and 3.0V	30°C	1.8 V – 3.6 V	−3	±2	+3	%
1 MHz tolerance overall	BCSCTL1= CALBC1_1MHz DCOCTL = CALDCO_1MHz calibrated at 30°C and 3.0V	−40°C to 85°C	1.8 V – 3.6 V	−6	±3	+6	%

NOTES: 1. This is the frequency change from the measured frequency at 30°C over temperature.

wake-up from low-power modes (LPM3/4)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3/4 (see Note 1)	BCSCTL1= CALBC1_1MHz DCOCTL = CALDCO_1MHz	3 V		1.5		μs
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3/4 (see Note 2)				$1/f_{MCLK}$ + $t_{Clock,LPM3/4}$		

NOTES: 1. The DCO clock wake-up time is measured from the edge of an external wake-up signal (e.g. port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
2. Parameter applicable only if DCOCLK is used for MCLK.

typical characteristics – DCO clock wake-up time from LPM3/4

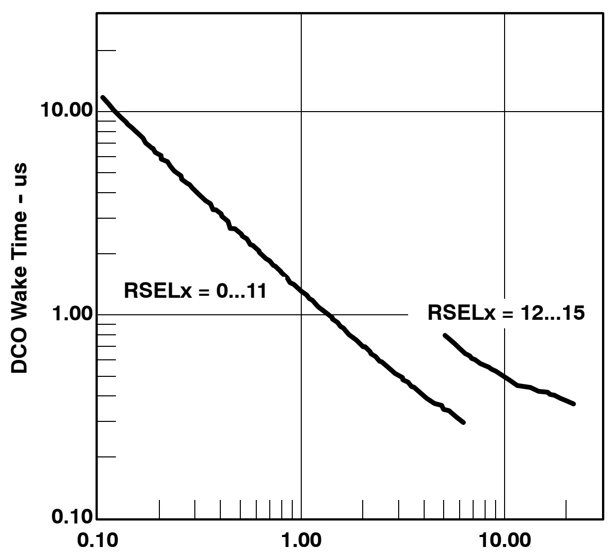

Figure 11. DCO wake-up time from LPM3 vs DCO frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1, low frequency modes (see Note 4)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, XCAPx = 0, LFXT1Sx = 3	1.8 V to 3.6 V	10000	32768	50000	Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 6 pF			500		kΩ
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32,768 kHz, $C_{L,eff}$ = 12 pF			200		kΩ
$C_{L,eff}$	Integrated effective load capacitance, LF mode (see Note)	XTS = 0, XCAPx = 0			1		pF
$C_{L,eff}$		XTS = 0, XCAPx = 1			5.5		pF
$C_{L,eff}$		XTS = 0, XCAPx = 2			8.5		pF
$C_{L,eff}$		XTS = 0, XCAPx = 3			11		pF
Duty cycle	LF mode	XTS = 0, Measured at P2.0/ACLK, $f_{LFXT1,LF}$ = 32,768Hz	2.2 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode (see Note 3)	XTS = 0, XCAPx = 0. LFXT1Sx = 3 (see Note 2)	2.2 V	10		10000	Hz

NOTES:
1. Includes parasitic bond and package capacitance (approximately 2 pF per pin).
   Since the PCB adds additional capacitance it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup the effective load capacitance should always match the specification of the used crystal.
2. Measured with logic level input frequency but also applies to operation with crystals.
3. Frequencies below the MIN specification set the fault flag, frequencies above the MAX specification do not set the fault flag, and frequencies in between might set the flag.
4. To improve EMI on the LFXT1 oscillator the following guidelines should be observed.
   - Keep the trace between the device and the crystal as short as possible.
   - Design a good ground plane around the oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

internal very low power, low frequency oscillator (VLO)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency		-40 − 85°C	3.0 V	4	12	20	kHz
df_{VLO}/dT	VLO frequency temperature drift		-40 − 85°C	3.0 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift		25°C	1.8 V − 3.6 V		4		%/V

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Timer_A

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK; External: TACLK, INCLK; Duty Cycle = 50% ±10%			f_{SYSTEM}		MHz
$t_{TA,cap}$	Timer_A, capture timing	TA0, TA1	3.0 V	20			ns

USI, Universal Serial Interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USI}	USI clock frequency	External: SCLK; Duty Cycle = 50% ±10%; SPI Slave Mode			f_{SYSTEM}		MHz
$V_{OL,I2C}$	Low-level output voltage on SDA and SCL	USI module in I2C mode $I_{(OLmax)}$ = 1.5 mA	3.0 V	V_{SS}		V_{SS}+0.4	V

typical characteristics – USI low-level output voltage on SDA and SCL

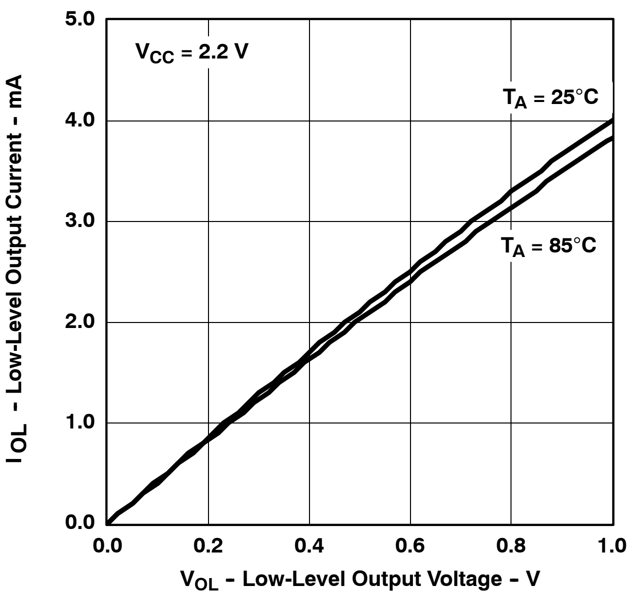

Figure 12. USI Low-Level Output Voltage vs. Output Current

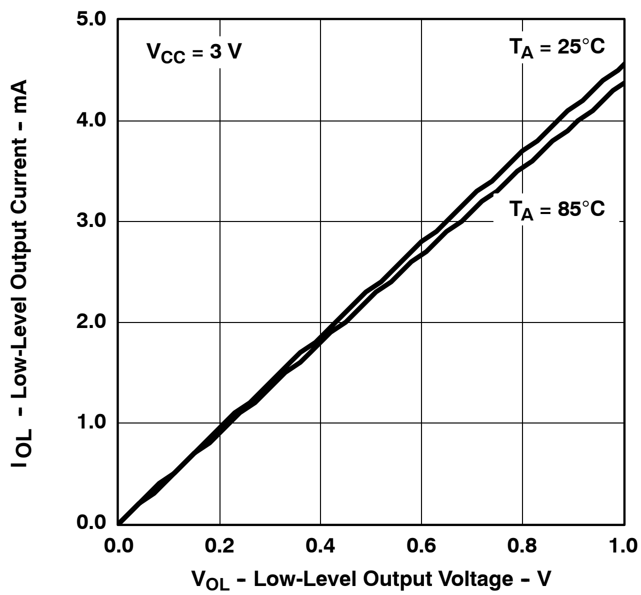

Figure 13. USI Low-Level Output Voltage vs. Output Current

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, power supply and input range conditions − MSP430G2x31 only

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Analog supply voltage range	V_{SS} = 0 V			2.2		3.6	V
V_{Ax}	Analog input voltage range (see Note 2)	All Ax terminals. Analog inputs selected in ADC10AE register.		3 V	0		V_{CC}	V
I_{ADC10}	ADC10 supply current (see Note 3)	$f_{ADC10CLK}$ = 5.0 MHz ADC10ON = 1, REFON = 0 ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	25°C	3 V		0.6		mA
I_{REF+}	Reference supply current, reference buffer disabled (see Note 4)	$f_{ADC10CLK}$ = 5.0 MHz ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0	25°C	3 V		0.25		mA
		$f_{ADC10CLK}$ = 5.0 MHz ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0	25°C					
$I_{REFB,0}$	Reference buffer supply current with ADC10SR=0 (see Note 4)	$f_{ADC10CLK}$ = 5.0 MHz ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR=0	25°C	3 V		1.1		mA
$I_{REFB,1}$	Reference buffer supply current with ADC10SR=1 (see Note 4)	$f_{ADC10CLK}$ = 5.0 MHz ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR=1	25°C	3 V		0.5		mA
C_I	Input capacitance	Only one terminal Ax selected at a time	25°C	3 V			27	pF
R_I	Input MUX ON resistance	0V ≤ V_{Ax} ≤ V_{CC}	25°C	3 V		1000		Ω

NOTES: 1. The leakage current is defined in the leakage current table with Px.x/Ax parameter.
2. The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
3. The internal reference supply current is not included in current consumption parameter I_{ADC10}.
4. The internal reference current is supplied via terminal V_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, built-in voltage reference – MSP430G2x31 only

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC,REF+}$	Positive built-in reference analog supply voltage range	I_{VREF+} ≤ 1mA, REF2_5V=0			2.2			V
		I_{VREF+} ≤ 1mA, REF2_5V=1			2.9			
V_{REF+}	Positive built-in reference voltage	I_{VREF+} ≤ I_{VREF+}max, REF2_5V = 0		3 V	1.41	1.5	1.59	V
		I_{VREF+} ≤ I_{VREF+}max, REF2_5V = 1		3 V	2.35	2.5	2.65	V
$I_{LD,VREF+}$	Maximum V_{REF+} load current			3 V			±1	mA
	V_{REF+} load regulation	I_{VREF+} = 500 µA +/– 100 µA Analog input voltage V_{Ax} ≈ 0.75 V; REF2_5V = 0		3 V			±2	LSB
		I_{VREF+} = 500 µA ± 100 µA Analog input voltage V_{Ax} ≈ 1.25 V; REF2_5V = 1		3 V			±2	LSB
	V_{REF+} load regulation response time	I_{VREF+} = 100µA→900µA, V_{Ax} ≈ 0.5 x V_{REF+} Error of conversion result ≤ 1 LSB	ADC10SR = 0	3 V			400	ns
C_{VREF+}	Max. capacitance at pin V_{REF+}	I_{VREF+} ≤ ±1mA, REFON = 1, REFOUT = 1		3 V			100	pF
TC_{REF+}	Temperature coefficient	I_{VREF+} = const. with 0 mA ≤ I_{VREF+} ≤ 1 mA		3 V			±100	ppm/°C
t_{REFON}	Settling time of internal reference voltage to 99.9% VREF	I_{VREF+} = 0.5 mA, REF2_5V=0 REFON = 0 → 1,		3.6 V			30	µs
$t_{REFBURST}$	Settling time of reference buffer to 99.9% VREF	I_{VREF+} = 0.5 mA, REF2_5V=1, REFON = 1, REFBURST = 1	ADC10SR = 0	3 V			2	µs

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, external reference − MSP430G2x31 only

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$VEREF_+$	Positive external reference input voltage range (see Note 2)	$VEREF_+ > VEREF_-$ SREF1 = 1, SREF0 = 0		1.4		V_{CC}	V
		$VEREF_- \le VEREF_+ \le V_{CC} - 0.15V$ SREF1 = 1, SREF0 = 1 (see Note 3)		1.4		3.0	V
$VEREF_-$	Negative external reference input voltage range (see Note 4)	$VEREF_+ > VEREF_-$		0		1.2	V
ΔVEREF	Differential external reference input voltage range ΔVEREF = $VEREF_+ - VEREF_-$	$VEREF_+ > VEREF_-$ (see Note 5)		1.4		V_{CC}	V
I_{VEREF+}	Static input current into $VEREF_+$	$0V \le VEREF_+ \le V_{CC}$, SREF1 = 1, SREF0 = 0	3 V		±1		µA
		$0V \le VEREF_+ \le V_{CC} - 0.15V \le 3V$ SREF1 = 1, SREF0 = 1 (see Note 3)	3 V		0		µA
I_{VEREF-}	Static input current into $VEREF_-$	$0V \le VEREF_- \le V_{CC}$	3 V		±1		µA

NOTES: 1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
3. Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.
4. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
5. The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, timing parameters – MSP430G2x31 only

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$	ADC10 input clock frequency	For specified performance of ADC10 linearity parameters	ADC10SR = 0	3 V	0.45		6.3	MHz
			ADC10SR = 1	3 V	0.45		1.5	
$f_{ADC10OSC}$	ADC10 built-in oscillator frequency	ADC10DIVx=0, ADC10SSELx = 0 $f_{ADC10CLK} = f_{ADC10OSC}$		3 V	3.7		6.3	MHz
$t_{CONVERT}$	Conversion time	ADC10 built-in oscillator, ADC10SSELx = 0 $f_{ADC10CLK} = f_{ADC10OSC}$		3 V	2.06		3.51	μs
		$f_{ADC10CLK}$ from ACLK, MCLK or SMCLK: ADC10SSELx ≠ 0				13× ADC10DIV× 1/$f_{ADC10CLK}$		μs
$t_{ADC10ON}$	Turn on settling time of the ADC	(see Note 1)					100	ns

NOTES: 1. The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

10-bit ADC, linearity parameters – MSP430G2x31 only

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error		3 V			±1	LSB
E_D	Differential linearity error		3 V			±1	LSB
E_O	Offset error	Source impedance R_S < 100 Ω,	3 V			±1	LSB
E_G	Gain error		3 V		±1.1	±2	LSB
E_T	Total unadjusted error		3 V		±2	±5	LSB

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

10-bit ADC, temperature sensor and built-in V_{MID} - MSP430G2x31 only

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Temperature sensor supply current (see Note 1)	REFON = 0, INCHx = 0Ah, T_A = 25°C	3 V		60		µA
TC_{SENSOR}		ADC10ON = 1, INCHx = 0Ah (see Note 2)	3 V		3.55		mV/°C
$t_{Sensor(sample)}$	Sample time required if channel 10 is selected (see Note 4)	ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB	3 V	30			µs
I_{VMID}	Current into divider at channel 11 (see Note 5)	ADC10ON = 1, INCHx = 0Bh,	3 V			NA	µA
V_{MID}	V_{CC} divider at channel 11	ADC10ON = 1, INCHx = 0Bh, V_{MID} is ≈0.5 x V_{CC}	3 V		1.5		V
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (see Note 6)	ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB	3 V	1220			ns

NOTES:
1. The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1), or (ADC10ON=1 and INCH=0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}. When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).
2. The following formula can be used to calculate the temperature sensor output voltage:
   $V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV] or
   $V_{Sensor,typ} = TC_{Sensor}$ T [°C] + $V_{Sensor}(T_A = 0°C)$ [mV]
3. Values are not based on calculations using TC_{Sensor} or $V_{Offset,sensor}$ but on measurements.
4. The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
5. No additional current is needed. The V_{MID} is used during sampling.
6. The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

flash memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and Erase supply voltage			2.2		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V/3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V/3.6 V		1	7	mA
t_{CPT}	Cumulative program time (see Note 1)		2.2 V/3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V/3.6 V	20			ms
	Program/Erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 2			30		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				25		
$t_{Block, 1-63}$	Block program time for each additional byte or word				18		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				10593		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage (see Note 1)	CPU halted	1.6			V

NOTE 1: This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

JTAG and Spy-Bi-Wire interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency		2.2 V / 3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse length		2.2 V / 3 V	0.025		15	us
$t_{SBW,En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge, see Note 1)		2.2 V/ 3 V			1	us
$t_{SBW,Ret}$	Spy-Bi-Wire return to normal operation time		2.2 V/ 3 V	15		100	us
f_{TCK}	TCK input frequency − 4-wire JTAG (see Note 2)		2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pull-down resistance on TEST		2.2 V/ 3 V	25	60	90	kΩ

NOTES: 1. Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
2. f_{TCK} may be restricted to meet the timing requirements of the module selected.

JTAG fuse (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5			V
V_{FB}	Voltage level on TEST for fuse-blow			6		7	V
I_{FB}	Supply current into TEST during fuse blow					100	mA
t_{FB}	Time to blow fuse					1	ms

NOTES: 1. Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible and JTAG is switched to bypass mode.

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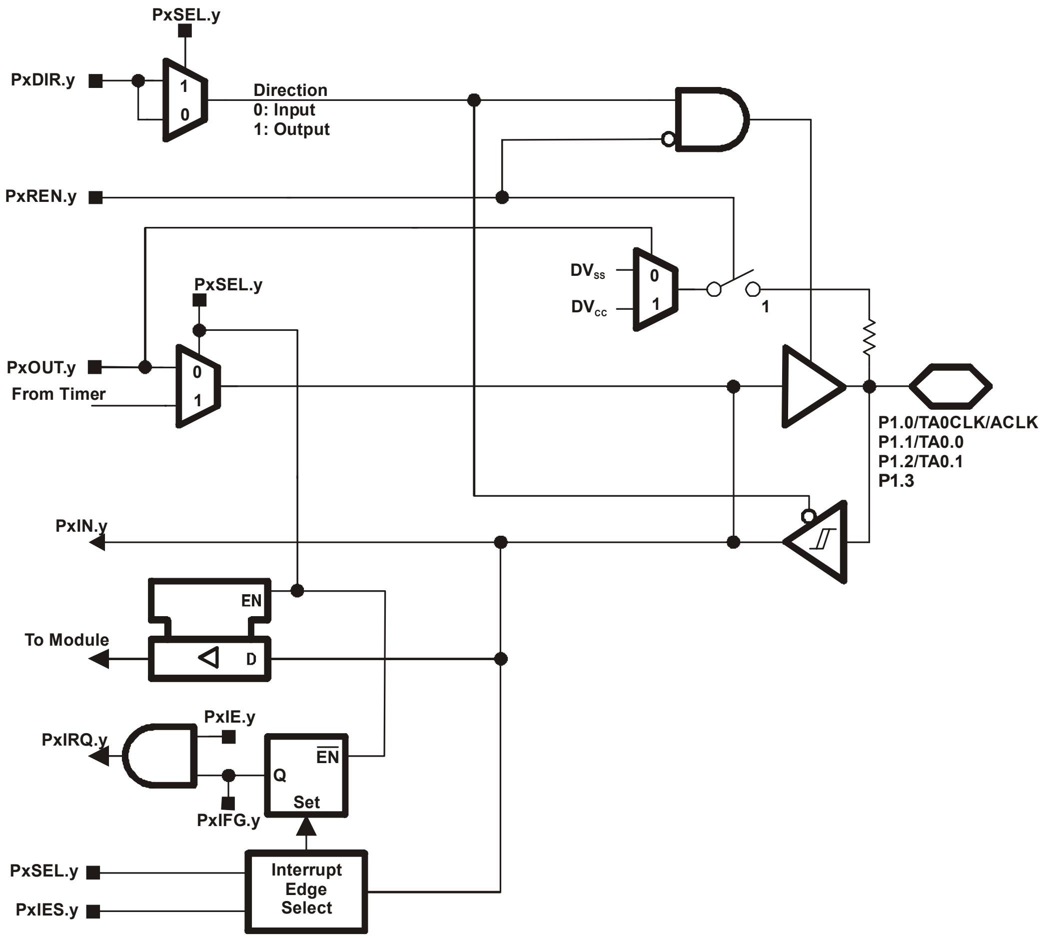
APPLICATION INFORMATION

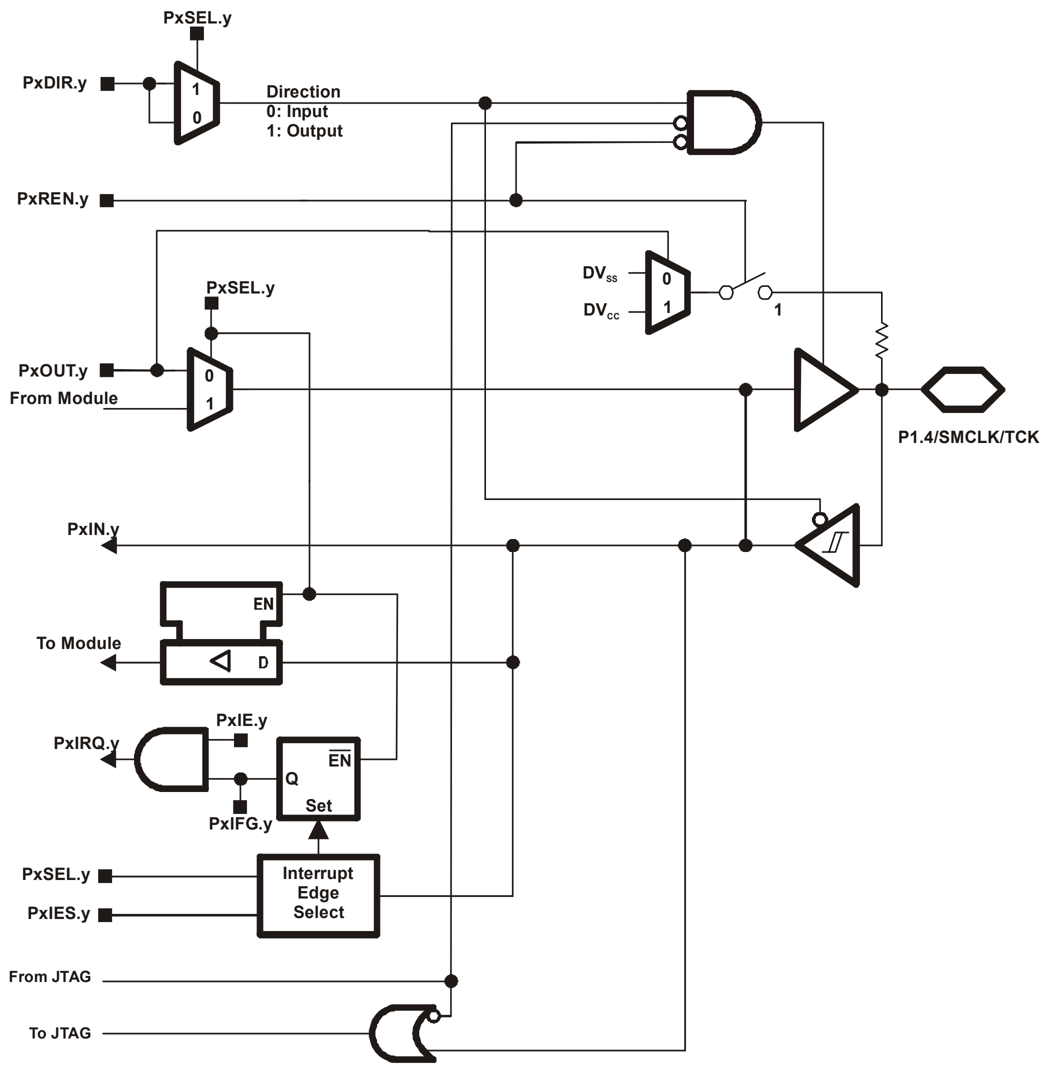
Port P1 pin schematic: P1.0 - P1.3, input/output with Schmitt trigger - MSP430G2x21



Port P1 (P1.0 to P1.3) pin functions - MSP430G2x21

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/	0	P1.x (I/O)	I: 0; O: 1	0
TA0CLK/		TA0.TACLK	0	1
ACLK/		ACLK	1	1
P1.1/	1	P1.x (I/O)	I: 0; O: 1	0
TA0.0/		TA0.0	1	1
		TA0.CCI0A	0	1
P1.2/	2	P1.x (I/O)	I: 0; O: 1	0
TA0.1/		TA0.1	1	1
		TA0.CCI1A	0	1
P1.3/	3	P1.x (I/O)	I: 0; O: 1	0

Port P1 pin schematic: P1.0 – P1.3, input/output with Schmitt trigger – MSP430G2x21



Port P1 (P1.4) pin functions – MSP430G2x21

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P1DIR.x	P1SEL.x	JTAG Mode
P1.4/	4	P1.x (I/O)	I: 0; O: 1	0	0
SMCLK/		SMCLK	1	1	0
TCK		TCK	x	x	1

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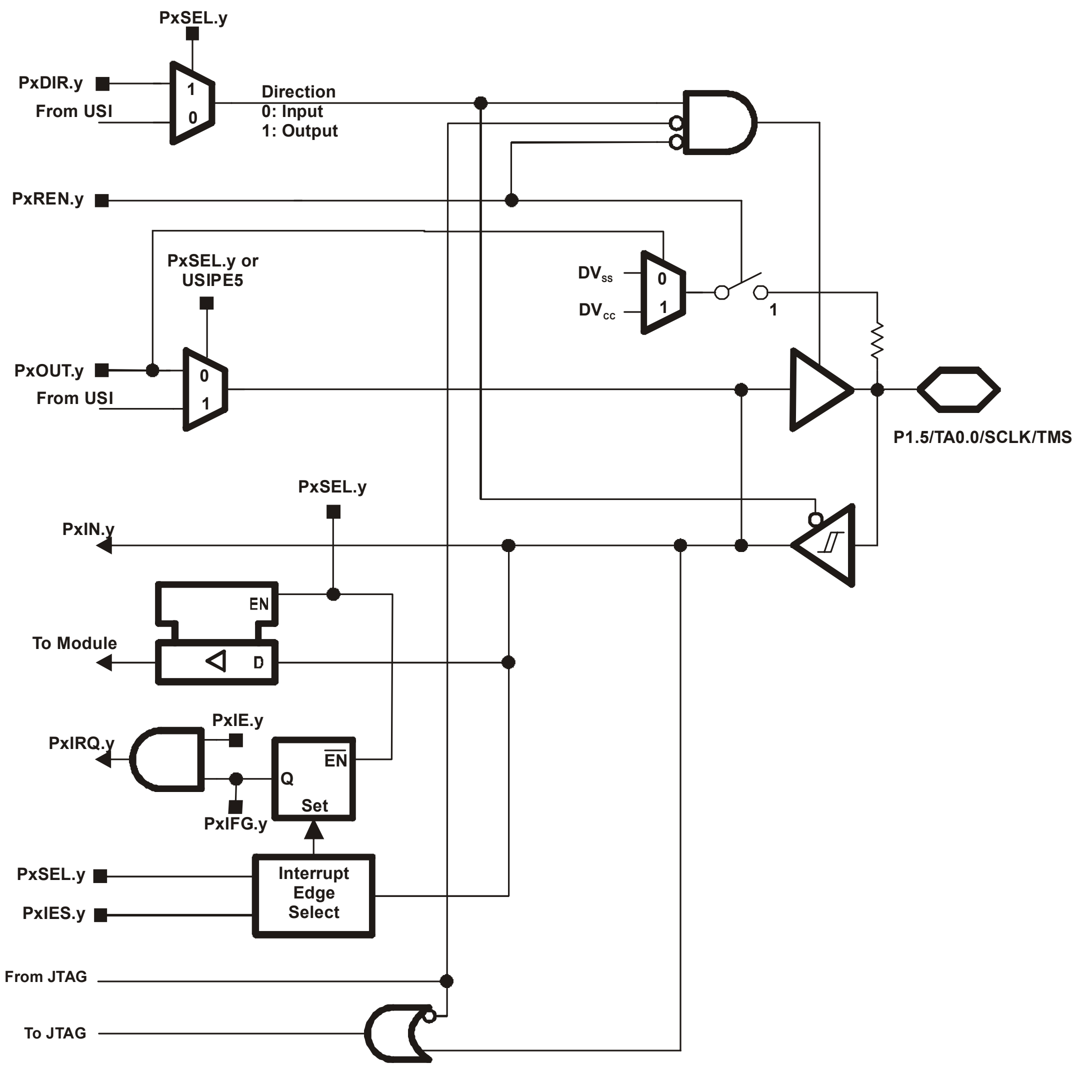
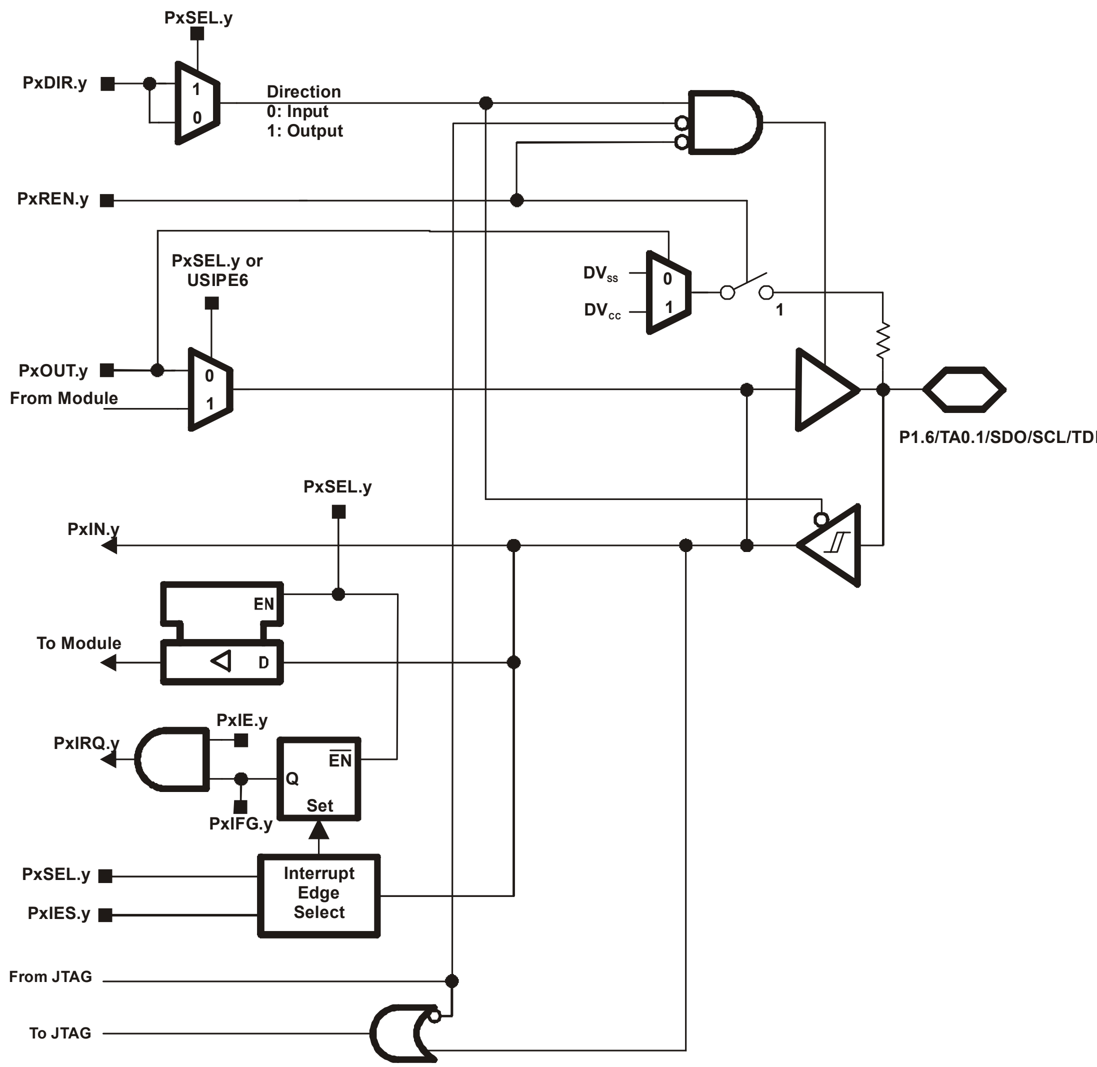
Port P1 pin schematic: P1.5, input/output with Schmitt trigger − MSP430G2x21



Port P1 (P1.5) pin functions − MSP430G2x21

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			P1DIR.x	P1SEL.x	USIP.x	JTAG Mode
P1.5/	5	P1.x (I/O)	I: 0; O: 1	0	0	0
TA0.0/		TA0.0	1	1	0	0
SCLK/		SCLK	x	x	1	0
SIMO0/		SIMO0	x	1	0	0
TMS		TMS	x	x	0	1

Port P1 pin schematic: P1.6, input/output with Schmitt trigger – MSP430G2x21



Port P1 (P1.6) pin functions – MSP430G2x21

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			P1DIR.x	P1SEL.x	USIP.x	JTAG Mode
P1.6/	6	P1.x (I/O)	I: 0; O: 1	0	0	0
TA0.1/		TA0.1	1	1	0	0
SDO/		SDO	x	x	1	0
TDI/TCLK		TDI/TCLK	x	x	0	1

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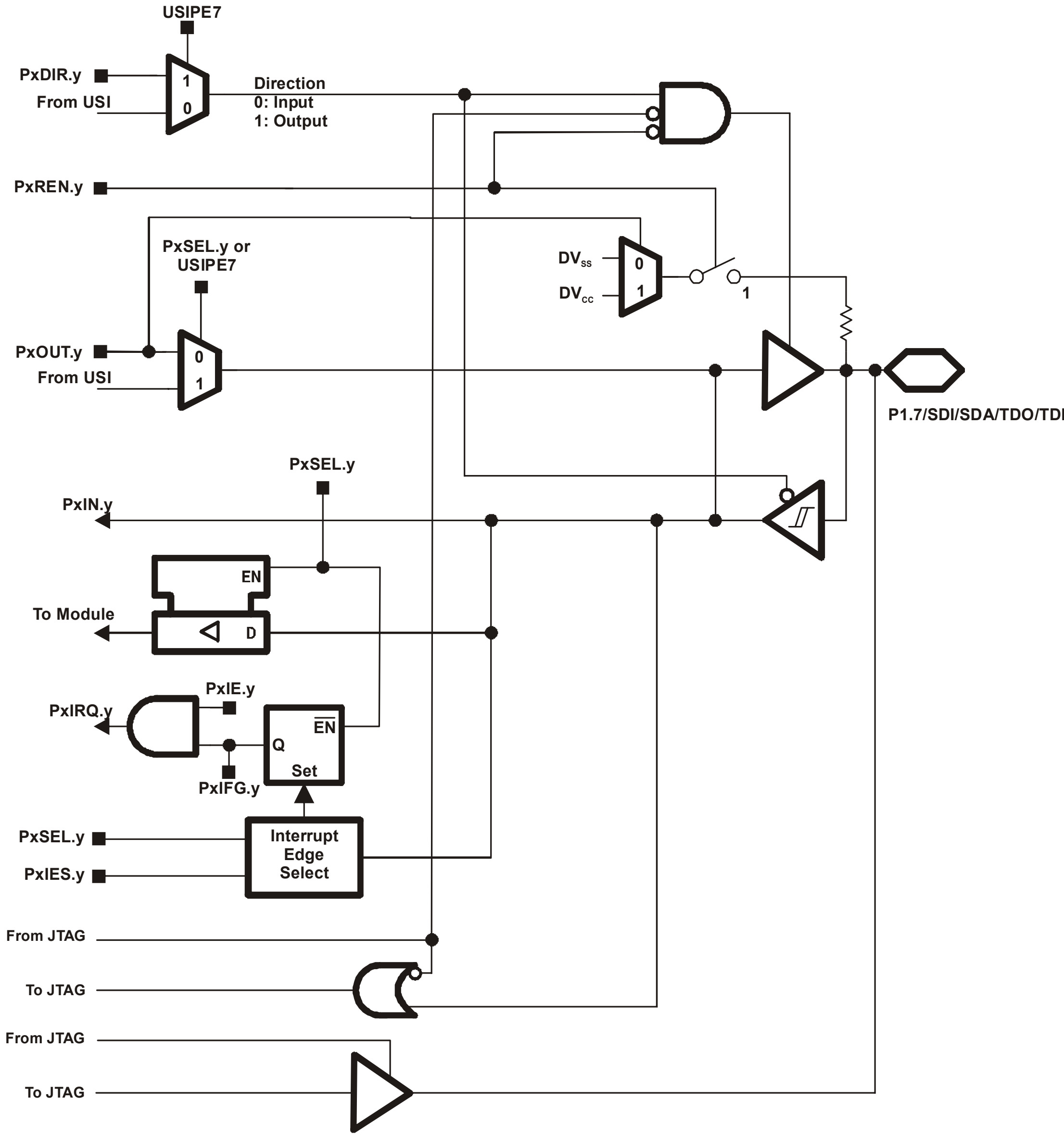
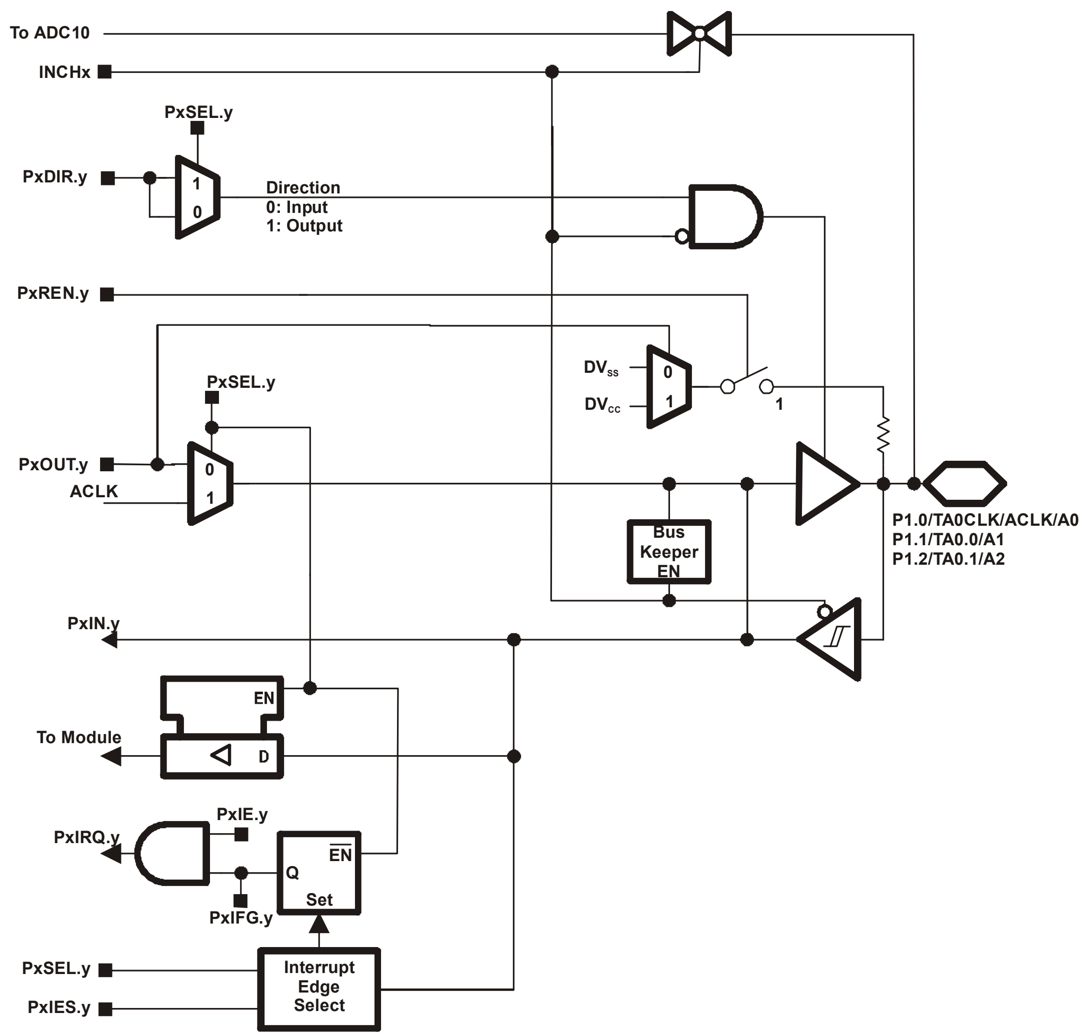
Port P1 pin schematic: P1.7, input/output with Schmitt trigger - MSP430G2x21



Port P1 (P1.7) pin functions - MSP430G2x21

P1.7/	7	P1.x (I/O)	I: 0; O: 1	0	0	0	0
SDI/SDO		SDI/SDO	x	x	1	0	0
TDO/TDI		TDO/TDI	x	x	0	0	1

Port P1 pin schematic: P1.0 – P1.2, input/output with Schmitt trigger – MSP430G2x31



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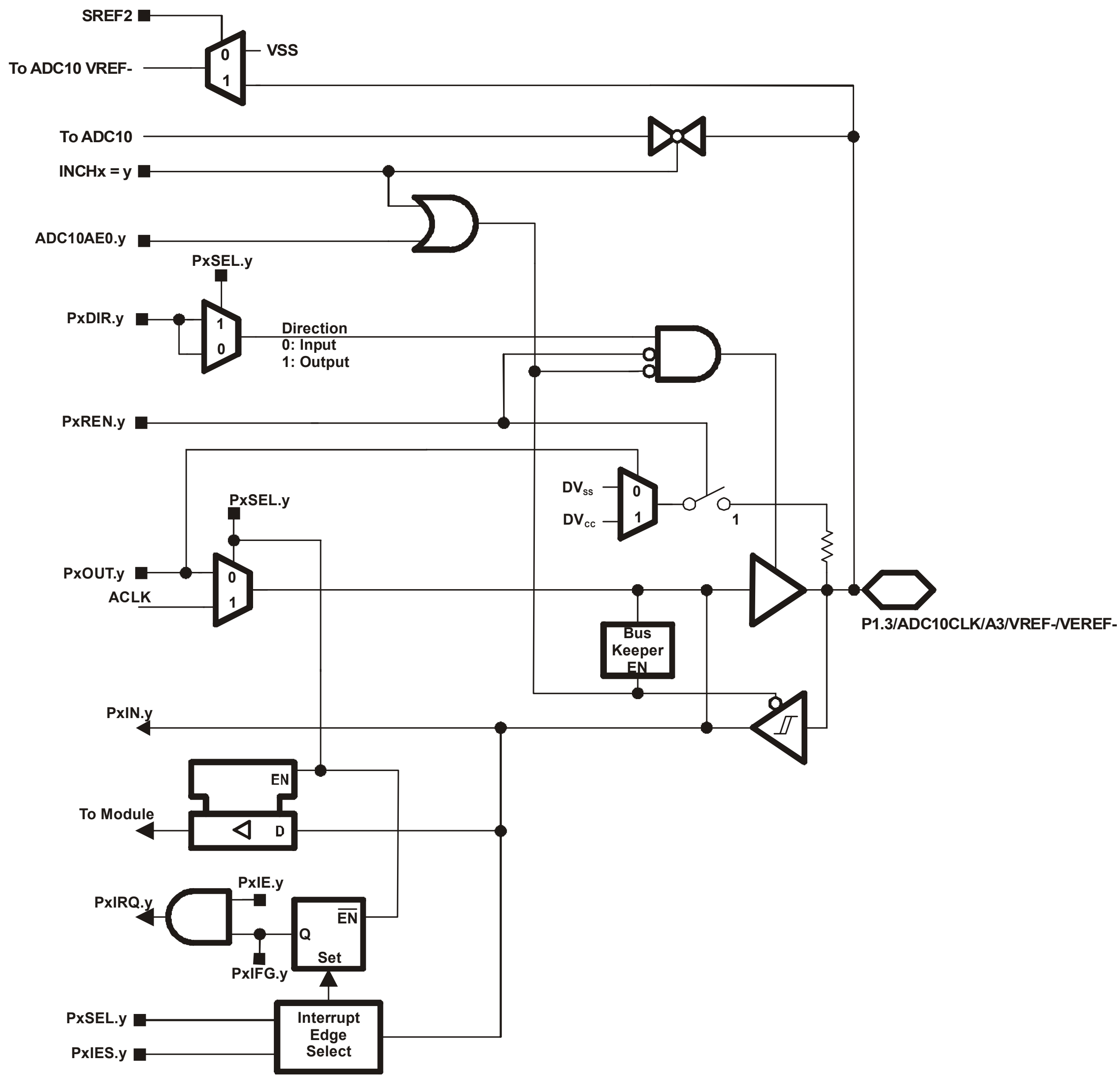
Port P1 (P1.0 to P1.2) pin functions – MSP430G2x31

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P1DIR.x	P1SEL.x	ADC10AE.x (INCH.y = 1)
P1.0/	0	P1.x (I/O)	I: 0; O: 1	0	0
TA0CLK/		TA0.TACLK	0	1	0
ACLK/		ACLK	1	1	0
A0/		A0	x	x	1 (y = 0)
P1.1/	1	P1.x (I/O)	I: 0; O: 1	0	0
TA0.0/		TA0.0	1	1	0
		TA0.CCI0A	0	1	0
A1/		A1	x	x	1 (y = 1)
P1.2/	2	P1.x (I/O)	I: 0; O: 1	0	0
TA0.1/		TA0.1	1	1	0
		TA0.CCI1A	0	1	0
A2/		A2	x	x	1 (y = 2)

PRODUCT PREVIEW

Port P1 pin schematic: P1.3, input/output with Schmitt trigger − MSP430G2x31



Port P1 (P1.3) pin functions − MSP430G2x31

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			P1DIR.x	P1SEL.x	ADC10AE.x (INCH.x = 1)	CAPD.y
P1.3/	3	P1.x (I/O)	I: 0; O: 1	0	0	0
ADC10CLK/		ADC10CLK	1	1	0	0
A3		A3	x	x	1 (y = 3)	0
VREF−/		VREF−	x	x	1	0
VEREF−		VEREF−	x	x	1	0
CA3		CA3	x	x	0	1 (y = 3)

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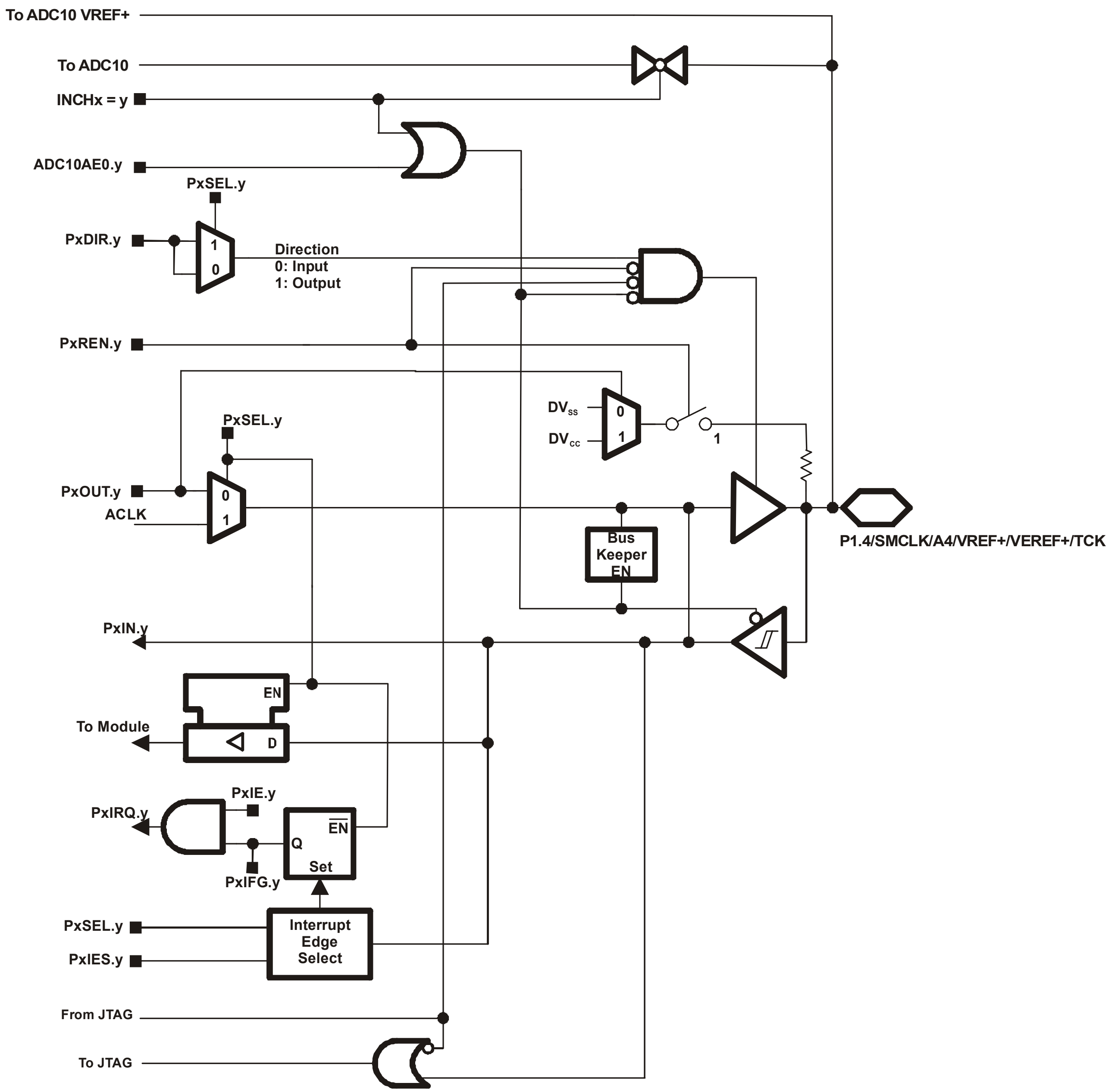
Port P1 pin schematic: P1.4, input/output with Schmitt trigger − MSP430G2x31



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Port P1 (P1.4) pin functions – MSP430G2x31

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			P1DIR.x	P1SEL.x	ADC10AE.x (INCH.x = 1)	JTAG Mode
P1.4/	4	P1.x (I/O)	I: 0; O: 1	0	0	0
SMCLK/		SMCLK	1	1	0	0
A4/		A4	x	x	1 (y = 4)	0
VREF+/		VREF+	x	x	1	0
VEREF+/		VEREF+	x	x	1	0
CA4/		CA4	x	x	0	0
TCK		TCK	x	x	0	1

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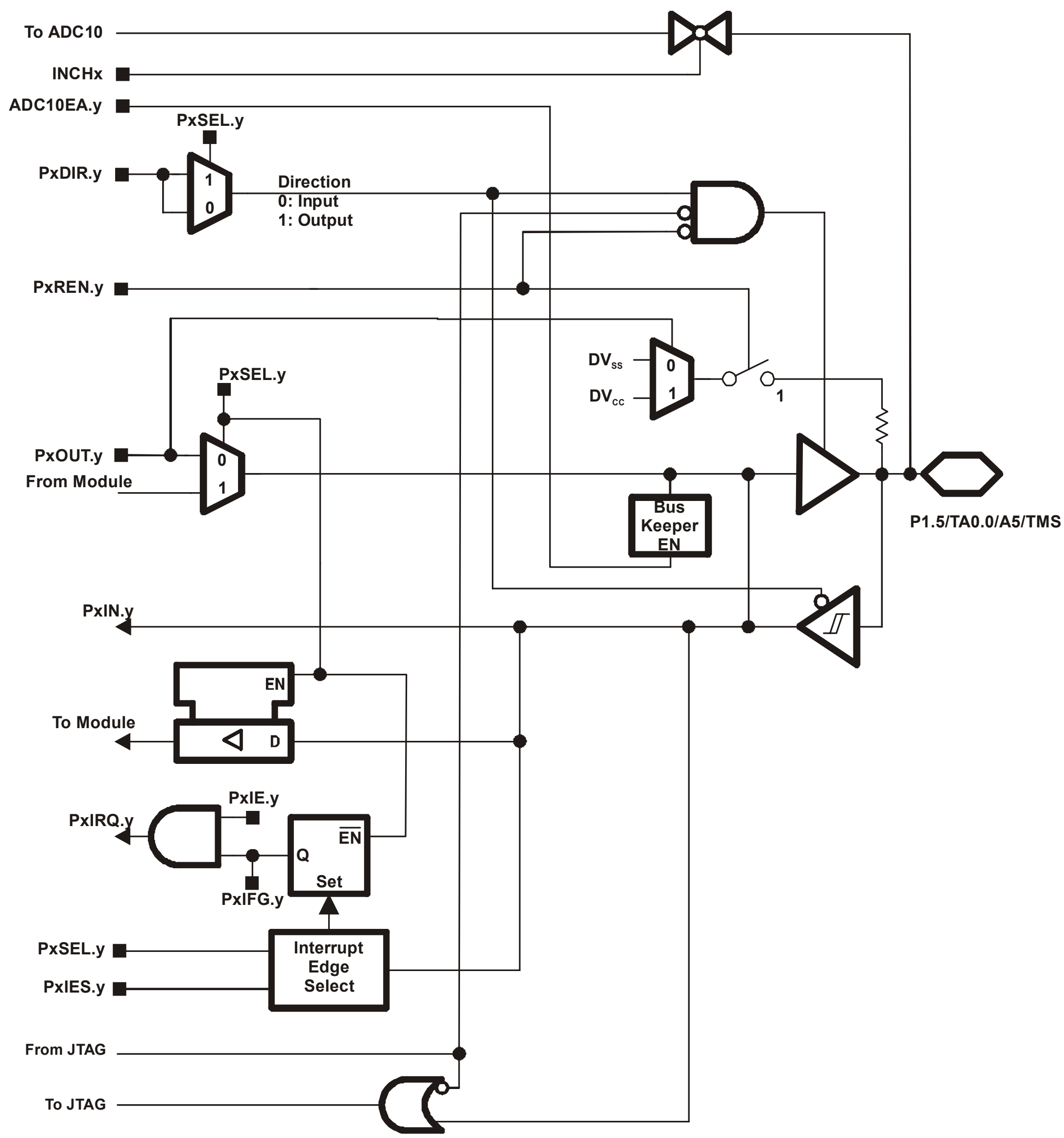
Port P1 pin schematic: P1.5, input/output with Schmitt trigger − MSP430G2x31



Port P1 (P1.5) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			P1DIR.x	P1SEL.x	USIP.x	ADC10AE.x (INCH.x = 1)	JTAG Mode
P1.5/	5	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.0/		TA0.0	1	1	0	0	0
A5/		A5	x	x	0	1 (y = 5)	0
SCLK/		SCLK	x	x	1	0	0
SIMO0/		SIMO0	x	1	0	0	0
TMS		TMS	x	x	0	0	1

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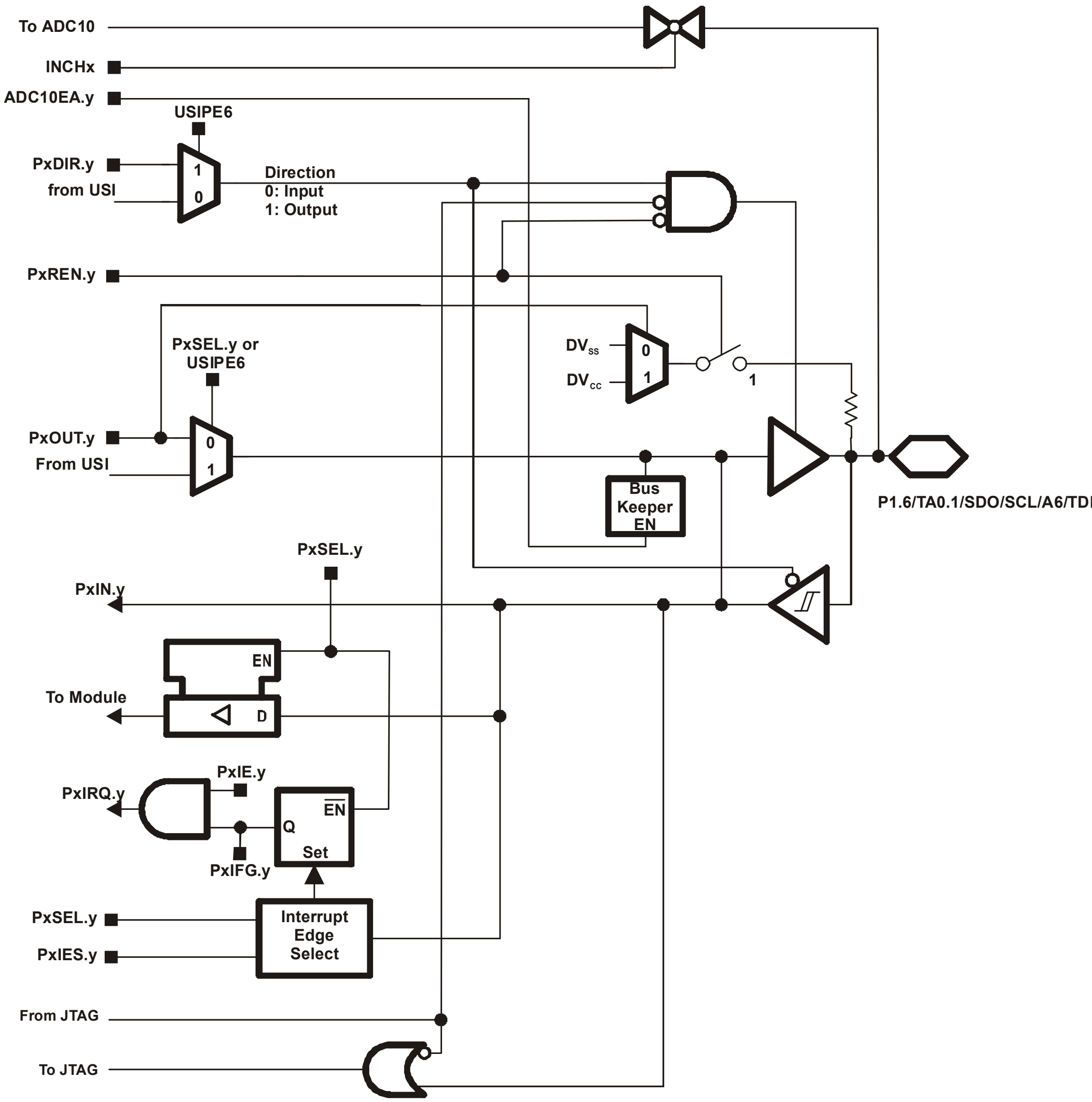
Port P1 pin schematic: P1.6, input/output with Schmitt trigger − MSP430G2x31



USI in I2C mode: Output driver drives low level only. Driver is disabled in JTAG mode.

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Port P1 (P1.6) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			P1DIR.x	P1SEL.x	USIP.x	ADC10AE.x (INCH.x = 1)	JTAG Mode
P1.6/	6	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.1/		TA0.1	1	1	0	0	0
A6/		A6	x	x	0	1 (y = 6)	0
SDO/		SDO	x	x	1	0	0
TDI/TCLK		TDI/TCLK	x	x	0	0	1

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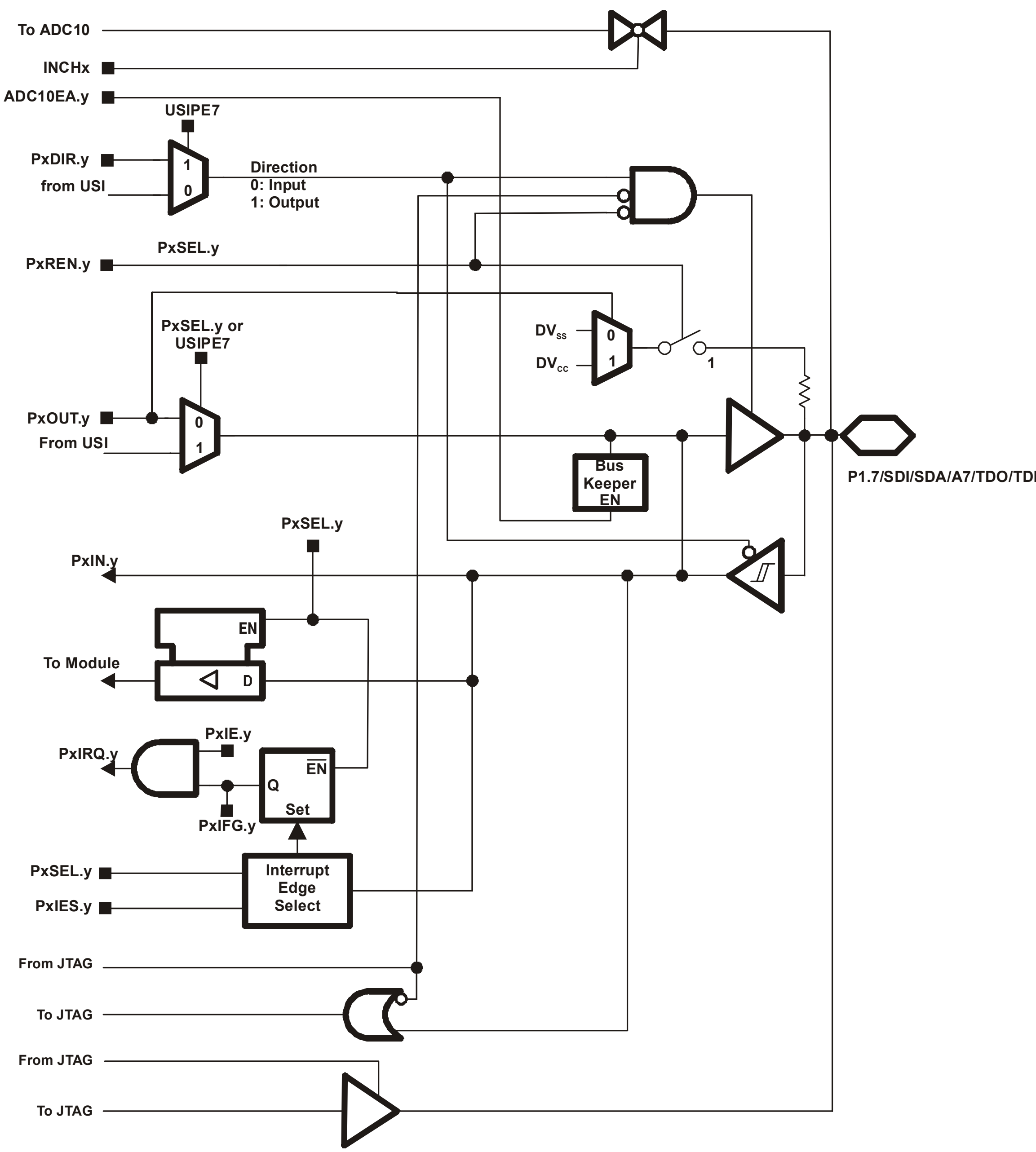
Port P1 pin schematic: P1.7, input/output with Schmitt trigger − MSP430G2x31



USI in I2C mode: Output driver drives low level only. Driver is disabled in JTAG mode.

Port P1 (P1.7) pin functions – MSP430G2x31

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			P1DIR.x	P1SEL.x	USIP.x	ADC10AE.x (INCH.x = 1)	JTAG Mode
P1.7/	7	P1.x (I/O)	I: 0; O: 1	0	0	0	0
A7/		A7	x	x	0	1 (y = 7)	0
SDI/SDO		SDI/SDO	x	x	1	0	0
TDO/TDI		TDO/TDI	x	x	0	0	1

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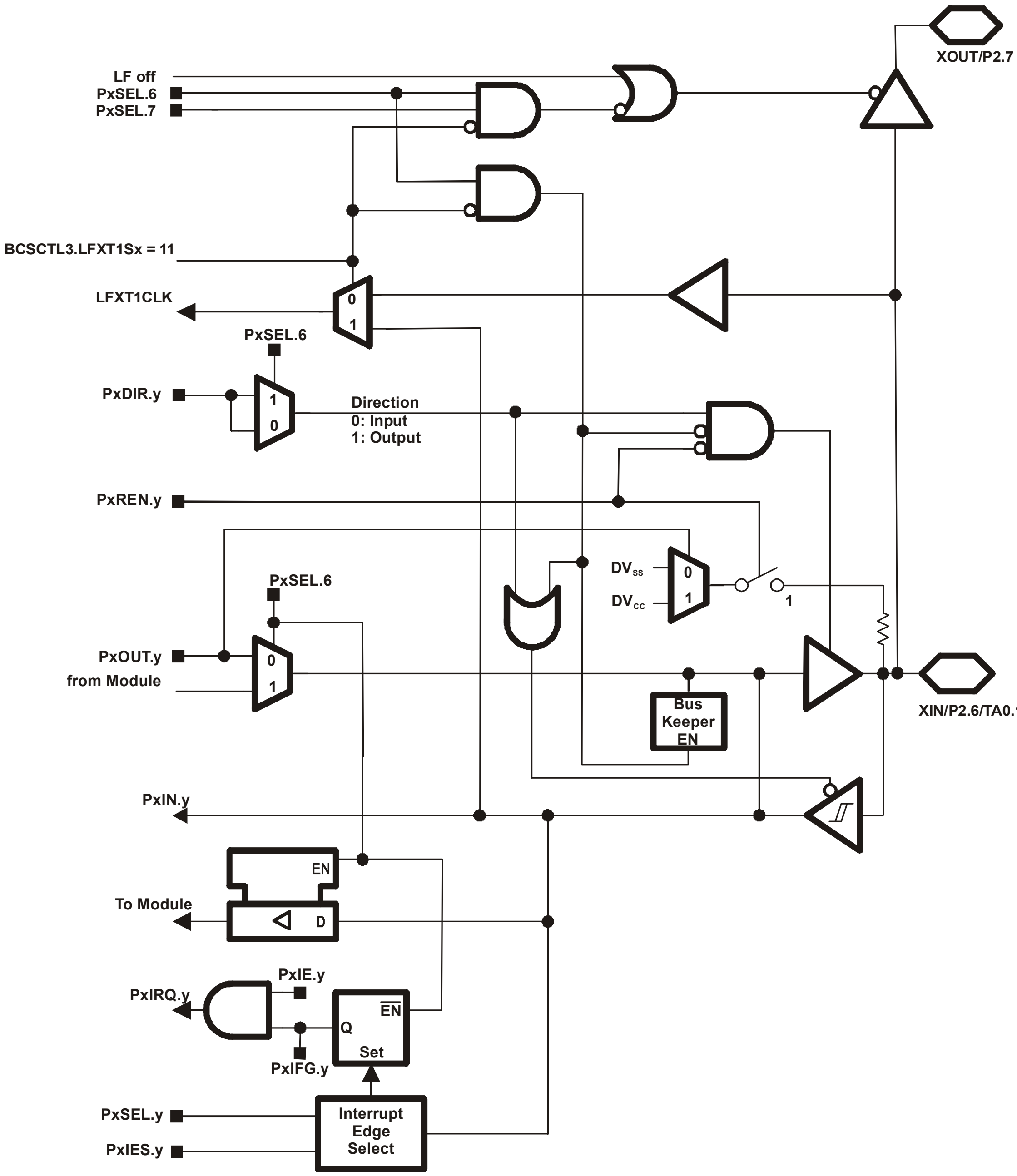
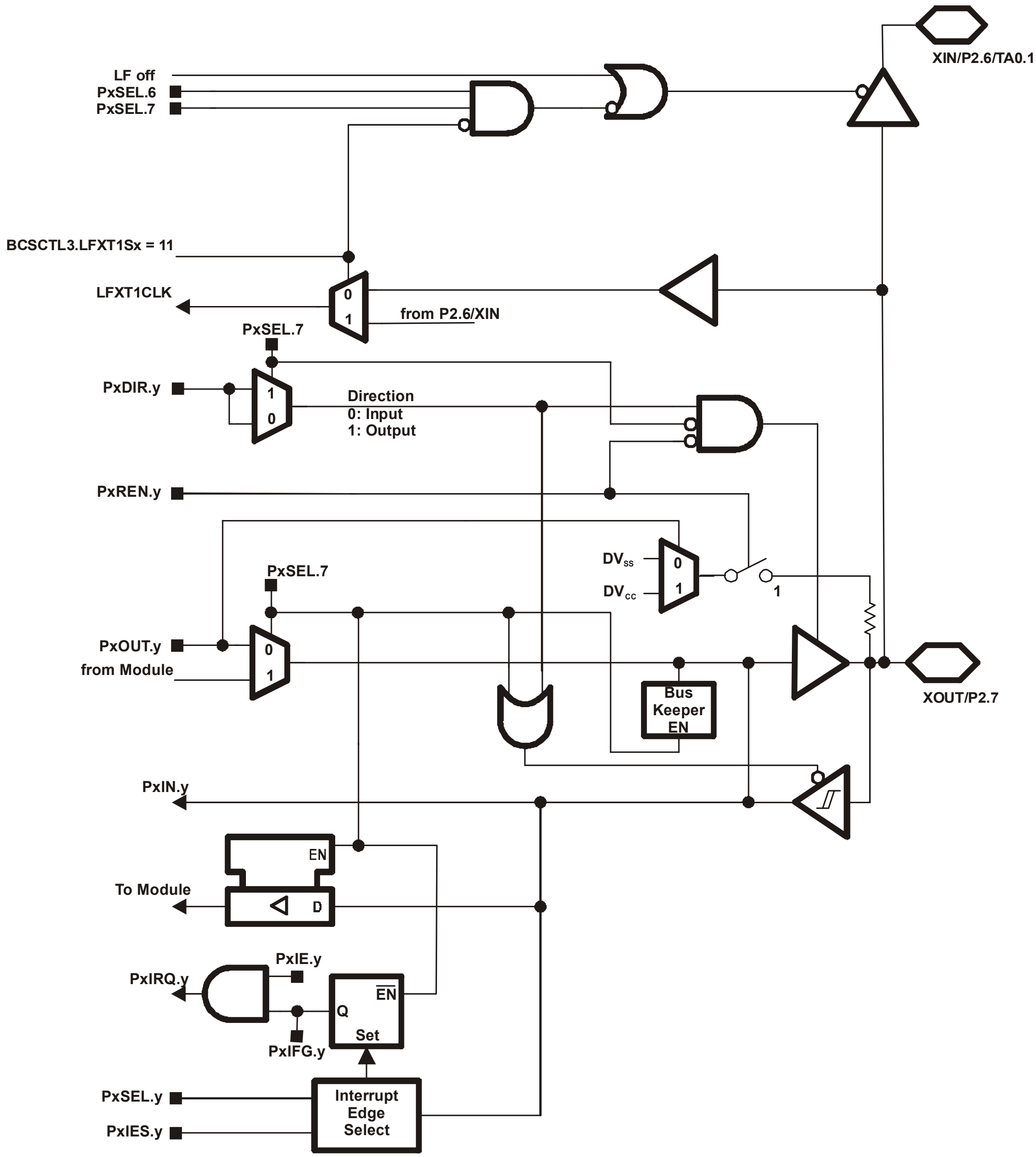
Port P2 pin schematic: P2.6, input/output with Schmitt trigger − MSP430G2x21 and MSP430G2x31



Port P2 (P2.6) pin functions − MSP430G2x21 and MSP430G2x31

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.6	PSEL2.7
XIN	6	XIN	0	1	1
P2.6		P2.x (I/O)	I: 0; O: 1	0	x
TA0.1		Timer0_A3.TA1	1	1	x

Port P2 pin schematic: P2.7, input/output with Schmitt trigger - MSP430G2x21 and MSP430G2x31



PRODUCT PREVIEW

Port P2 (P2.7) pin functions − MSP430G2x21 and MSP430G2x31

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.6 P2SEL.7	P2SEL.7
XOUT	7	XOUT	1	1	1
P2.7		P2.x (I/O)	I: 0; O: 1	0	x

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Pea
MSP430G2121IN14	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-1-260
MSP430G2121IPW14	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
MSP430G2121IPW14R	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
MSP430G2121IRSA16R	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
MSP430G2121IRSA16T	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
MSP430G2131IN14	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-1-260
MSP430G2131IPW14	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
MSP430G2131IPW14R	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
MSP430G2131IRSA16R	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
MSP430G2131IRSA16T	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
MSP430G2221IN14	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-1-260
MSP430G2221IPW14	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
MSP430G2221IPW14R	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
MSP430G2221IRSA16R	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
MSP430G2221IRSA16T	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
MSP430G2231IN14	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-1-260
MSP430G2231IPW14	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
MSP430G2231IPW14R	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
MSP430G2231IRSA16R	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260
MSP430G2231IRSA16T	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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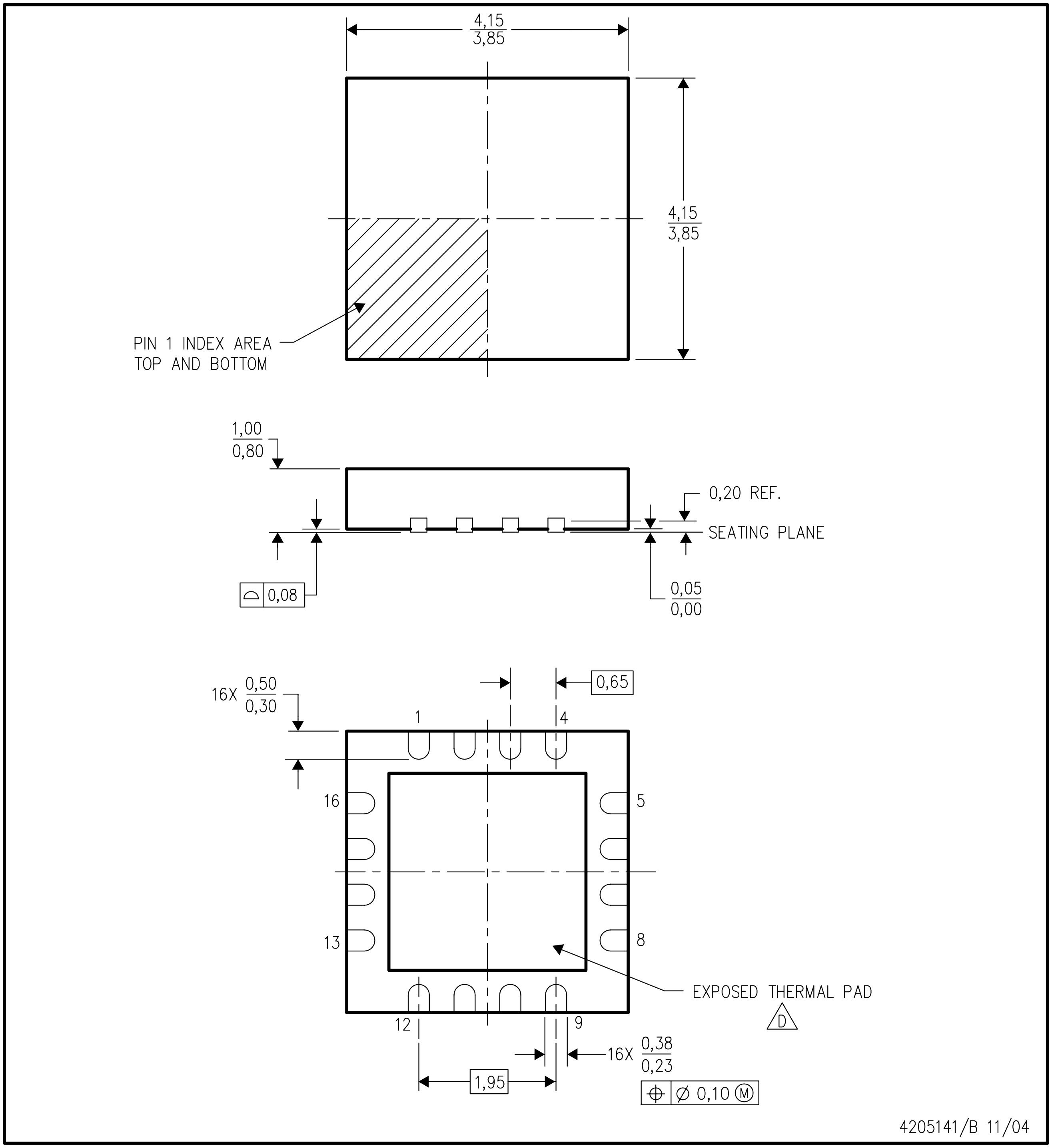
RSA (S–PQFP–N16) PLASTIC QUAD FLATPACK



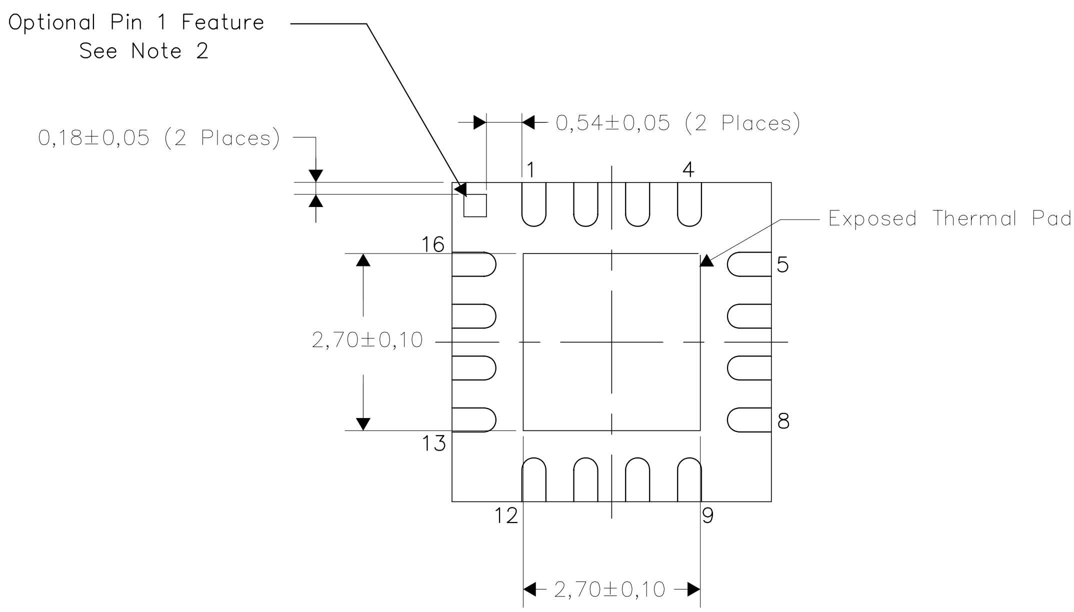
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



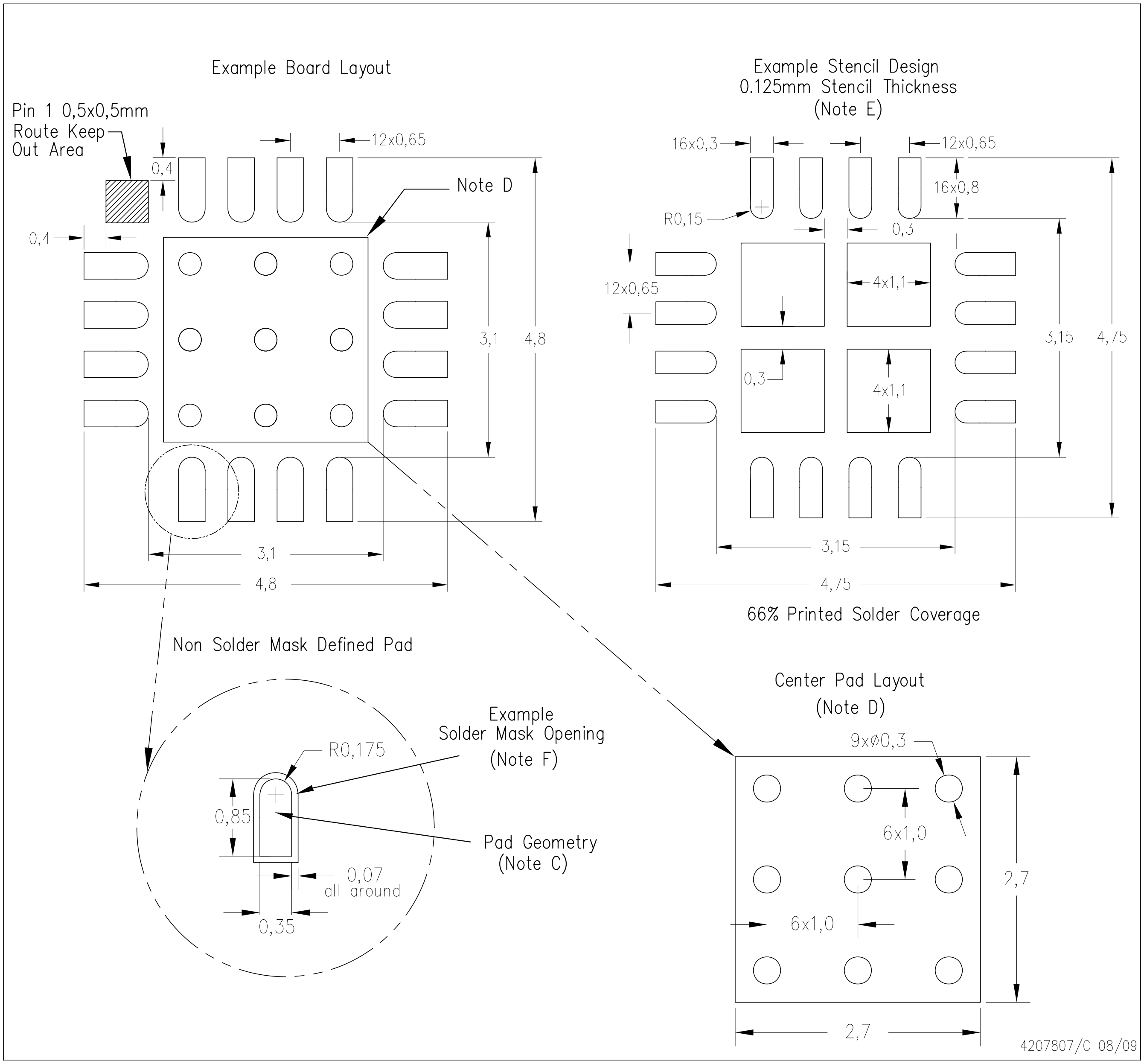
Bottom View

Exposed Thermal Pad Dimensions

NOTES:

1) All linear dimensions are in millimeters
2) The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

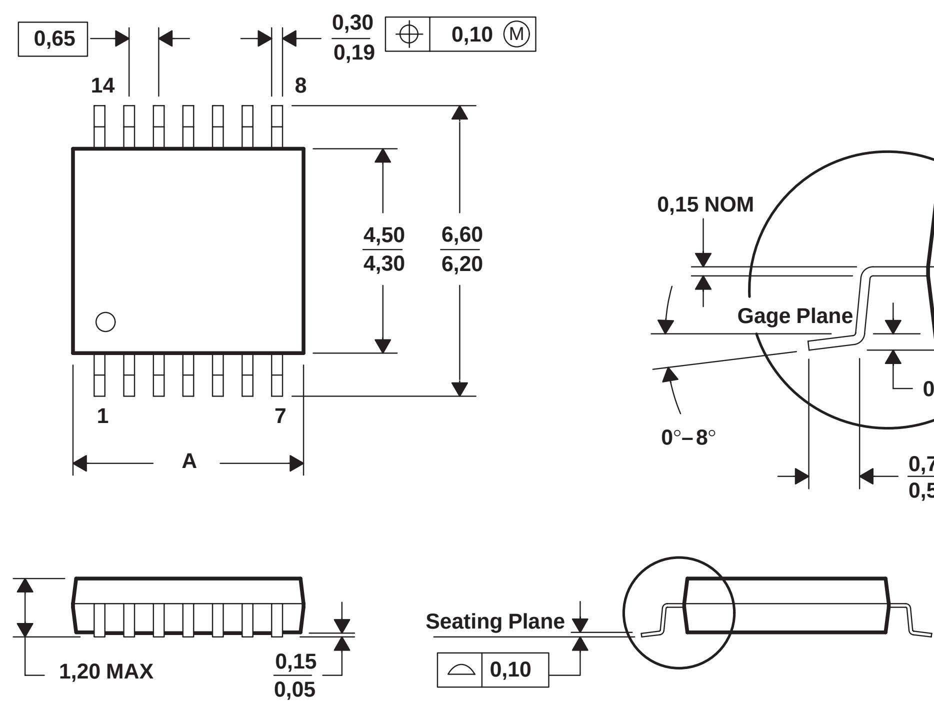
RSA (S–PVQFN–N16)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE