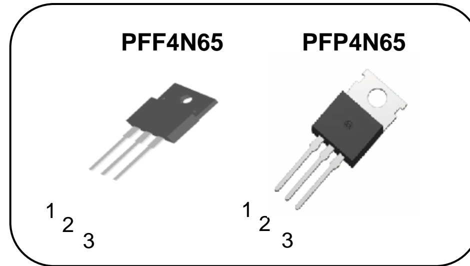
PFP4N65/PFF4N65

N-channel MOSFET

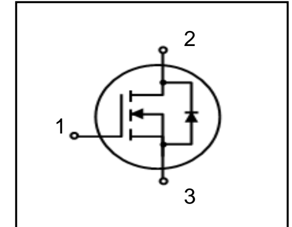
Features

- High ruggedness
- $R_{DS(ON)}$ (Max 2.5 Ω)@V_{GS}=10V
- Gate Charge (Typ. 28.6nC)
- Improved dv/dt Capability
- 100% Avalanche Tested



1. Gate 2. Drain 3. Source

BV_{DSS} : 650V
I_D : 4.0A
$R_{DS(ON)}$: 2.5ohm



General Description

These N-channel enhancement mode field effect power transistor is using PowerGate semiconductor's advanced planar stripe, DMOS technology intended for off line switch mode power supply. Also, especially designed to minimize $R_{DS(ON)}$ and high rugged avalanche characteristics. These devices are well suited for high efficiency switching Mode power supplies and active power factor correction.

Absolute maximum ratings

Symbol	Parameter	Value		Unit
		PFP4N65	PFF4N65	
V_{DSS}	Drain to Source Voltage	650		V
I_D	Continuous Drain Current (@T_C=25°C)	4.0	4.0*	A
	Continuous Drain Current (@T_C=100°C)	2.5	2.5*	A
I_{DM}	Drain current pulsed (note 1)	16		A
V_{GS}	Gate to Source Voltage	±30		V
E_{AS}	Single pulsed Avalanche Energy (note 2)	157		mJ
E_{AR}	Repetitive Avalanche Energy (note 1)	3.0		mJ
dv/dt	Peak diode Recovery dv/dt (note 3)	4.5		V/ns
P_D	Total power dissipation (@T_C=25°C)	98	33*	W
	Derating Factor above 25°C	0.78	0.31	W/°C
T_{STG}, T_J	Operating Junction Temperature & Storage Temperature	-55 ~ + 150		°C
T_L	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.	300		°C

*. Drain current limited by maximum Junction temperature.

Thermal characteristics

Symbol	Parameter	Value		Unit
		PFP4N65	PFF4N65	
R_{thJC}	Thermal resistance, Junction to case	1.28	3.8	°C/W
R_{thCS}	Thermal resistance, Case to Sink	0.5		°C/W
R_{thJA}	Thermal resistance, Junction to ambient	62.5		°C/W

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Electrical characteristic (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	650	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown voltage temperature coefficient	I_D=250uA, referenced to 25°C	-	0.53	-	V/°C
I_{DSS}	Drain to source leakage current	V_{DS}=650V, V_{GS}=0V	-	-	50	uA
		V_{DS}=520V, T_C=125°C	-	-	100	uA
I_{GSS}	Gate to source leakage current, forward	V_{GS}=30V, V_{DS}=0V	-	-	100	nA
	Gate to source leakage current, reverse	V_{GS}=-30V, V_{DS}=0V	-	-	-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250uA	3.0	-	5.0	V
$R_{DS(ON)}$	Drain to source on state resistance	V_{GS}=10V, I_D = 2.0A		2.2	2.5	Ω
Dynamic characteristics						
C_{iss}	Input capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz		570	740	pF
C_{oss}	Output capacitance			70	90	
C_{rss}	Reverse transfer capacitance			18	24	
$t_{d(on)}$	Turn on delay time	V_{DS}=325V, I_D=4.0A, R_G=25Ω		21	52	ns
tr	Rising time			46	102	
$t_{d(off)}$	Turn off delay time			100	214	
t_f	Fall time			34	78	
Q_g	Total gate charge	V_{DS}=520V, V_{GS}=10V, I_D=4.0A		28.6	35	nC
Q_{gs}	Gate-source charge			3.0	-	
Q_{gd}	Gate-drain charge			8.0	-	

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET	-	-	4	A
I_{SM}	Pulsed source current		-	-	16	A
V_{SD}	Diode forward voltage drop.	I_S=4.0A, V_{GS}=0V	-	-	1.5	V
T_{rr}	Reverse recovery time	I_S=4.0A, V_{GS}=0V, dI_F/dt=100A/us	-	392	-	ns
Q_{rr}	Breakdown voltage temperature		-	1.57	-	uC

※. Notes

1. Repetitive rating : pulse width limited by junction temperature.
2. L = 19mH, I_{AS} = 4.0A, V_{DD} = 50V, R_G=50Ω, Starting T_J = 25°C
3. I_{SD} ≤ 4.0A, di/dt = 300A/us, V_{DD} ≤ BV_{DSS}, Staring T_J =25°C
4. Pulse Test : Pulse Width ≤ 300us, duty cycle ≤ 2%
5. Essentially independent of operating temperature.

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Fig. 1. On-state characteristics

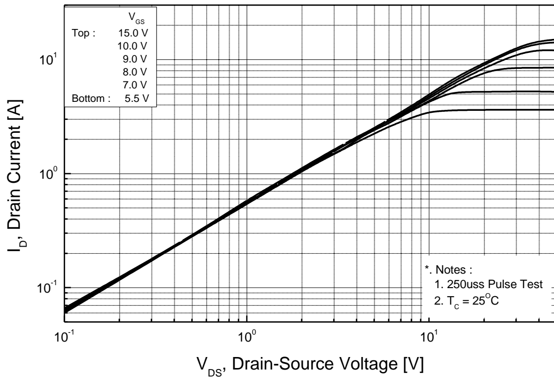

Fig. 2. Transfer characteristics

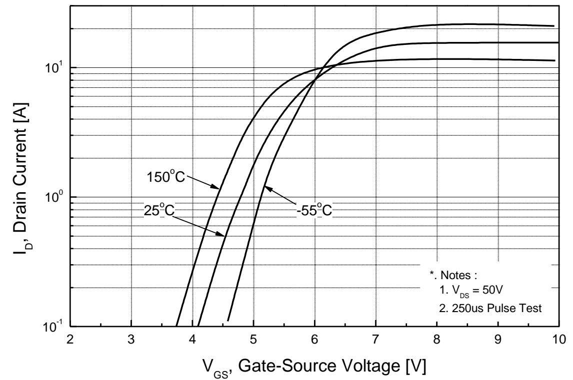

Fig. 3. On-resistance variation vs. drain current and gate voltage

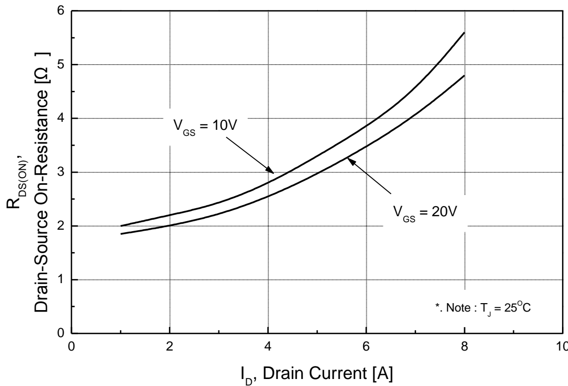

Fig. 4. On state current vs. diode forward voltage

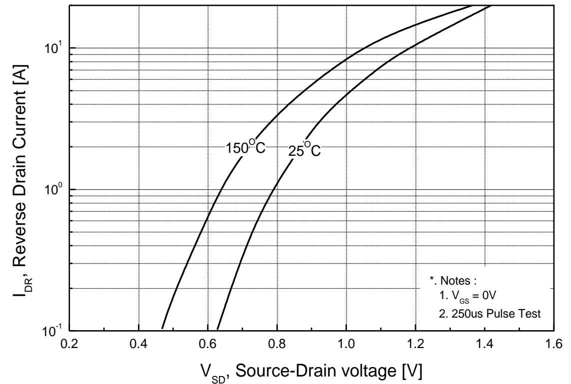

Fig. 5. Capacitance characteristics (Non-Repetitive)

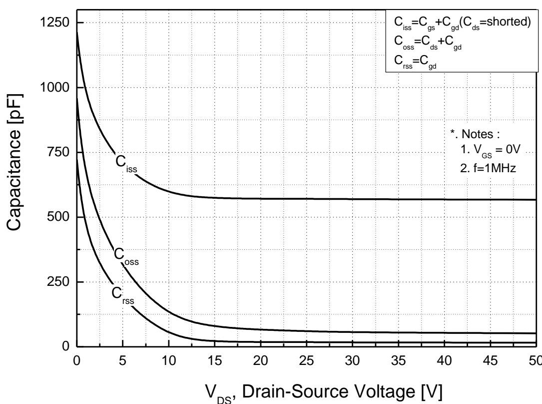

Fig. 6. Gate charge characteristics

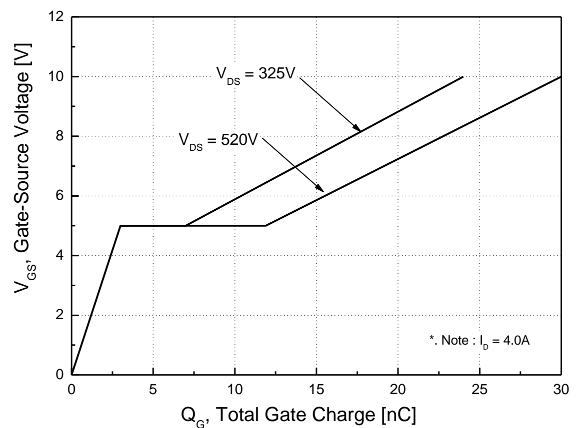

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Fig 7. Breakdown Voltage Variation vs. Junction Temperature

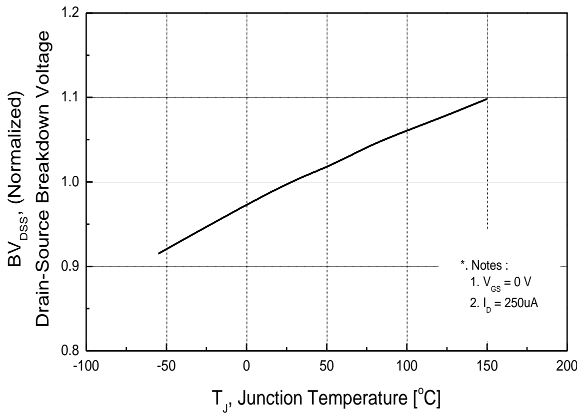

Fig. 8. On resistance variation vs. junction temperature

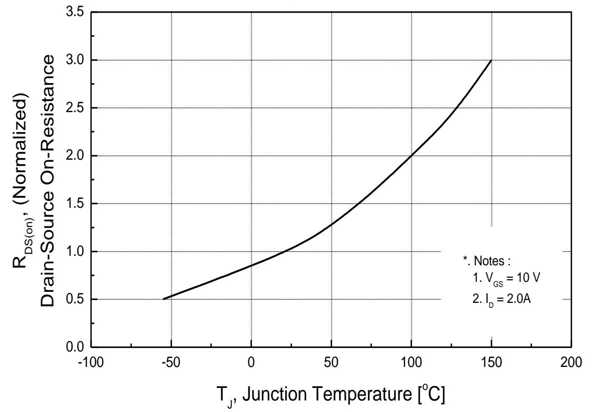

Fig. 9. Maximum drain current vs. case temperature.

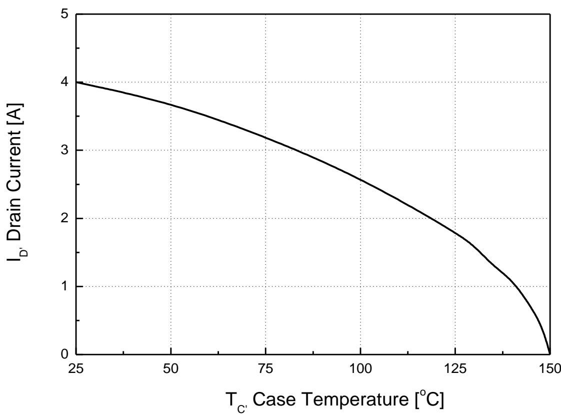

Fig. 10. Maximum safe operating area

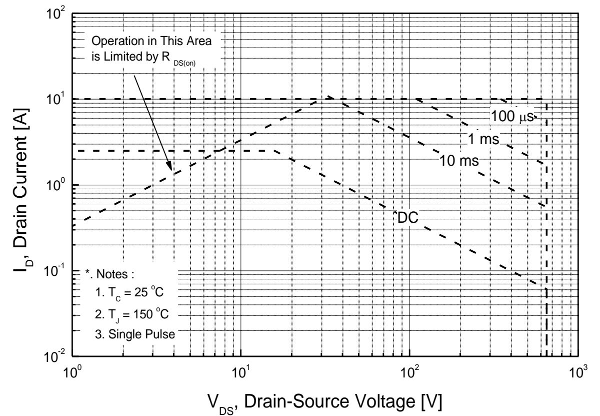

Fig. 11. Transient thermal response curve

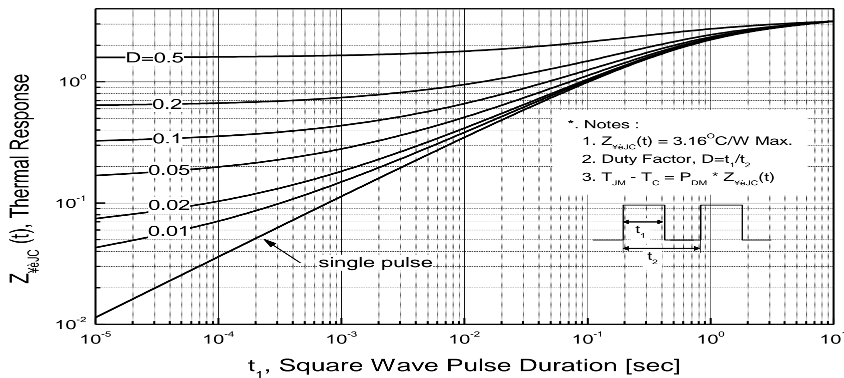

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Fig. 12. Gate charge test circuit & waveform

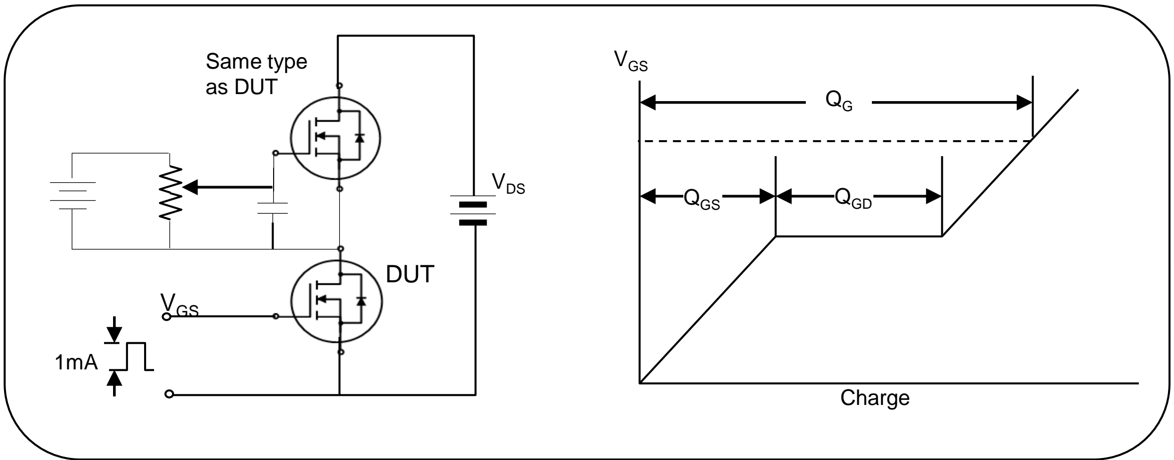

Fig. 13. Switching time test circuit & waveform

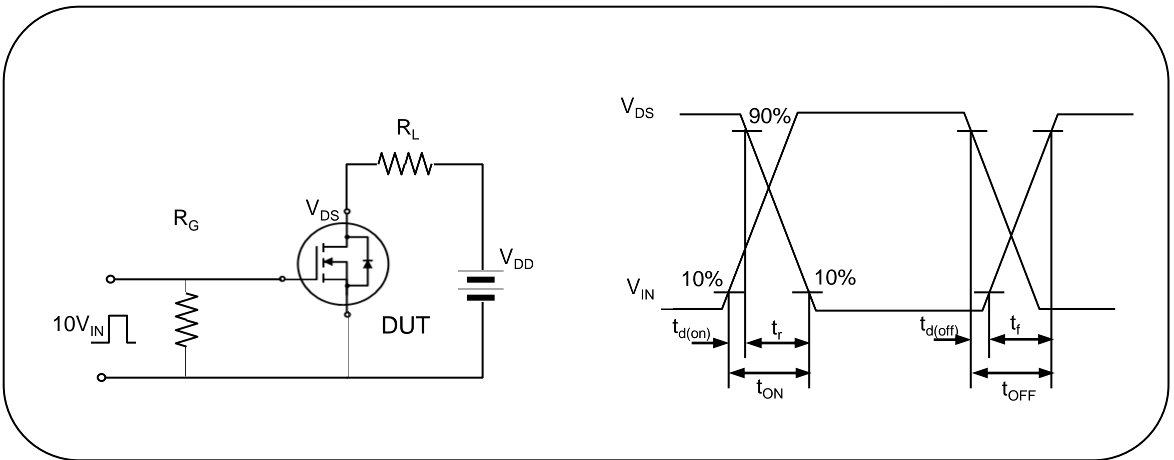

Fig. 14. Unclamped Inductive switching test circuit & waveform

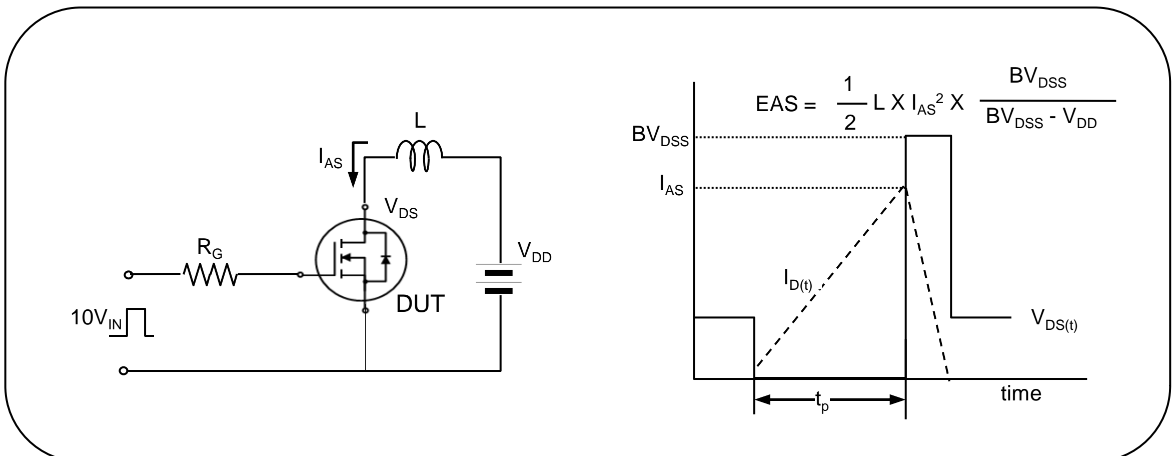

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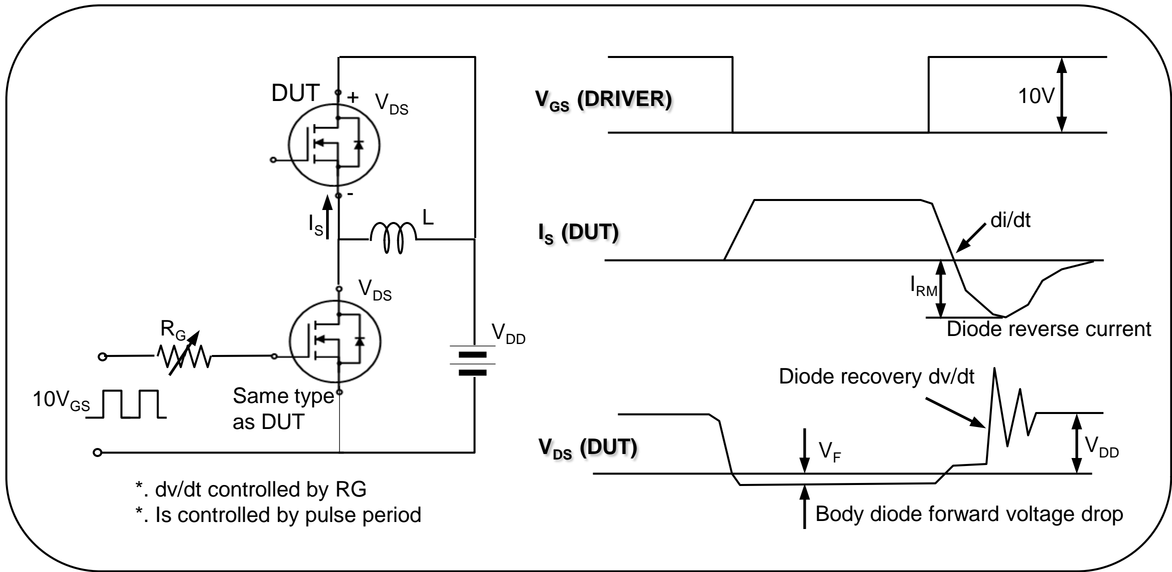
Fig. 15. Peak diode recovery dv/dt test circuit & waveform



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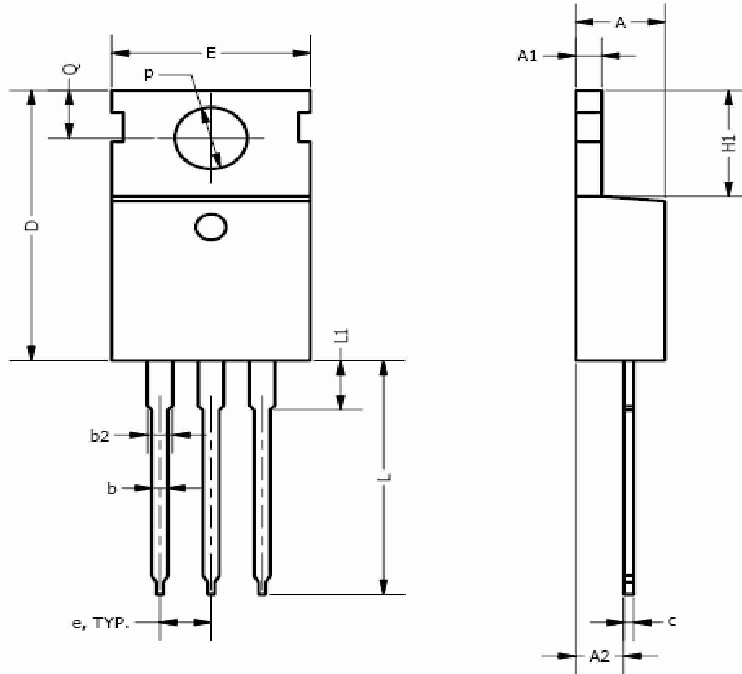
TO-220 Package Dimension



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.14	0.19	3.56	4.83
A1	0.02	0.055	0.51	1.4
A2	0.08	0.115	2.03	2.92
b	0.015	0.04	0.38	1.02
b2	0.045	0.07	1.14	1.78
c	0.014	0.024	0.36	0.61
D	0.56	0.65	14.22	16.51
e	0.096	0.104	2.44	2.64
E	0.38	0.42	9.65	10.67
H1	0.23	0.27	5.84	6.86
L	0.5	0.58	12.7	14.73
L1	-	0.25	-	6.35
¢P	0.139	0.161	3.53	4.09
Q	0.1	0.135	2.54	3.43

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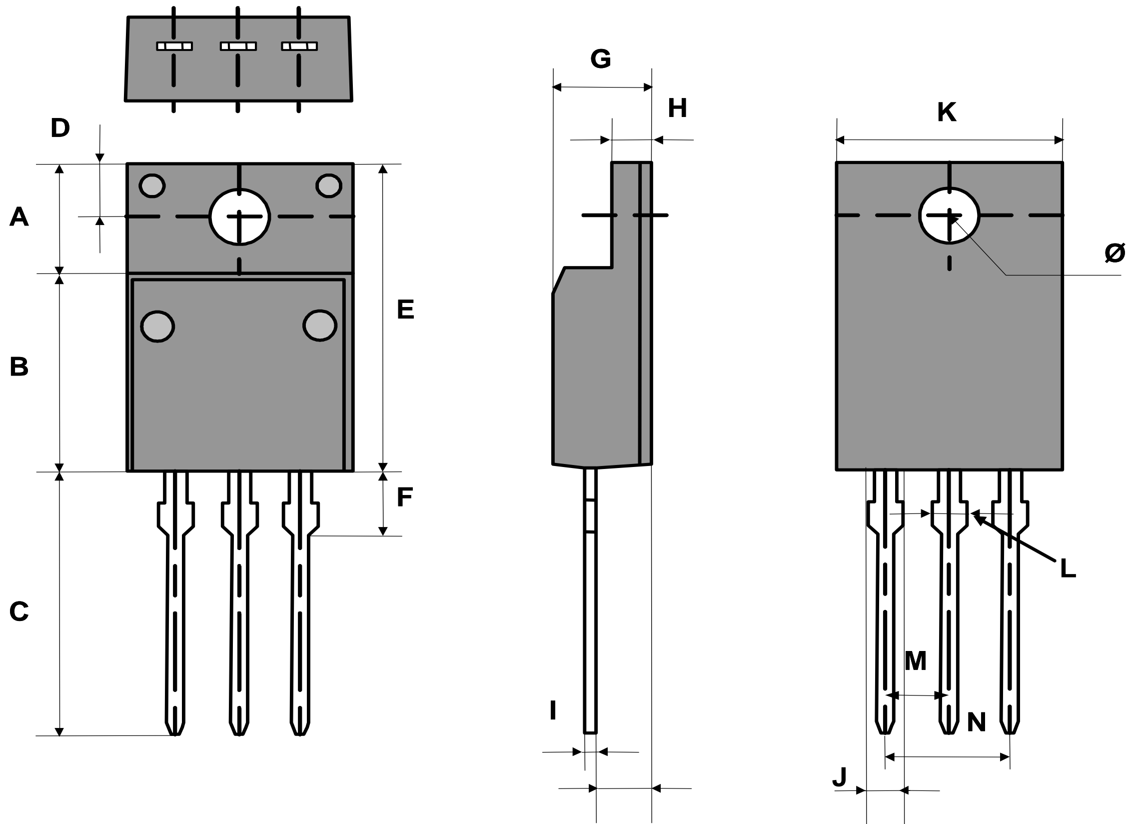
TO-220F Package Dimension



DIMENSION		A	B	C	D	E	F	G	H
mm	Min	6.00	7.85	12.88	3.00	15.0	3.15	4.45	3.05
	Typ.	6.05	7.90	13.08	3.02	15.2	3.25	4.50	3.10
	Max	6.10	7.95	13.28	3.04	15.4	3.35	4.55	3.15

DIMENSION		I	J	K	L	M	N	Ø	
mm	Min	0.585	1.245	9.95	1.65	2.00	4.58	2.90	
	Typ.	0.595	1.250	10.00	1.66	2.05	4.60	2.95	
	Max	0.605	1.255	10.05	1.67	2.10	4.62	3.00	

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