



MICROCHIP

PIC12CE67X

8-Pin, 8-Bit CMOS Microcontroller with A/D Converter and EEPROM Data Memory

Devices Included in this Data Sheet:

- PIC12CE673
- PIC12CE674

High-Performance RISC CPU:

- Only 35 single word instructions to learn
- All instructions are single cycle (400 ns) except for program branches which are two-cycle
- Operating speed: DC - 10 MHz clock input
DC - 400 ns instruction cycle

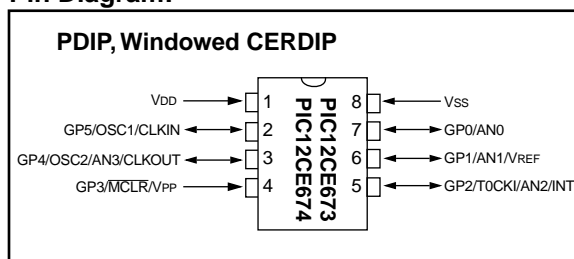
Device	Memory		
	Program	Data RAM	Data EEPROM
PIC12CE673	1024 x 14	128 x 8	16 x 8
PIC12CE674	2048 x 14	128 x 8	16 x 8

- 14-bit wide instructions
- 8-bit wide data path
- Interrupt capability
- Special function hardware registers
- 8-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features:

- Four-channel, 8-bit A/D converter
- 8-bit real time clock/counter (TMR0) with 8-bit programmable prescaler
- Interrupt on pin change (GP0, GP1, GP3)
- 1,000,000 erase/write cycle EEPROM data memory
- EEPROM data retention > 40 years

Pin Diagram:



Special Microcontroller Features:

- In-Circuit Serial Programming (ICSP™)
- Internal 4 MHz oscillator with programmable calibration
- Selectable clockout
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Internal pull-ups on I/O pins (GP0, GP1, GP3)
- Internal pull-up on $\overline{\text{MCLR}}$ pin
- Selectable oscillator options:
 - INTRC: Precision internal 4 MHz oscillator
 - EXTRC: External low-cost RC oscillator
 - XT: Standard crystal/resonator
 - HS: High speed crystal/resonator
 - LP: Power saving, low frequency crystal

CMOS Technology:

- Low-power, high-speed CMOS EPROM/EEPROM technology
- Fully static design
- Wide operating voltage range 2.5V to 5.5V
- Commercial, Industrial, and Extended temperature ranges
- Low power consumption
 - < 2 mA @ 5V, 4 MHz
 - 15 μ A typical @ 3V, 32 kHz
 - < 1 μ A typical standby current

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Errata

An errata sheet may exist for current devices, describing minor operational differences (from the data sheet) and recommended workarounds. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; <http://www.microchip.com>
- Your local Microchip sales office (see last page)
- The Microchip Corporate Literature Center; U.S. FAX: (602) 786-7277

When contacting a sales office or the literature center, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Corrections to this Data Sheet

We constantly strive to improve the quality of all our products and documentation. We have spent a great deal of time to ensure that this document is correct. However, we realize that we may have missed a few things. If you find any information that is missing or appears in error, please:

- Fill out and mail in the reader response form in the back of this data sheet.
- E-mail us at webmaster@microchip.com.

We appreciate your assistance in making this a better document.

1.0 GENERAL DESCRIPTION

The PIC12CE67X devices are low-cost, high-performance, CMOS, fully-static, 8-bit microcontroller with integrated analog-to-digital (A/D) converter and EEPROM data memory in the PIC12CEXXX Microcontroller family.

All PICmicro™ microcontrollers employ an advanced RISC architecture. The PIC12C67X microcontrollers have enhanced core features, eight-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 14-bit wide instruction word with the separate 8-bit wide data. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches which require two cycles. A total of 35 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance.

PIC12C67X microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

The PIC12CE67X devices have 128 bytes of RAM, 16 bytes of EEPROM data memory, 5 I/O pins and 1 input pin. In addition a timer/counter is available. Also a 4-channel high-speed 8-bit A/D is provided. The 8-bit resolution is ideally suited for applications requiring low-cost analog interface, e.g. thermostat control, pressure sensing, etc.

The PIC12CE67X device has special features to reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption. The Power-On Reset (POR), Power-up Timer (PWRT), and Oscillator Start-up Timer (OST) eliminate the need for external reset circuitry. There are five oscillator configurations to choose from, including INTRC precision internal oscillator mode and the power-saving LP (Low Power) oscillator mode. Power saving SLEEP mode, Watchdog Timer and code protection features improve system cost, power and reliability. The SLEEP (power-down) feature provides a power saving mode. The user can wake up the chip from SLEEP through several external and internal interrupts and resets.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software lock-up.

A UV erasable windowed package version is ideal for code development while the cost-effective One-Time-Programmable (OTP) version is suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers while benefiting from the OTP's flexibility.

The PIC12CE67X device fits perfectly in applications ranging from security and remote sensors to appliance control and automotive. The EPROM technology makes customization of application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages make this microcontroller series perfect for all applications with space limitations. Low cost, low power, high performance, ease of use and I/O flexibility make the PIC12CE67X very versatile even in areas where no microcontroller use has been considered before (e.g. timer functions, communications and coprocessor applications).

1.1 Family and Upward Compatibility

The PIC12CE67X products are compatible with other members of the 14-Bit, PIC12C67X and PIC16CXXX families.

1.2 Development Support

The PIC12CE67X device is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a full-featured programmer. A "C" compiler and fuzzy logic support tools are also available.

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TABLE 1-1: PIC12CXXX & PIC12CEXXX FAMILY OF DEVICES

		PIC12C508(A)	PIC12C509(A)	PIC12CE518	PIC12CE519	PIC12C671	PIC12C672	PIC12CE673	PIC12CE674
Clock	Maximum Frequency of Operation (MHz)	4	4	4	4	10	10	10	10
	Memory								
	EPROM Program Memory	512 x 12	1024 x 12	512 x 12	1024 x 12	1024 x 14	2048 x 14	1024 x 14	2048 x 14
	RAM Data Memory (bytes)	25	41	25	41	128	128	128	128
Peripherals	EEPROM Data Memory (bytes)	—	—	16	16	—	—	16	16
	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0	TMR0
	A/D Converter (8-bit) Channels	—	—	—	—	4	4	4	4
Features	Wake-up from SLEEP on pin change	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Interrupt Sources	—	—	—	—	4	4	4	4
	I/O Pins	5	5	5	5	5	5	5	5
	Input Pins	1	1	1	1	1	1	1	1
	Internal Pull-ups	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	In-Circuit Serial Programming	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Number of Instructions	33	33	33	33	35	35	35	35
Packages	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW, SOIC	8-pin DIP, JW	8-pin DIP, JW

All PIC12CXXX & PIC12CEXXX devices have Power-on Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

All PIC12CXXX & PIC12CEXXX devices use serial programming with data pin GP0 and clock pin GP1.

2.0 PIC12CE67X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in the PIC12CE67X Product Identification System section at the end of this data sheet. When placing orders, please use that page of the data sheet to specify the correct part number.

For example, the PIC12CE67X device "type" is indicated in the device number:

1. **CE**, as in PIC12**CE**674. These devices have OTP program memory, EEPROM data memory and operate over the standard voltage range.

2.1 UV Erasable Devices

The UV erasable version, offered in windowed package, is optimal for prototype development and pilot programs.

The UV erasable version can be erased and reprogrammed to any of the configuration modes. Microchip's PICSTART[®] Plus and PRO MATE[®] programmers both support the PIC12CE67X. Third party programmers also are available; refer to the Microchip Third Party Guide for a list of sources.

Note: Please note that erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be saved prior to erasing the part.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers who need the flexibility for frequent code updates and small volume applications.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must also be programmed.

2.3 Quick-Turn-Programming (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

2.4 Serialized Quick-Turn Programming (SQTPSM) Devices

Microchip offers a unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random, or sequential.

Serial programming allows each device to have a unique number which can serve as an entry-code, password, or ID number.

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NOTES:

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC12CE67X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC12CE67X uses a Harvard architecture, in which program and data are accessed from separate memories using separate buses. This improves bandwidth over traditional von Neumann architecture in which program and data are fetched from the same memory using the same bus. Separating program and data buses also allow instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 14-bits wide making it possible to have all single word instructions. A 14-bit wide program memory access bus fetches a 14-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions (Example 3-1). Consequently, all instructions (35) execute in a single cycle (400 ns @ 10 MHz) except for program branches.

The table below lists program memory (EPROM), data memory (RAM), and non-volatile memory (EEPROM) for each PIC12CE67X device.

Device	Program Memory	RAM Data Memory	EEPROM Data Memory
PIC12CE673	1K x 14	128 x 8	16x8
PIC12CE674	2K x 14	128 x 8	16x8

The PIC12CE67X can directly or indirectly address its register files or data memory. All special function registers, including the program counter, are mapped in the data memory. The PIC12CE67X has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC12CE67X simple yet efficient. In addition, the learning curve is reduced significantly.

PIC12CE67X devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between the data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the working register (W register). The other operand is a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow bit and a digit borrow out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

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FIGURE 3-1: PIC12CE67X BLOCK DIAGRAM

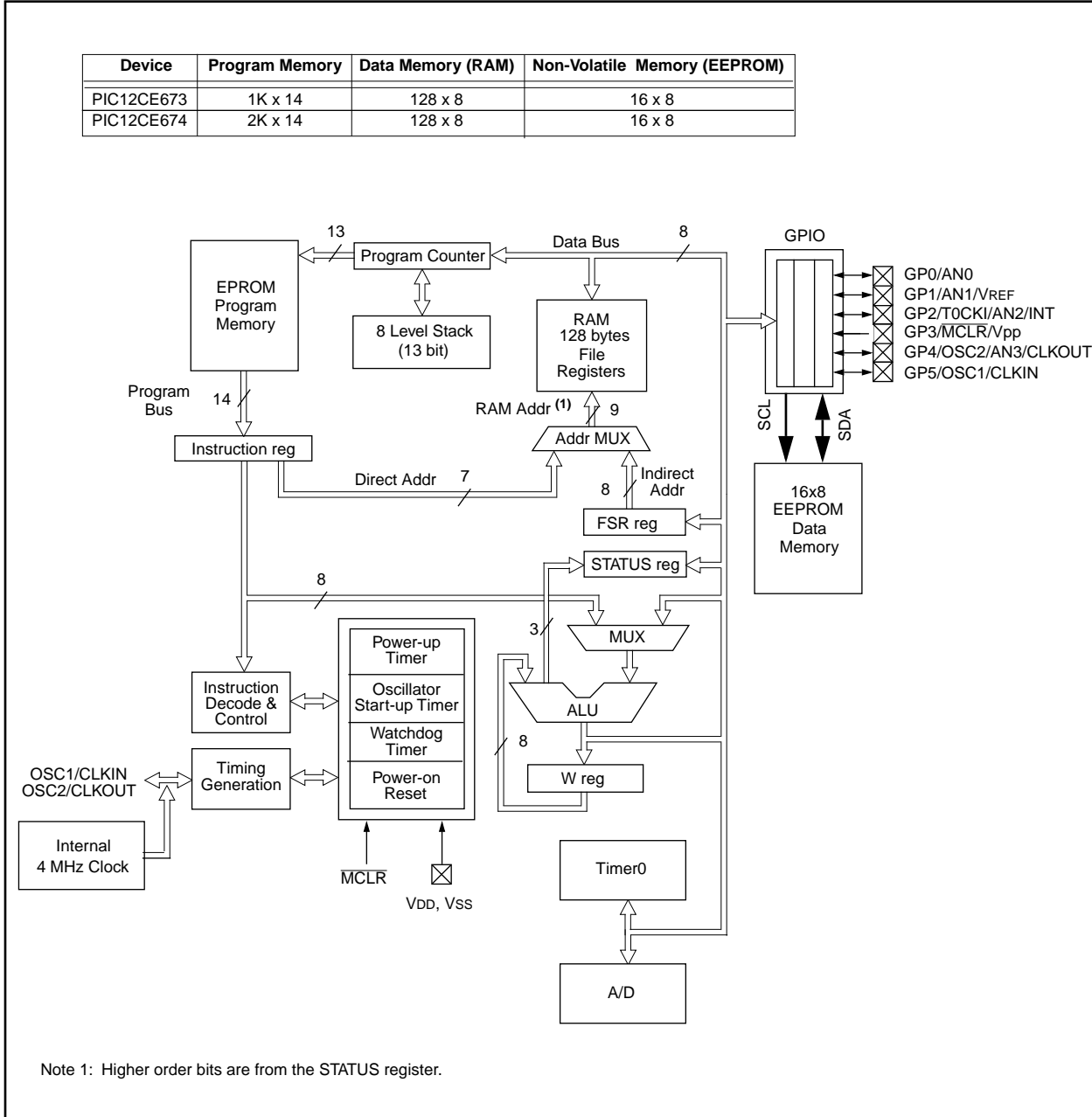


TABLE 3-1: PIC12CE67X PINOUT DESCRIPTION

Name	DIP Pin #	I/O/P Type	Buffer Type	Description
GP0/AN0	7	I/O	TTL/ST	Bi-directional I/O port/serial programming data/analog input 0. Can be software programmed for internal weak pull-up and interrupt on pin change. This buffer is a Schmitt Trigger input when used in serial programming mode.
GP1/AN1/V _{REF}	6	I/O	TTL/ST	Bi-directional I/O port/serial programming clock/analog input 1/voltage reference. Can be software programmed for internal weak pull-up and interrupt on pin change. This buffer is a Schmitt Trigger input when used in serial programming mode.
GP2/T0CKI/AN2/INT	5	I/O	ST	Bi-directional I/O port/analog input 2. Can be configured as T0CKI or external interrupt.
GP3/MCLR/VPP	4	I	TTL/ST	Input port/master clear (reset) input/programming voltage input. When configured as MCLR, this pin is an active low reset to the device. Voltage on MCLR/VPP must not exceed VDD during normal device operation. Can be software programmed for internal weak pull-up and interrupt on pin change. Weak pull-up always on if configured as MCLR. This buffer is Schmitt Trigger when in MCLR mode.
GP4/OSC2/AN3/CLKOUT	3	I/O	TTL	Bi-directional I/O port/oscillator crystal output/analog input 3. Connections to crystal or resonator in crystal oscillator mode (HS, XT and LP modes only, GPIO in other modes). In EXTRC and INTRC modes, the pin output can be configured to CLKOUT which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
GP5/OSC1/CLKIN	2	I/O	TTL/ST	Bidirectional IO port/oscillator crystal input/external clock source input (GPIO in INTRC mode only, OSC1 in all other oscillator modes). Schmitt trigger in EXTRC mode only.
VDD	1	P	—	Positive supply for logic and I/O pins
VSS	8	P	—	Ground reference for logic and I/O pins

Legend: I = input, O = output, I/O = input/output, P = power, — = not used, TTL = TTL input, ST = Schmitt Trigger input

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3.1 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2.

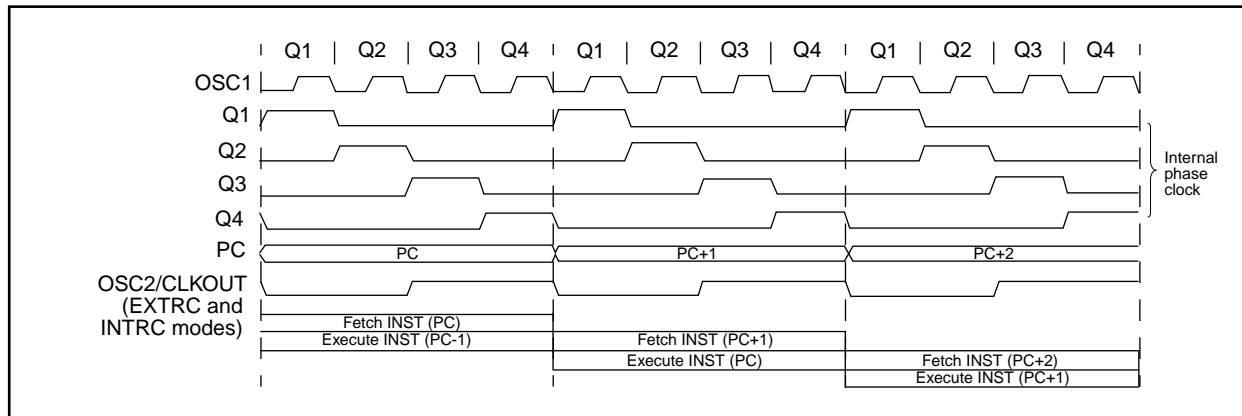
3.2 Instruction Flow/Pipelining

An "Instruction Cycle" consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g. GOTO) then two cycles are required to complete the instruction (Example 3-1).

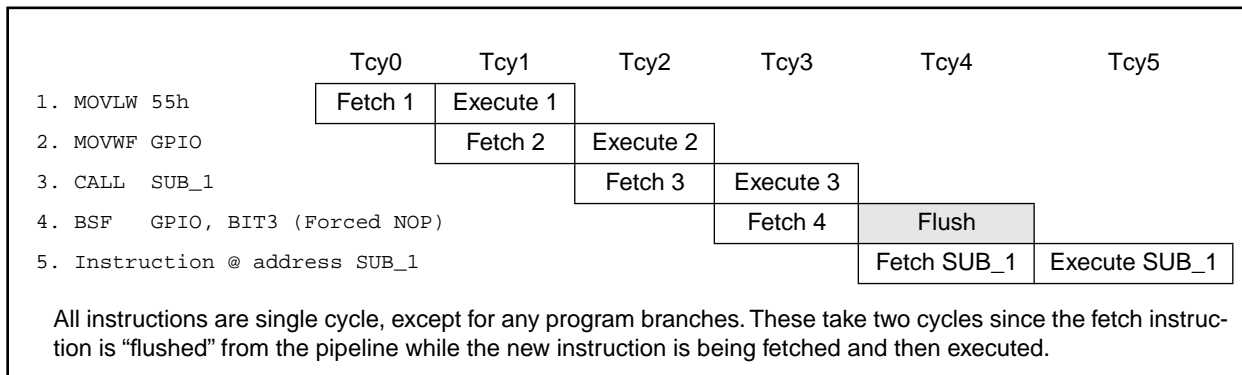
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the "Instruction Register" (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



4.0 MEMORY ORGANIZATION

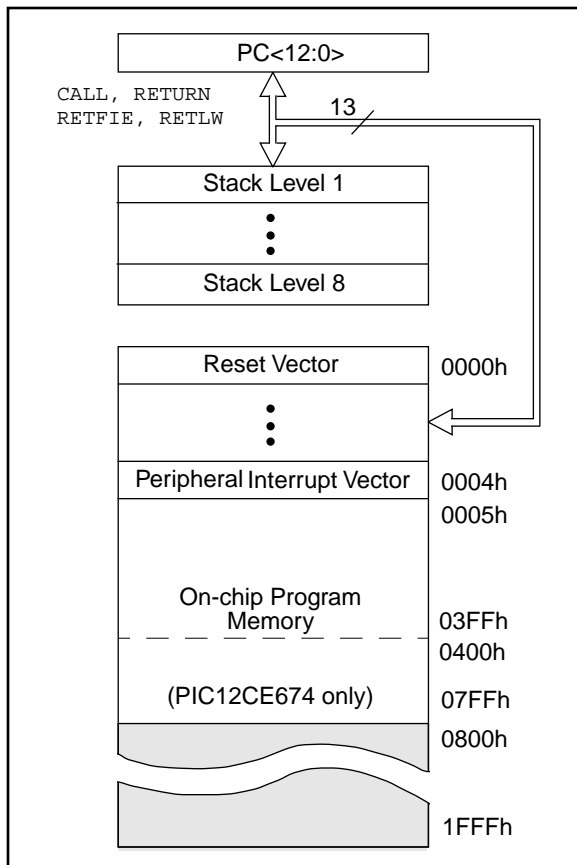
4.1 Program Memory Organization

The PIC12CE67X has a 13-bit program counter capable of addressing an 8K x 14 program memory space.

For the PIC12CE673 the first 1K x 14 (0000h-03FFh) is implemented.

For the PIC12CE674, the first 2K x 14 (0000h-07FFh) is implemented. Accessing a location above the physically implemented address will cause a wraparound. The reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 4-1: PIC12CE67X PROGRAM MEMORY MAP AND STACK



4.2 Data Memory Organization

The data memory is partitioned into two Banks which contain the General Purpose Registers and the Special Function Registers. Bit RP0 is the bank select bit.

RP0 (STATUS<5>) = 1 → Bank 1

RP0 (STATUS<5>) = 0 → Bank 0

Each Bank extends up to 7Fh (128 bytes). The lower locations of each Bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers implemented as static RAM. Both Bank 0 and Bank 1 contain special function registers. Some "high use" special function registers from Bank 0 are mirrored in Bank 1 for code reduction and quicker access.

Also note that F0h through FFh on the PIC12CE67X is mapped into Bank 0 registers 70h-7Fh as common RAM.


4.2.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly, or indirectly through the File Select Register FSR (Section 4.5).

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FIGURE 4-2: PIC12CE67X REGISTER FILE MAP

File Address			File Address
00h	INDF ⁽¹⁾	INDF ⁽¹⁾	80h
01h	TMR0	OPTION	81h
02h	PCL	PCL	82h
03h	STATUS	STATUS	83h
04h	FSR	FSR	84h
05h	GPIO	TRIS	85h
06h			86h
07h			87h
08h			88h
09h			89h
0Ah	PCLATH	PCLATH	8Ah
0Bh	INTCON	INTCON	8Bh
0Ch	PIR1	PIE1	8Ch
0Dh			8Dh
0Eh		PCON	8Eh
0Fh		OSCCAL	8Fh
10h			90h
11h			91h
12h			92h
13h			93h
14h			94h
15h			95h
16h			96h
17h			97h
18h			98h
19h			99h
1Ah			9Ah
1Bh			9Bh
1Ch			9Ch
1Dh			9Dh
1Eh	ADRES		9Eh
1Fh	ADCON0	ADCON1	9Fh
20h	General Purpose Register	General Purpose Register	A0h
			BFh
			C0h
			EFh
70h			F0h
7Fh			Mapped in Bank 0
	Bank 0	Bank 1	

 Unimplemented data memory locations, read as '0'.
 Note 1: Not a physical register.

4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and Peripheral Modules for controlling the desired operation of the device. These registers are implemented as static RAM.

The special function registers can be classified into two sets (core and peripheral). Those registers associated with the “core” functions are described in this section, and those related to the operation of the peripheral features are described in the section of that peripheral feature.

TABLE 4-1: PIC12CE67X SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other Resets ⁽³⁾
Bank 0											
00h ⁽¹⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
03h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	\overline{TO}	\overline{PD}	Z	DC	C	0001 1xxx	000q quuu
04h ⁽¹⁾	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
05h	GPIO	SCL	SDA	GP5	GP4	GP3	GP2	GP1	GP0	11xx xxxx	11uu uuuu
06h	—	Unimplemented								—	—
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah ^(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	---0 0000
0Bh ⁽¹⁾	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	—	—	—	—	-0-- ----	-0-- ----
0Dh	—	Unimplemented								—	—
0Eh	—	Unimplemented								—	—
0Fh	—	Unimplemented								—	—
10h	—	Unimplemented								—	—
11h	—	Unimplemented								—	—
12h	—	Unimplemented								—	—
13h	—	Unimplemented								—	—
14h	—	Unimplemented								—	—
15h	—	Unimplemented								—	—
16h	—	Unimplemented								—	—
17h	—	Unimplemented								—	—
18h	—	Unimplemented								—	—
19h	—	Unimplemented								—	—
1Ah	—	Unimplemented								—	—
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	r	CHS1	CHS0	GO/DONE	r	ADON	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0', r = reserved.
 Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

3: Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.

4: The IRP and RP1 bits are reserved on the PIC12CE67X, always maintain these bits clear.

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TABLE 4-1: PIC12CE67X SPECIAL FUNCTION REGISTER SUMMARY (CONT.)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other Resets ⁽³⁾
Bank 1											
80h ⁽¹⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	0000 0000
81h	OPTION	GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
82h ⁽¹⁾	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	0000 0000
83h ⁽¹⁾	STATUS	IRP ⁽⁴⁾	RP1 ⁽⁴⁾	RP0	T0	PD	Z	DC	C	0001 1xxx	000q quuu
84h ⁽¹⁾	FSR	Indirect data memory address pointer								xxxx xxxx	uuuu uuuu
85h	TRIS	—	—	GPIO Data Direction Register						0011 1111	0011 1111
86h	—	Unimplemented								—	—
87h	—	Unimplemented								—	—
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah ^(1,2)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the PC					---0 0000	---0 0000
8Bh ⁽¹⁾	INTCON	GIE	PEIE	T0IE	INTE	GPIE	TOIF	INTF	GPIF	0000 000x	0000 000u
8Ch	PIE1	—	ADIE	—	—	—	—	—	—	-0-- ----	-0-- ----
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	—	—	—	—	POR	—	---- --0-	---- --u-
8Fh	OSCCAL	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—	1000 00--	uuuu uu--
90h	—	Unimplemented								—	—
91h	—	Unimplemented								—	—
92h	—	Unimplemented								—	—
93h	—	Unimplemented								—	—
94h	—	Unimplemented								—	—
95h	—	Unimplemented								—	—
96h	—	Unimplemented								—	—
97h	—	Unimplemented								—	—
98h	—	Unimplemented								—	—
99h	—	Unimplemented								—	—
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	—	Unimplemented								—	—
9Dh	—	Unimplemented								—	—
9Eh	—	Unimplemented								—	—
9Fh	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

- Note 1: These registers can be addressed from either bank.
 2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.
 3: Other (non power-up) resets include external reset through MCLR and Watchdog Timer Reset.
 4: The IRP and RP1 bits are reserved on the PIC12CE67X, always maintain these bits clear.

4.2.2.1 STATUS REGISTER

The STATUS register, shown in Figure 4-3, contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the \overline{TO} and \overline{PD} bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as `000u u1uu` (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions, not affecting any status bits, see the "Instruction Set Summary."

Note 1: Bits IRP and RP1 (STATUS<7:6>) are not used by the PIC12CE67X and should be maintained clear. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.

Note 2: The C and DC bits operate as a borrow and digit borrow bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

FIGURE 4-3: STATUS REGISTER (ADDRESS 03h, 83h)

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	\overline{TO}	\overline{PD}	Z	DC	C
							bit0
bit7							

R = Readable bit
 W = Writable bit
 U = Unimplemented bit, read as '0'
 - n = Value at POR reset

bit 7: **IRP:** Register Bank Select bit (used for indirect addressing)
 1 = Bank 2, 3 (100h - 1FFh)
 0 = Bank 0, 1 (00h - FFh)
 The IRP bit is reserved, always maintain this bit clear.

bit 6-5: **RP1:RP0:** Register Bank Select bits (used for direct addressing)
 11 = Bank 3 (180h - 1FFh)
 10 = Bank 2 (100h - 17Fh)
 01 = Bank 1 (80h - FFh)
 00 = Bank 0 (00h - 7Fh)
 Each bank is 128 bytes. The RP1 bit is reserved, always maintain this bit clear.

bit 4: **\overline{TO} :** Time-out bit
 1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
 0 = A WDT time-out occurred

bit 3: **\overline{PD} :** Power-down bit
 1 = After power-up or by the `CLRWDT` instruction
 0 = By execution of the `SLEEP` instruction

bit 2: **Z:** Zero bit
 1 = The result of an arithmetic or logic operation is zero
 0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC:** Digit carry/borrow bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)(for borrow the polarity is reversed)
 1 = A carry-out from the 4th low order bit of the result occurred
 0 = No carry-out from the 4th low order bit of the result

bit 0: **C:** Carry/borrow bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions)
 1 = A carry-out from the most significant bit of the result occurred
 0 = No carry-out from the most significant bit of the result occurred
 Note: For borrow the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

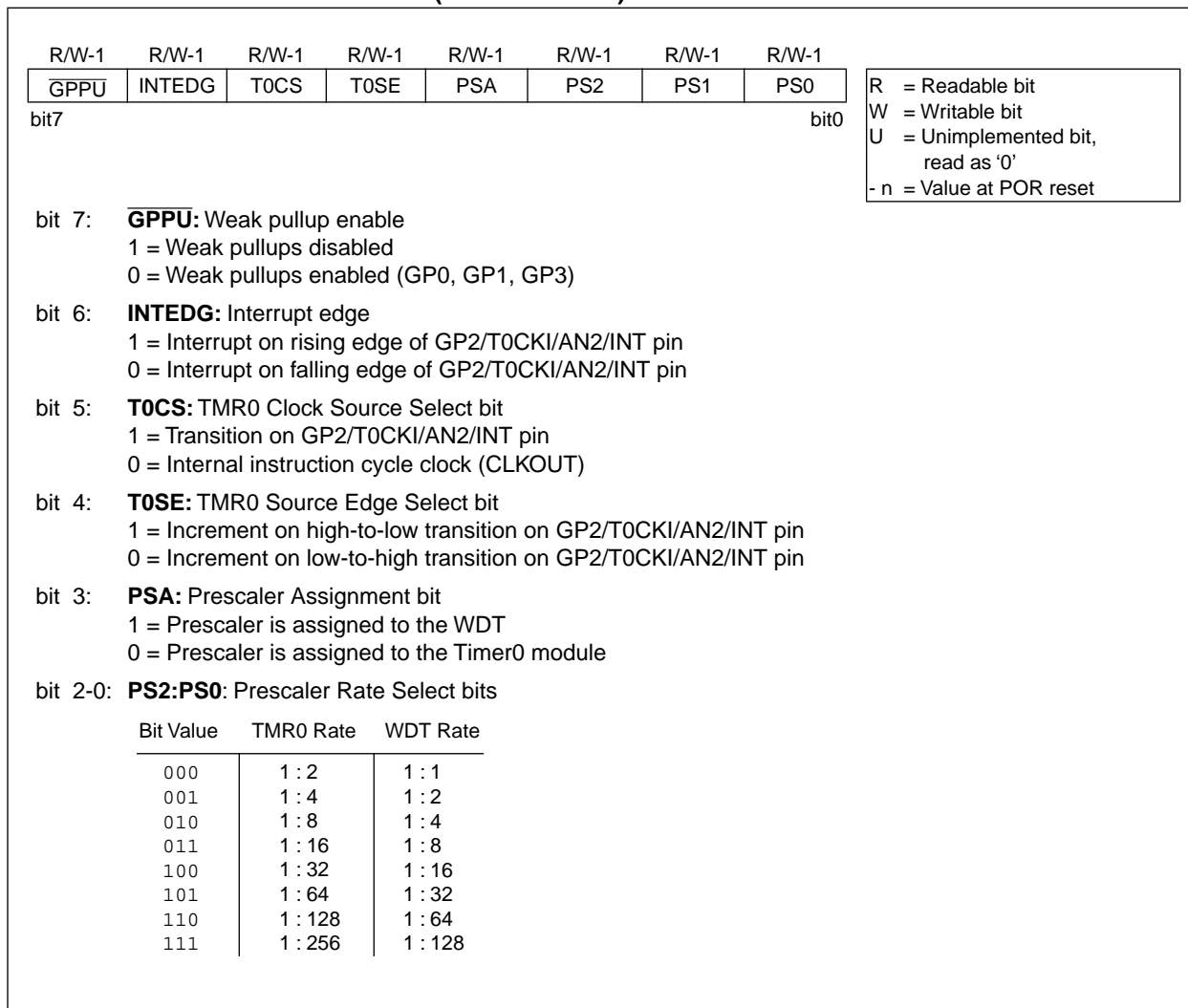
PIC12CE67X

4.2.2.2 OPTION REGISTER

The OPTION register is a readable and writable register which contains various control bits to configure the TMR0/WDT prescaler, the External INT Interrupt, TMR0, and the weak pull-ups on GPIO.

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer by setting bit PSA (OPTION<3>).

FIGURE 4-4: OPTION REGISTER (ADDRESS 81h)



4.2.2.3 INTCON REGISTER

The INTCON Register is a readable and writable register which contains various enable and flag bits for the TMR0 register overflow, GPIO Port change and External GP2/INT Pin interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

FIGURE 4-5: INTCON REGISTER (ADDRESS 0Bh, 8Bh)

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
bit7	GIE	PEIE	TOIE	INTE	GPIE	TOIF	INTF
							GPIF
							bit0

bit 7: **GIE:** Global Interrupt Enable bit
 1 = Enables all un-masked interrupts
 0 = Disables all interrupts

bit 6: **PEIE:** Peripheral Interrupt Enable bit
 1 = Enables all un-masked peripheral interrupts
 0 = Disables all peripheral interrupts

bit 5: **TOIE:** TMR0 Overflow Interrupt Enable bit
 1 = Enables the TMR0 interrupt
 0 = Disables the TMR0 interrupt

bit 4: **INTE:** INT External Interrupt Enable bit
 1 = Enables the external interrupt on GP2/INT/T0CKI/AN2 pin
 0 = Disables the external interrupt on GP2/INT/T0CKI/AN2 pin

bit 3: **GPIE:** GPIO Interrupt on Change Enable bit
 1 = Enables the GPIO Interrupt on Change
 0 = Disables the GPIO Interrupt on Change

bit 2: **TOIF:** TMR0 Overflow Interrupt Flag bit
 1 = TMR0 register has overflowed (must be cleared in software)
 0 = TMR0 register did not overflow

bit 1: **INTF:** INT External Interrupt Flag bit
 1 = The external interrupt on GP2/INT/T0CKI/AN2 pin occurred (must be cleared in software)
 0 = The external interrupt on GP2/INT/T0CKI/AN2 pin did not occur

bit 0: **GPIF:** GPIO Interrupt on Change Flag bit
 1 = GP0, GP1, or GP3 pins changed state (must be cleared in software)
 0 = Neither GP0, GP1, nor GP3 pins have changed state

R = Readable bit
 W = Writable bit
 U = Unimplemented bit, read as '0'
 - n = Value at POR reset

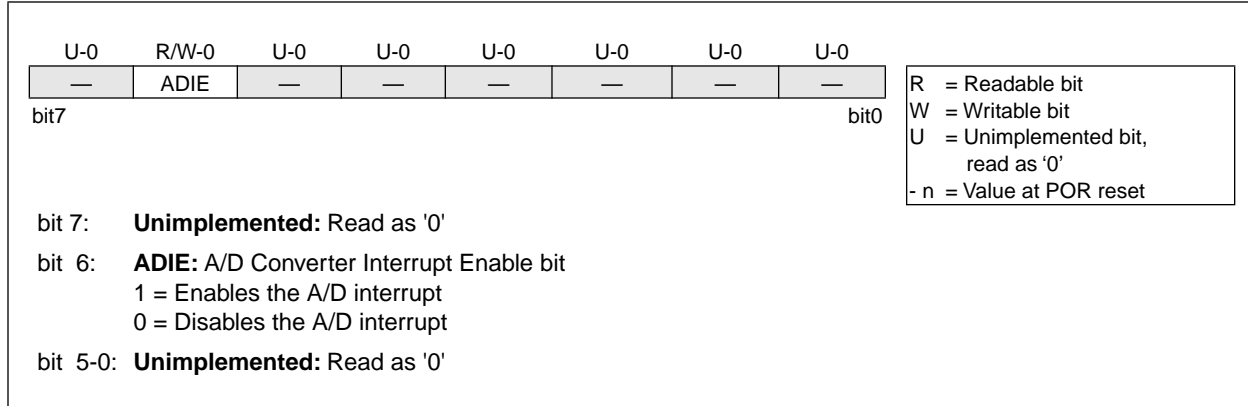
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4.2.2.4 PIE1 REGISTER

This register contains the individual enable bits for the Peripheral interrupts.

Note: Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

FIGURE 4-6: PIE1 REGISTER (ADDRESS 8Ch)

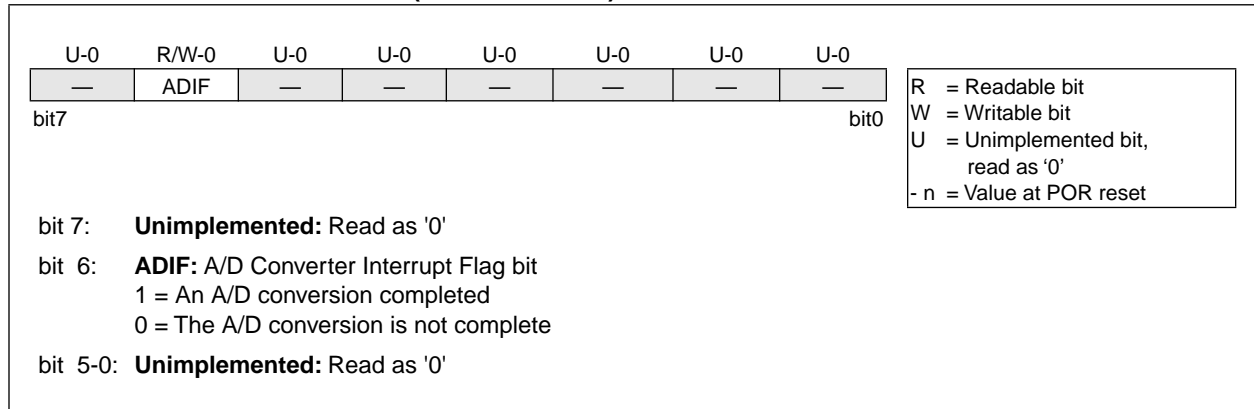


4.2.2.5 PIR1 REGISTER

This register contains the individual flag bits for the Peripheral interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 4-7: PIR1 REGISTER (ADDRESS 0Ch)

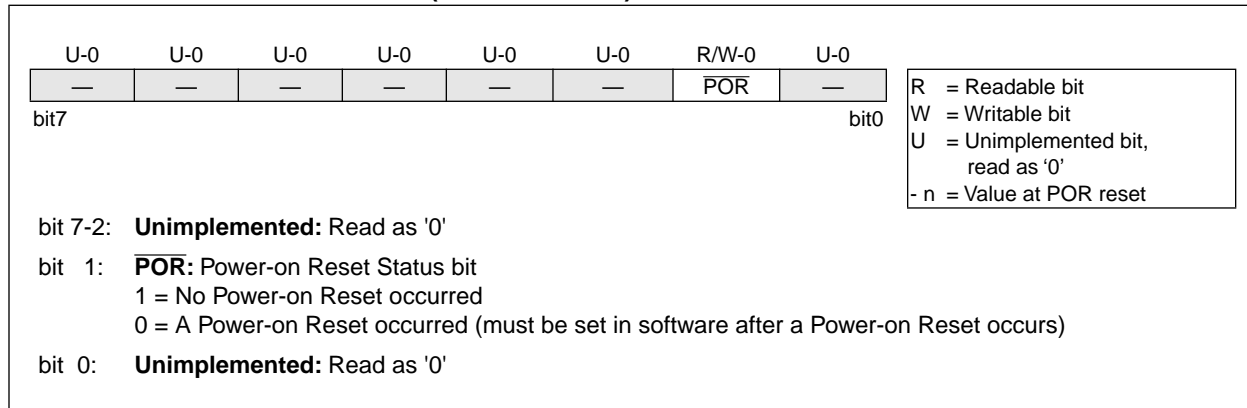


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4.2.2.6 PCON REGISTER

The Power Control (PCON) register contains a flag bit to allow differentiation between a Power-on Reset (POR), an external $\overline{\text{MCLR}}$ Reset, and WDT Reset.

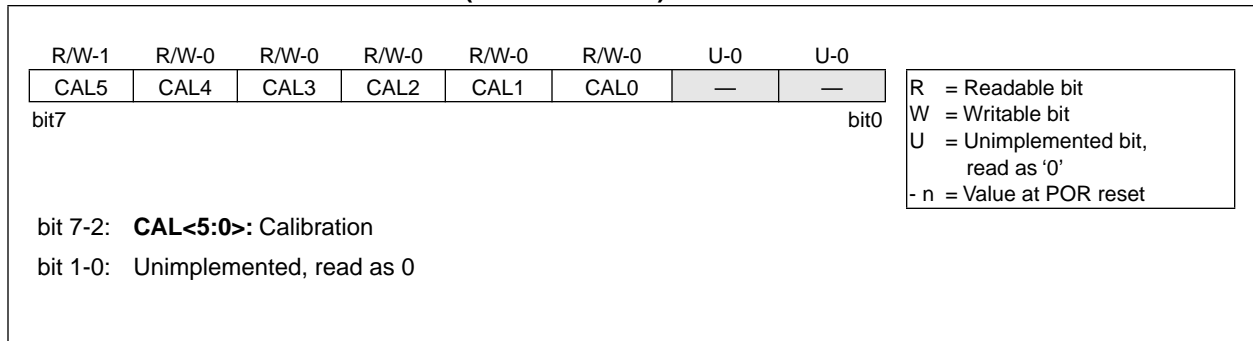
FIGURE 4-8: PCON REGISTER (ADDRESS 8Eh)



4.2.2.7 OSCCAL REGISTER

The Oscillator Calibration (OSCCAL) register is used to calibrate the internal 4 MHz oscillator. It contains six bits for calibration. Increasing the cal value increases the frequency.

FIGURE 4-9: OSCCAL REGISTER (ADDRESS 8Fh)

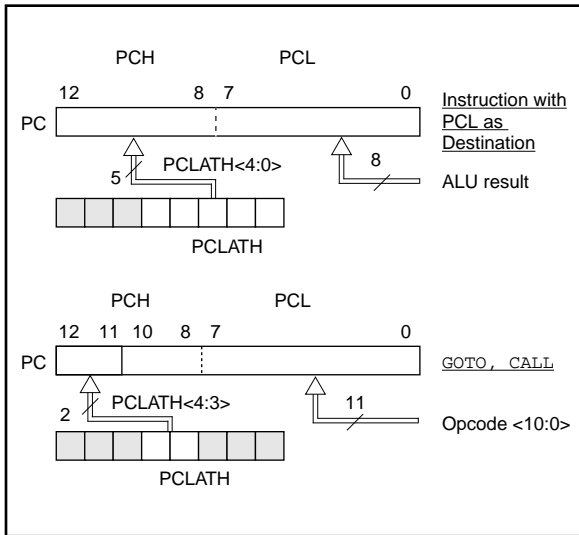


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4.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<12:8>) is not directly readable or writable and comes from PCLATH. On any reset, the PC is cleared. Figure 4-10 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 4-10: LOADING OF PC IN DIFFERENT SITUATIONS



4.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256 byte block). Refer to the application note "Implementing a Table Read" (AN556).

4.3.2 STACK

The PIC12CE67X family has an 8 level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no status bits to indicate stack overflow or stack underflow conditions.

Note 2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW, and RETFIE instructions, or the vectoring to an interrupt address.

4.4 Program Memory Paging

The PIC12CE67X ignores both paging bits PCLATH<4:3>, which are used to access program memory when more than one page is available. The use of PCLATH<4:3> as general purpose read/write bits for the PIC12CE67X is not recommended since this may affect upward compatibility with future products.

4.5 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses the register pointed to by the File Select Register, FSR. Reading the INDF register itself indirectly (FSR = '0') will read 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 4-11. However, IRP is not used in the PIC12CE67X.

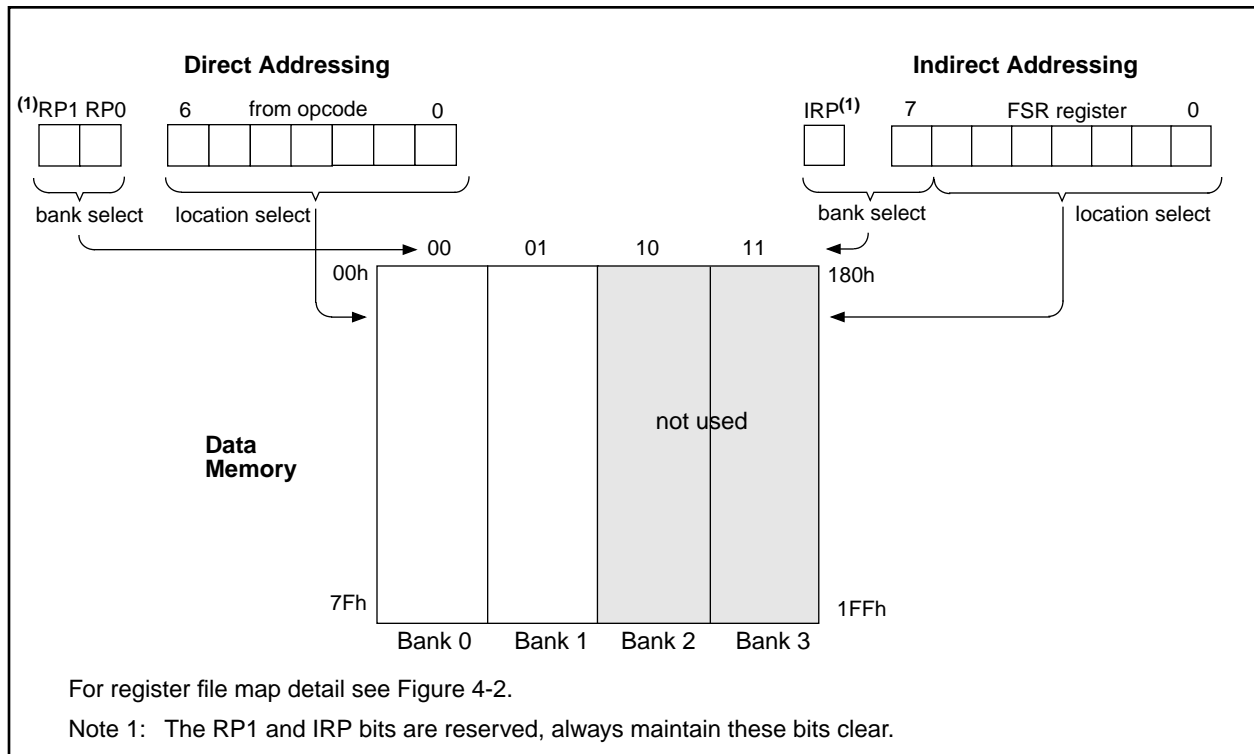
A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 4-1.

EXAMPLE 4-1: INDIRECT ADDRESSING

```

movlw 0x20 ;initialize pointer
movwf FSR ;to RAM
NEXT  clrf  INDF ;clear INDF register
      incf  FSR,F ;inc pointer
      btfss FSR,4 ;all done?
      goto NEXT ;no clear next
CONTINUE
      : ;yes continue
    
```

FIGURE 4-11: DIRECT/INDIRECT ADDRESSING



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NOTES:

5.0 I/O PORT

As with any other register, the I/O register can be written and read under program control. However, read instructions (e.g., `MOVF GPIO, W`) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers are all set.

5.1 GPIO

GPIO is an 8-bit I/O register. Only the low order 6 bits are used (GP5:GP0). Bits 6 and 7 (SDA and SCL) are used by the EEPROM peripheral. Refer to Section 6.0 and Appendix A for use of SDA and SCL. Please note that GP3 is an input only pin. The configuration word can set several I/O's to alternate functions. When acting as alternate functions the pins will read as '0' during port read. Pins GP0, GP1, and GP3 can be configured with weak pull-ups and also with interrupt on change. The interrupt on change and weak pull-up functions are not pin selectable. If pin 4 is configured as MCLR, the weak pull-up is always on. Interrupt on change for this pin is not set and GP3 will read as '0'. Interrupt on change is enabled by setting `INTCON<3>`. Note that external oscillator use overrides the GPIO functions on GP4 and GP5.

5.2 TRIS Register

This register controls the data direction for GPIO. A '1' from a TRIS register bit puts the corresponding output driver in a hi-impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer. The exceptions are GP3 which is input only and its TRIS bit will always read as '1'.

Note: A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.

Upon reset, the TRIS register is all '1's, making all pins inputs.

TRIS for pins GP4 and GP5 is forced to a 1 where appropriate. Writes to `TRIS <5:4>` will have an effect in EXTRC and INTRC oscillator modes only. When GP4 is configured as CLKOUT, changes to `TRIS<4>` will have no effect.

5.3 I/O Interfacing

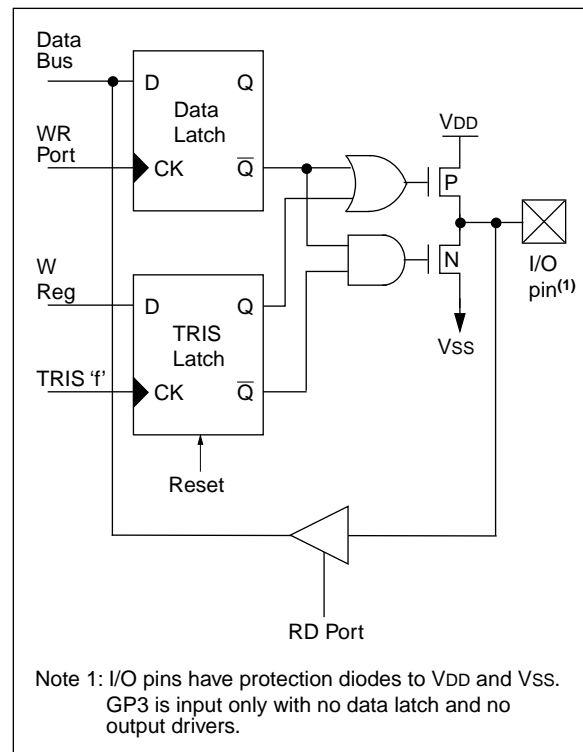
The equivalent circuit for an I/O port pin is shown in Figure 5-2. All port pins, except GP3 which is input only, may be used for both input and output operations. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., `MOVF GPIO, W`). The outputs are latched and remain unchanged until the output latch is

rewritten. To use a port pin as output, the corresponding direction control bit in TRIS must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin (except GP3) can be programmed individually as input or output.

Port pins GP6 and GP7 are used for the serial EEPROM interface. These port pins are not available externally on the package. Users should avoid writing to pins GP6 and GP7 when not communicating with the serial EEPROM memory. Please see section 6.0, EEPROM Peripheral Operation, for information on serial EEPROM communication.

Note: On a Power-on Reset, GP0, GP1, GP2, GP4 are configured as analog inputs and read as '0'.

FIGURE 5-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



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TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other Resets
85h	TRIS	—	—	GPIO Data Direction Register						--11 1111	--11 1111
81h	OPTION	$\overline{\text{GPPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
03h	STATUS	IRP ⁽¹⁾	RP1 ⁽¹⁾	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu
05h	GPIO	SCL	SDA	GP5	GP4	GP3	GP2	GP1	GP0	11xx xxxx	11uu uuuu

Legend: Shaded cells not used by Port Registers, read as '0', — = unimplemented, read as '0', x = unknown, u = unchanged, q = see tables in Section 9.4 for possible values.

Note 1: The IRP and RP1 bits are reserved on the PIC12CE67X, always maintain these bits clear.

5.4 I/O Programming Considerations

5.4.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read followed by a write operation. The BCF and BSF instructions, for example, read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of GPIO will cause all eight bits of GPIO to be read into the CPU. Then the BSF operation takes place on bit5 and GPIO is written to the output latches. If another bit of GPIO is used as a bi-directional I/O pin (e.g., bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched to an output, the content of the data latch may now be unknown.

Reading the port register, reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (ex. BCF, BSF, etc.) on a port, the value of the port pins is read, the desired operation is done to this value, and this value is then written to the port latch.

Example 5-1 shows the effect of two sequential read-modify-write instructions on an I/O port.

EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

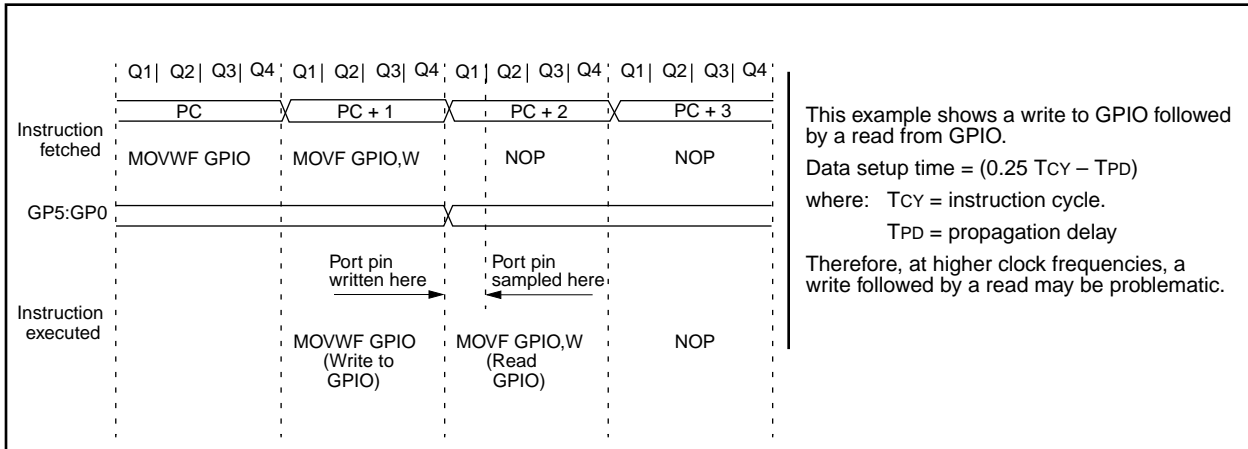
```

;Initial GPIO Settings
; GPIO<5:3> Inputs
; GPIO<2:0> Outputs
;
;
;           GPIO latch  GPIO pins
;           -----  -----
BCF  GPIO, 5 ;--01 -ppp  --11 pppp
BCF  GPIO, 4 ;--10 -ppp  --11 pppp
MOVLW 007h ;
TRIS GPIO ;--10 -ppp  --11 pppp
;
;Note that the user may have expected the pin
;values to be --00 pppp. The 2nd BCF caused
;GP5 to be latched as the pin value (High).

```

A pin actively outputting a Low or High should not be driven from external devices at the same time in order to change the level on this pin (“wired-or”, “wired-and”). The resulting high output currents may damage the chip.

FIGURE 5-2: SUCCESSIVE I/O OPERATION



6.0 EEPROM PERIPHERAL OPERATION

The PIC12CE673 and PIC12CE674 each have 16 bytes of EEPROM data memory. The EEPROM memory has an endurance of 1,000,000 erase/write cycles and a data retention of greater than 40 years. The EEPROM data memory supports a bi-directional 2-wire bus and data transmission protocol. These two-wires are serial data (SDA) and serial clock (SCL), that are mapped to bit6 and bit7, respectively, of the GPIO register (SFR 06h). Unlike the GP0-GP5 that are connected to the I/O pins, SDA and SCL are only connected to the internal EEPROM peripheral. For most applications, all that is required is calls to the following functions:

```
; Byte_Write: Byte write routine
;   Inputs: EEPROM Address   EEADDR
;           EEPROM Data     EEDATA
;   Outputs: Return 01 in W if OK, else
;            return 00 in W
;
; Read_Current: Read EEPROM at address
;               currently held by EE device.
;   Inputs: NONE
;   Outputs: EEPROM Data     EEDATA
;            Return 01 in W if OK, else
;            return 00 in W
;
; Read_Random: Read EEPROM byte at supplied
;              address
;   Inputs: EEPROM Address   EEADDR
;   Outputs: EEPROM Data     EEDATA
;            Return 01 in W if OK,
;            else return 00 in W
```

The code for these functions is available on our web site (www.microchip.com). The code will be accessed by either including the source code FL67XINC.ASM or by linking FLASH67X.ASM. FLASH62.IMC provides external definition to the calling program.

6.0.1 SERIAL DATA

SDA is a bi-directional pin used to transfer addresses and data into and data out of the device.

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

6.0.2 SERIAL CLOCK

This SCL input is used to synchronize the data transfer from and to the EEPROM.

6.1 BUS CHARACTERISTICS

The following **bus protocol** is to be used with the EEPROM data memory. In this section, the term "processor" is used to denote the portion of the PIC12CE67X that interfaces to the EEPROM via software.

- Data transfer may be initiated only when the bus is not busy.

During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 6-1).

6.1.1 BUS NOT BUSY (A)

Both data and clock lines remain HIGH.

6.1.2 START DATA TRANSFER (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

6.1.3 STOP DATA TRANSFER (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

6.1.4 DATA VALID (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the processor device and is theoretically unlimited.

6.1.5 ACKNOWLEDGE

The EEPROM, when addressed, will generate an acknowledge after the reception of each byte. The processor must generate an extra clock pulse which is associated with this acknowledge bit.

Note: Acknowledge bits are not generated if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. The processor must signal an end of data to the EEPROM by not generating an acknowledge bit on the last byte that has been clocked out of the EEPROM. In this case, the EEPROM must leave the data line HIGH to enable the processor to generate the STOP condition (Figure 6-2).

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FIGURE 6-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

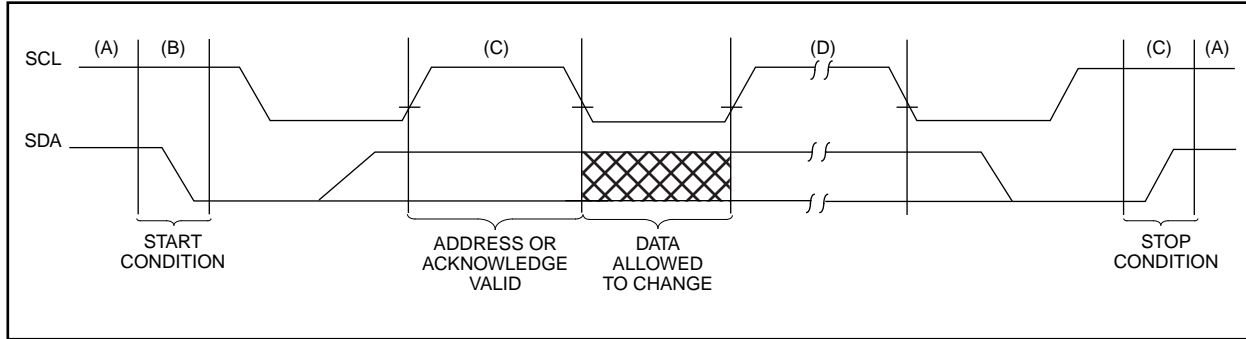
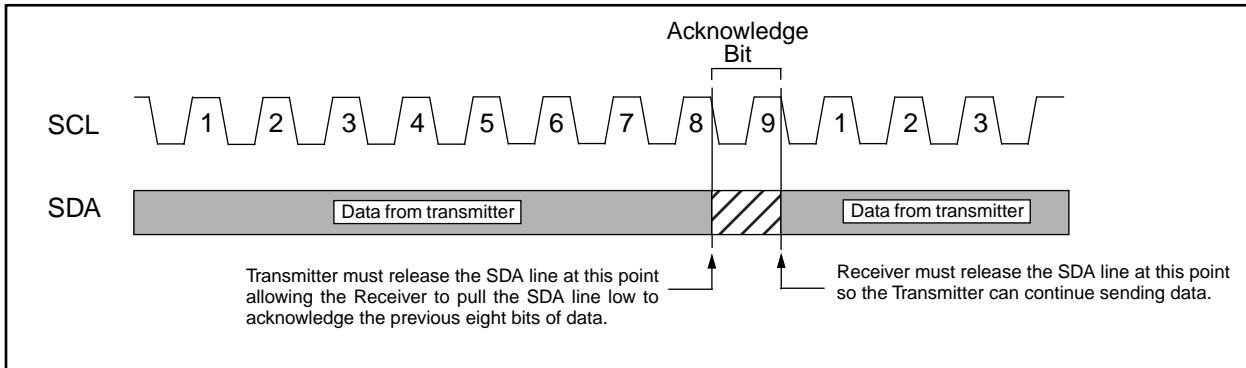


FIGURE 6-2: ACKNOWLEDGE TIMING

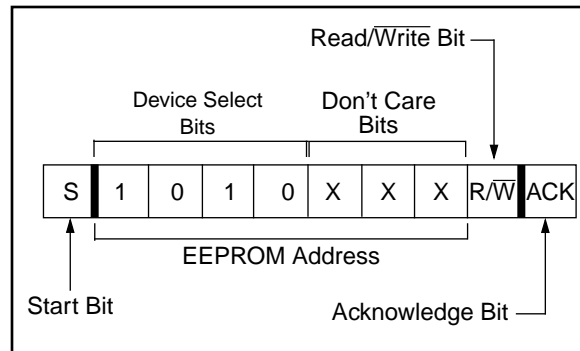


6.2 Device Addressing

After generating a START condition, the processor transmits a control byte consisting of a EEPROM address and a Read/Write bit that indicates what type of operation is to be performed. The EEPROM address consists of a 4-bit device code (1010) followed by three don't care bits.

The last bit of the control byte determines the operation to be performed. When set to a one a read operation is selected, and when set to a zero a write operation is selected. (Figure 6-3). The bus is monitored for its corresponding EEPROM address all the time. It generates an acknowledge bit if the EEPROM address was true and it is not in a programming mode.

FIGURE 6-3: CONTROL BYTE FORMAT



6.3 WRITE OPERATIONS

6.3.1 BYTE WRITE

Following the start signal from the processor, the device code (4 bits), the don't care bits (3 bits), and the R/W bit (which is a logic low) are placed onto the bus by the processor. This indicates to the addressed EEPROM that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the processor is the word address and will be written into the address pointer. Only the lower four address bits are used by the device, and the upper four bits are don't cares. The address byte is acknowledgeable and the processor will then transmit the data word to be written into the addressed memory location. The memory acknowledges again and the processor generates a stop condition. This initiates the internal write cycle, and during this time will not generate acknowledge signals (Figure 6-5). After a byte write command, the internal address counter will not be incremented and will point to the same address location that was just written. If a stop bit is transmitted to the device at any point in the write command sequence before the entire sequence is complete, then the command will abort and no data will be written. If more than 8 data bits are transmitted before the stop bit is sent, then the device will clear the previously loaded byte and begin loading the data buffer again. If more than one data byte is transmitted to the device and a stop bit is sent before a full eight data bits have been transmitted, then the write command will abort and no data will be written. The EEPROM memory employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below minimum VDD. Byte write operations must be preceded and immediately followed by a bus not busy bus cycle where both SDA and SCL are held high.

6.4 ACKNOWLEDGE POLLING

Since the EEPROM will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the processor, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the processor sending a start condition followed by the control byte for a write command (R/W = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the start bit and control byte must be re-sent. If the cycle is complete, then the device will return the ACK and the processor can then proceed with the next read or write command. See Figure 6-4 for flow diagram.

FIGURE 6-4: ACKNOWLEDGE POLLING FLOW

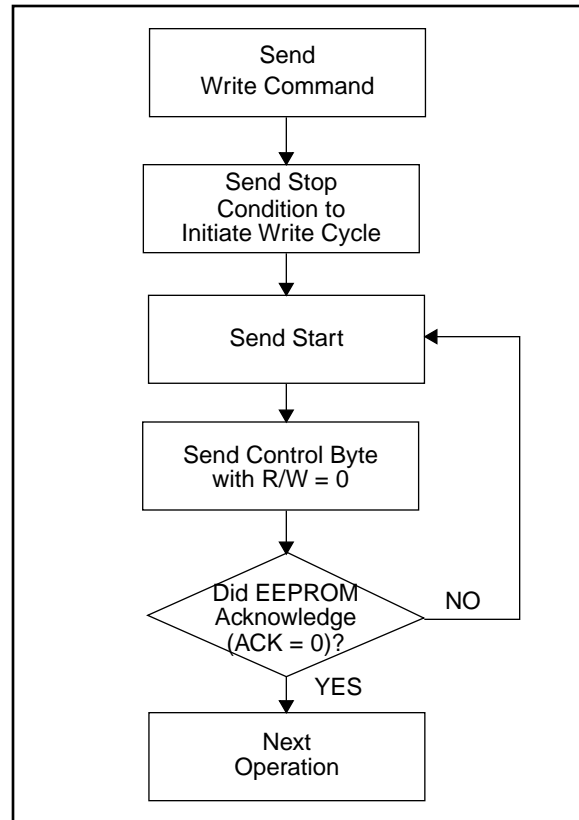
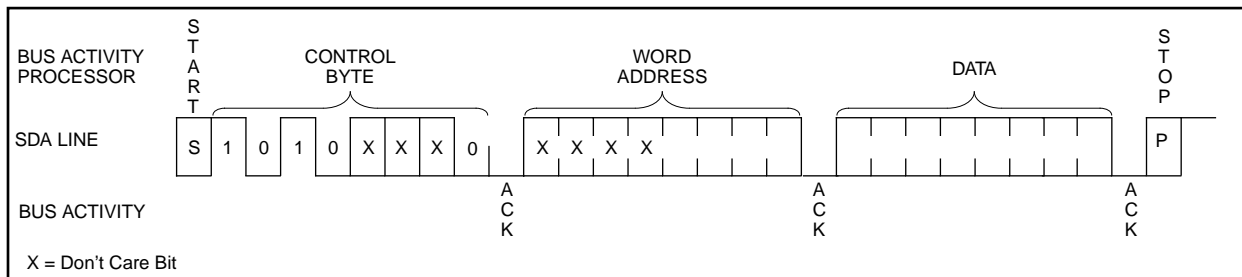


FIGURE 6-5: BYTE WRITE



6.5 READ OPERATIONS

Read operations are initiated in the same way as write operations with the exception that the R/\bar{W} bit of the EEPROM address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

6.5.1 CURRENT ADDRESS READ

It contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n , the next current address read operation would access data from address $n + 1$. Upon receipt of the EEPROM address with the R/\bar{W} bit set to one, the EEPROM issues an acknowledge and transmits the eight bit data word. The processor will not acknowledge the transfer but does generate a stop condition and the EEPROM discontinues transmission (Figure 6-6).

6.5.2 RANDOM READ

Random read operations allow the processor to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the

EEPROM as part of a write operation. After the word address is sent, the processor generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the processor issues the control byte again but with the R/\bar{W} bit set to a one. It will then issue an acknowledge and transmits the eight bit data word. The processor will not acknowledge the transfer but does generate a stop condition and the EEPROM discontinues transmission (Figure 6-7). After this command, the internal address counter will point to the address location following the one that was just read.

6.5.3 SEQUENTIAL READ

Sequential reads are initiated in the same way as a random read except that after the device transmits the first data byte, the processor issues an acknowledge as opposed to a stop condition in a random read. This directs the EEPROM to transmit the next sequentially addressed 8-bit word (Figure 6-8).

To provide sequential reads, it contains an internal address pointer which is incremented by one at the completion of each read operation. This address pointer allows the entire memory contents to be serially read during one operation.

FIGURE 6-6: CURRENT ADDRESS READ

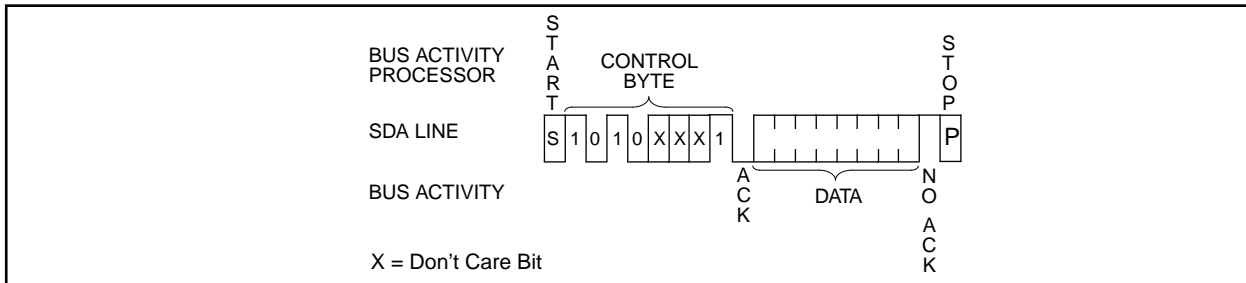


FIGURE 6-7: RANDOM READ

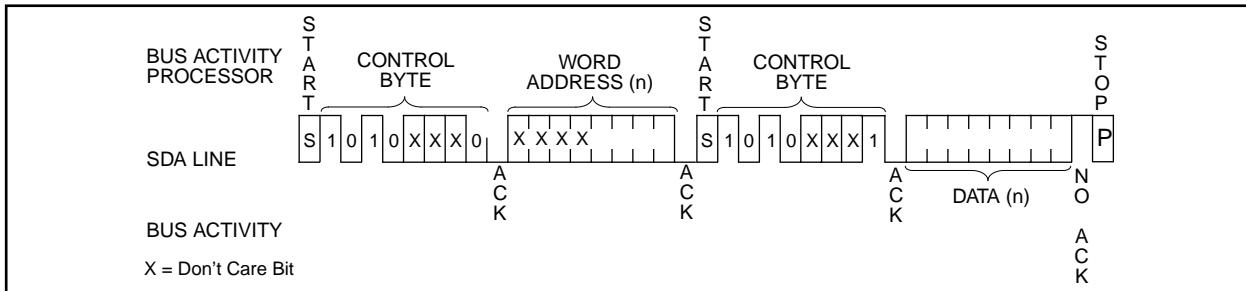
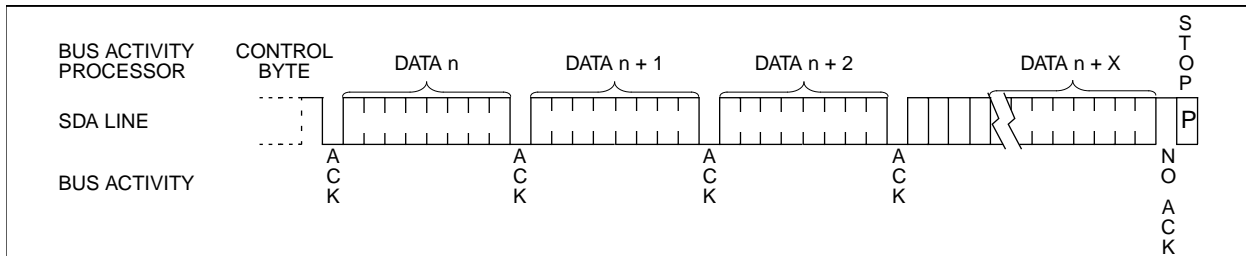


FIGURE 6-8: SEQUENTIAL READ



7.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 7-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing bit T0CS (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles (Figure 7-2 and Figure 7-3). The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting bit T0CS (OPTION<5>). In counter mode, Timer0 will increment either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit T0SE (OPTION<4>). Clearing

bit T0SE selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 7.2.

The prescaler is mutually exclusively shared between the Timer0 module and the Watchdog Timer. The prescaler assignment is controlled in software by control bit PSA (OPTION<3>). Clearing bit PSA will assign the prescaler to the Timer0 module. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4, ..., 1:256 are selectable. Section 7.3 details the operation of the prescaler.

7.1 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit T0IF (INTCON<2>). The interrupt can be masked by clearing bit T0IE (INTCON<5>). Bit T0IF must be cleared in software by the Timer0 module interrupt service routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP since the timer is shut off during SLEEP. See Figure 7-4 for Timer0 interrupt timing.

FIGURE 7-1: TIMER0 BLOCK DIAGRAM

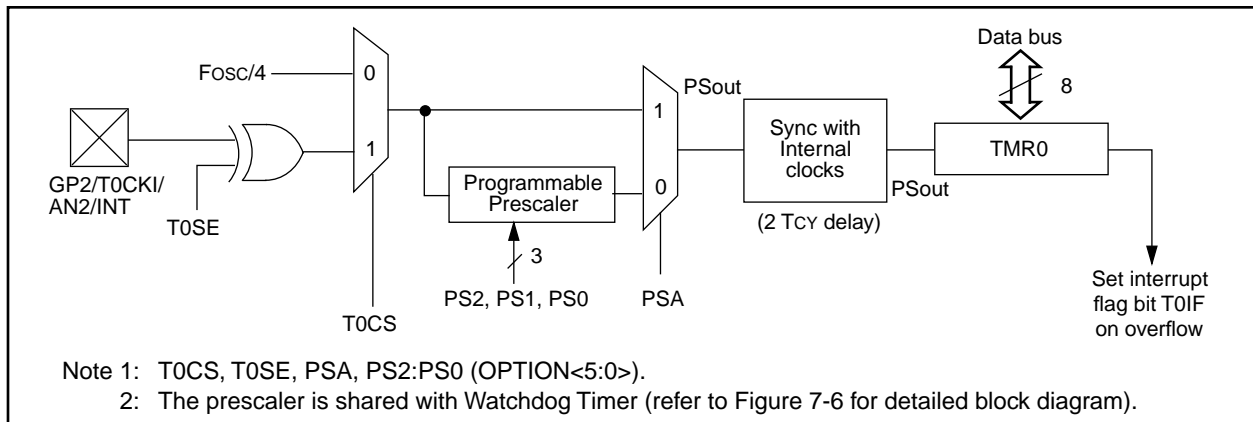
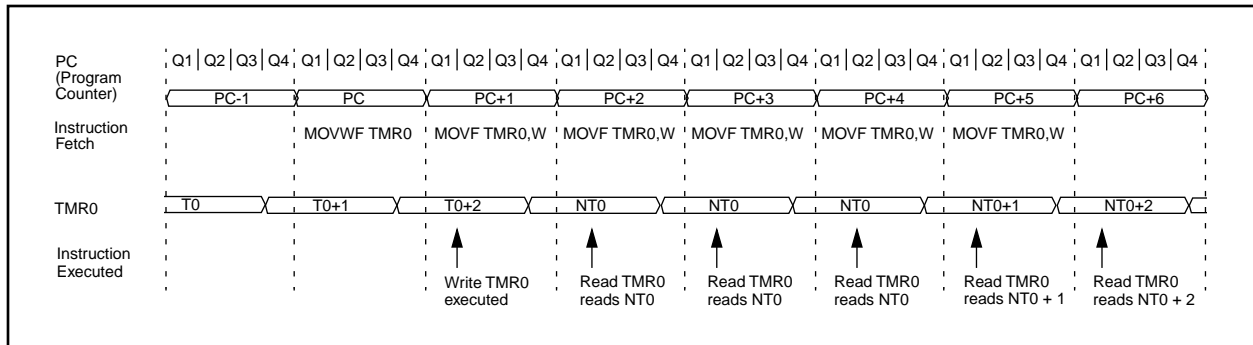


FIGURE 7-2: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE



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FIGURE 7-3: TMR0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

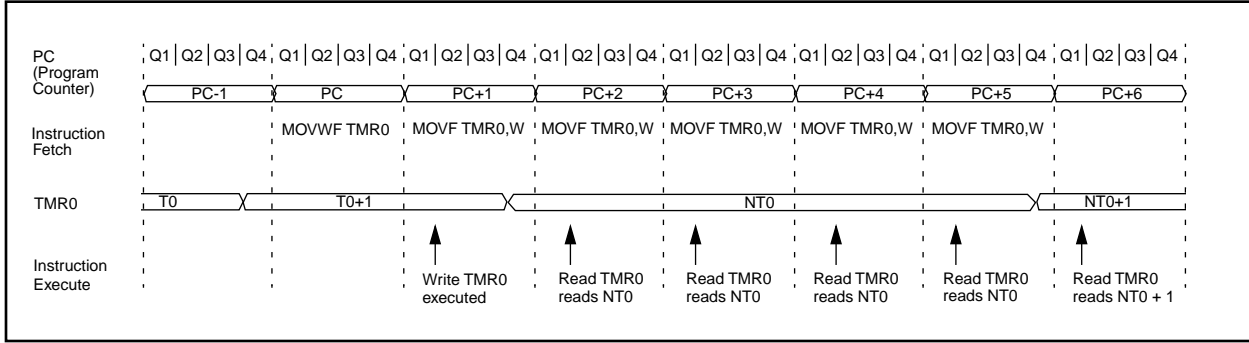
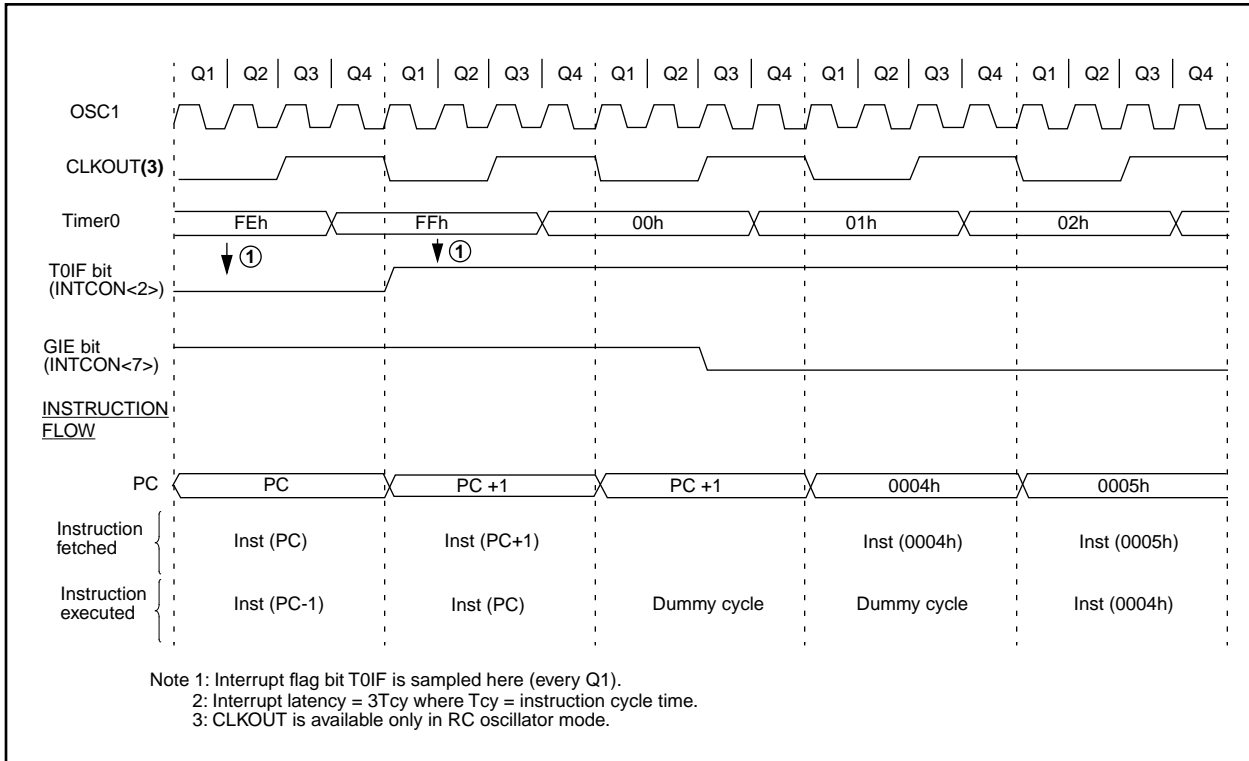


FIGURE 7-4: TMR0 INTERRUPT TIMING



7.2 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (TOSC). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

7.2.1 EXTERNAL CLOCK SYNCHRONIZATION

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 7-5). Therefore, it is necessary for T0CKI to be high for at least $2T_{osc}$ (and a small RC delay of 20 ns) and low for at least $2T_{osc}$ (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

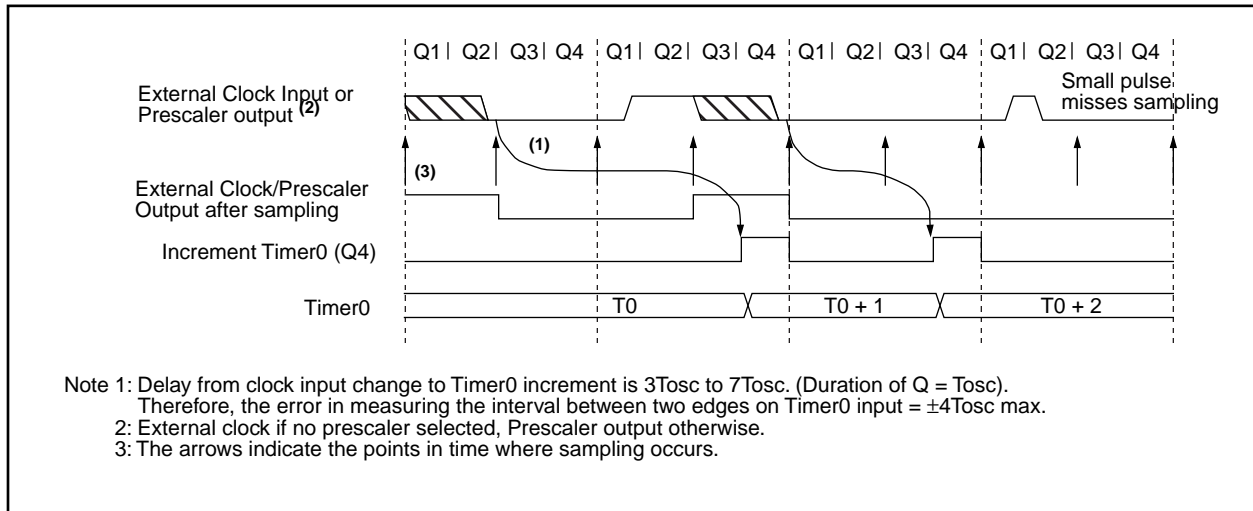
When a prescaler is used, the external clock input is divided by the asynchronous ripple-counter type pres-

caler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple-counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least $4T_{osc}$ (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

7.2.2 TMR0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 7-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 7-5: TIMER0 TIMING WITH EXTERNAL CLOCK



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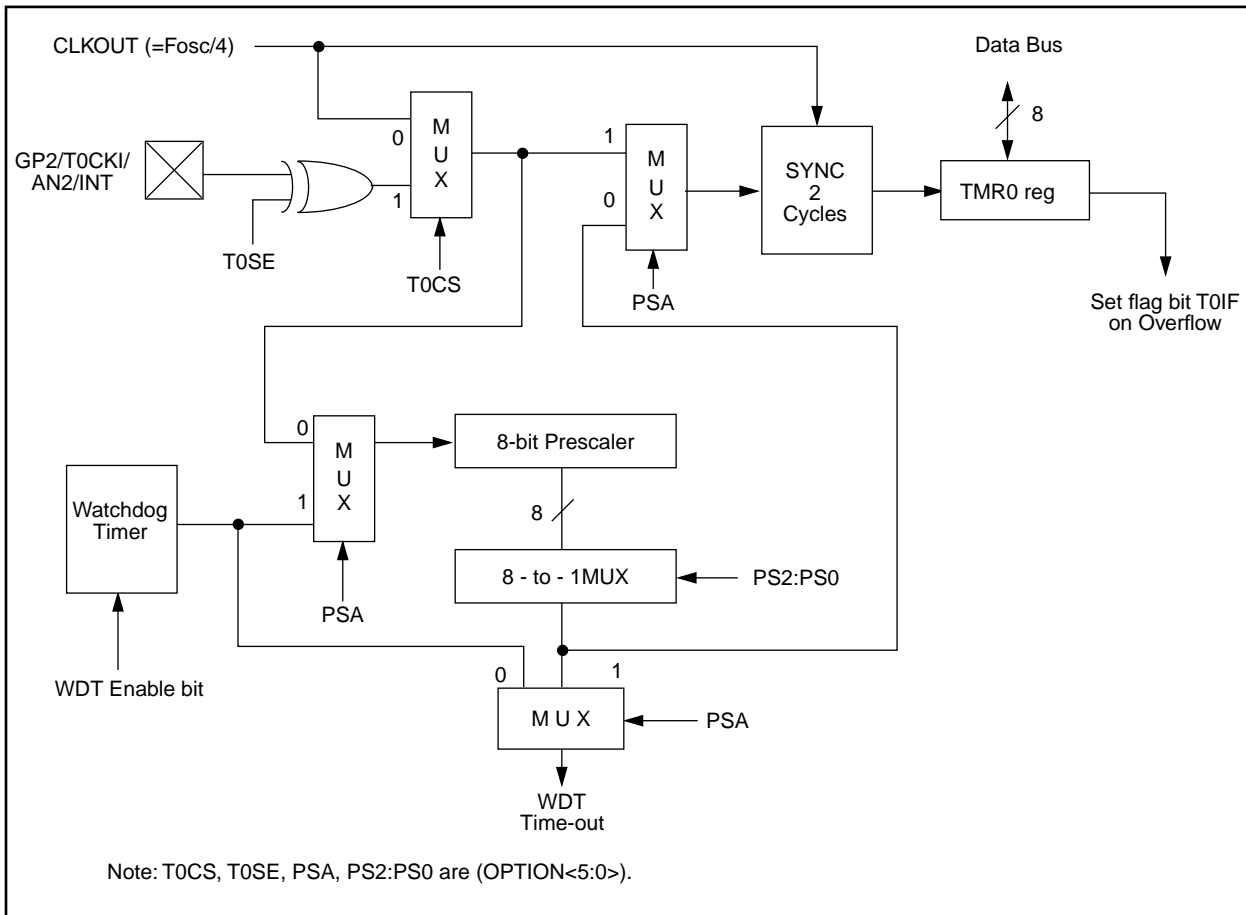
7.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer, respectively (Figure 7-6). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that there is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the Watchdog Timer, and vice-versa.

The PSA and PS2:PS0 bits (OPTION<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g. `CLRF 1`, `MOVWF 1`, `BSF 1,x...` etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

FIGURE 7-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



7.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, i.e., it can be changed “on the fly” during program execution.

Note: To avoid an unintended device RESET, the following instruction sequence (shown in Example 7-1) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled.

EXAMPLE 7-1: CHANGING PRESCALER (TIMER0→WDT)

```
BCF STATUS, RP0 ;Bank 0
CLRF TMR0 ;Clear TMR0 & Prescaler
BSF STATUS, RP0 ;Bank 1
CLRWDT ;Clears WDT
MOVLW b'xxxx1xxx' ;Select new prescale
MOVWF OPTION_REG ;value & WDT
BCF STATUS, RP0 ;Bank 0
```

To change prescaler from the WDT to the Timer0 module use the sequence shown in Example 7-2.

EXAMPLE 7-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT ;Clear WDT and
;prescaler
BSF STATUS, RP0 ;Bank 1
MOVLW b'xxxx0xxx' ;Select TMR0, new
;prescale value and
MOVWF OPTION_REG ;clock source
BCF STATUS, RP0 ;Bank 0
```

TABLE 7-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other Resets
01h	TMR0	Timer0 module's register								xxxx xxxx	uuuu uuuu
0Bh/8Bh	INTCON	GIE	PEIE	TOIE	INTE	GPIE	TOIF	INTF	GPIF	0000 000x	0000 000u
81h	OPTION	GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRIS	—	—	TRIS5	TRIS4	TRIS3	TRIS2	TRIS1	TRIS0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

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NOTES:

8.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The analog-to-digital (A/D) converter module has four analog inputs.

The A/D allows conversion of an analog input signal to a corresponding 8-bit digital number (refer to Application Note AN546 for use of A/D Converter). The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltage is software selectable to either the device's positive supply voltage (VDD) or the voltage level on the GP1/AN1/VREF pin. The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode.

The A/D module has three registers. These registers are:

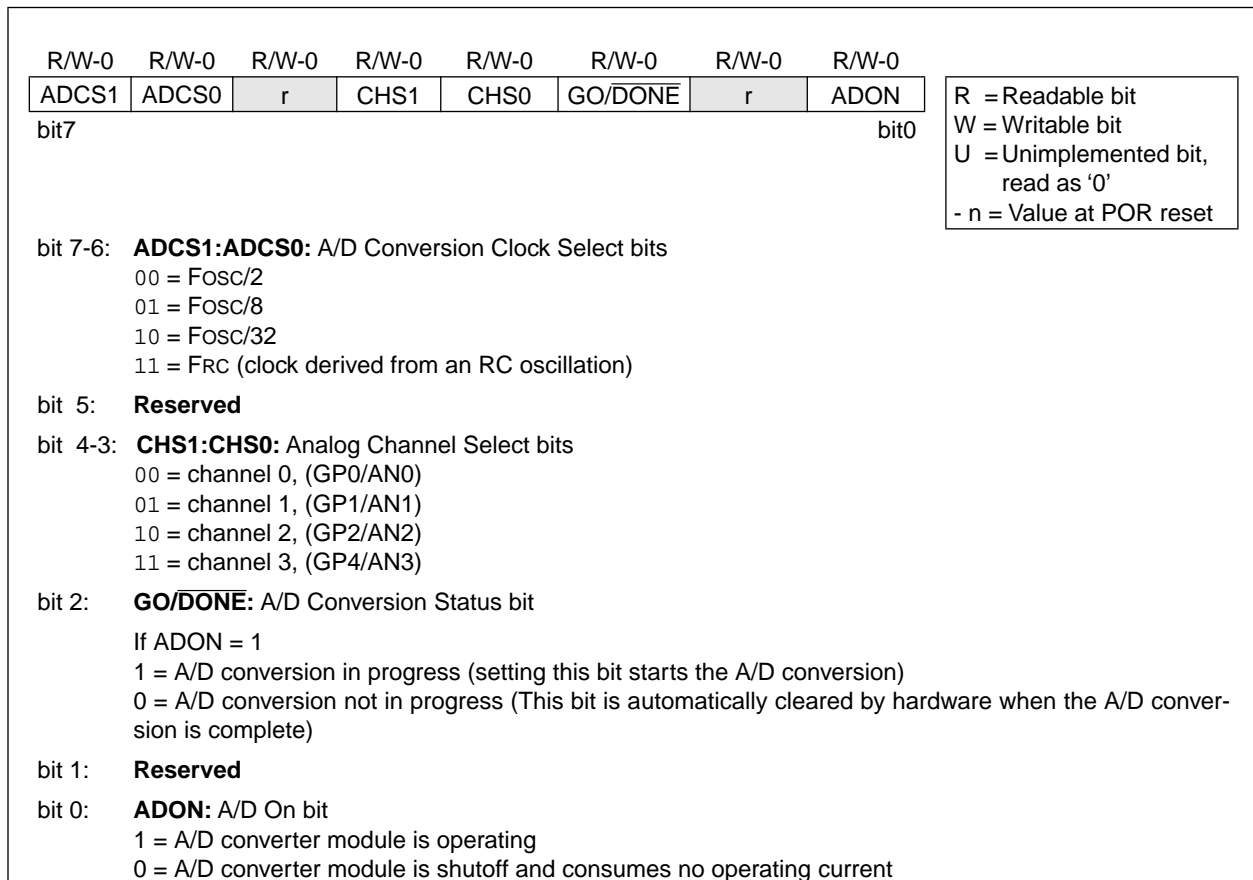
- A/D Result Register (ADRES)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

The ADCON0 register, shown in Figure 8-1, controls the operation of the A/D module. The ADCON1 register, shown in Figure 8-2, configures the functions of the port pins. The port pins can be configured as analog inputs (GP1 can also be a voltage reference) or as digital I/O.

Note: If the port pins are configured as analog inputs (reset condition), reading the port (MOVF GP,W) results in reading '0's.

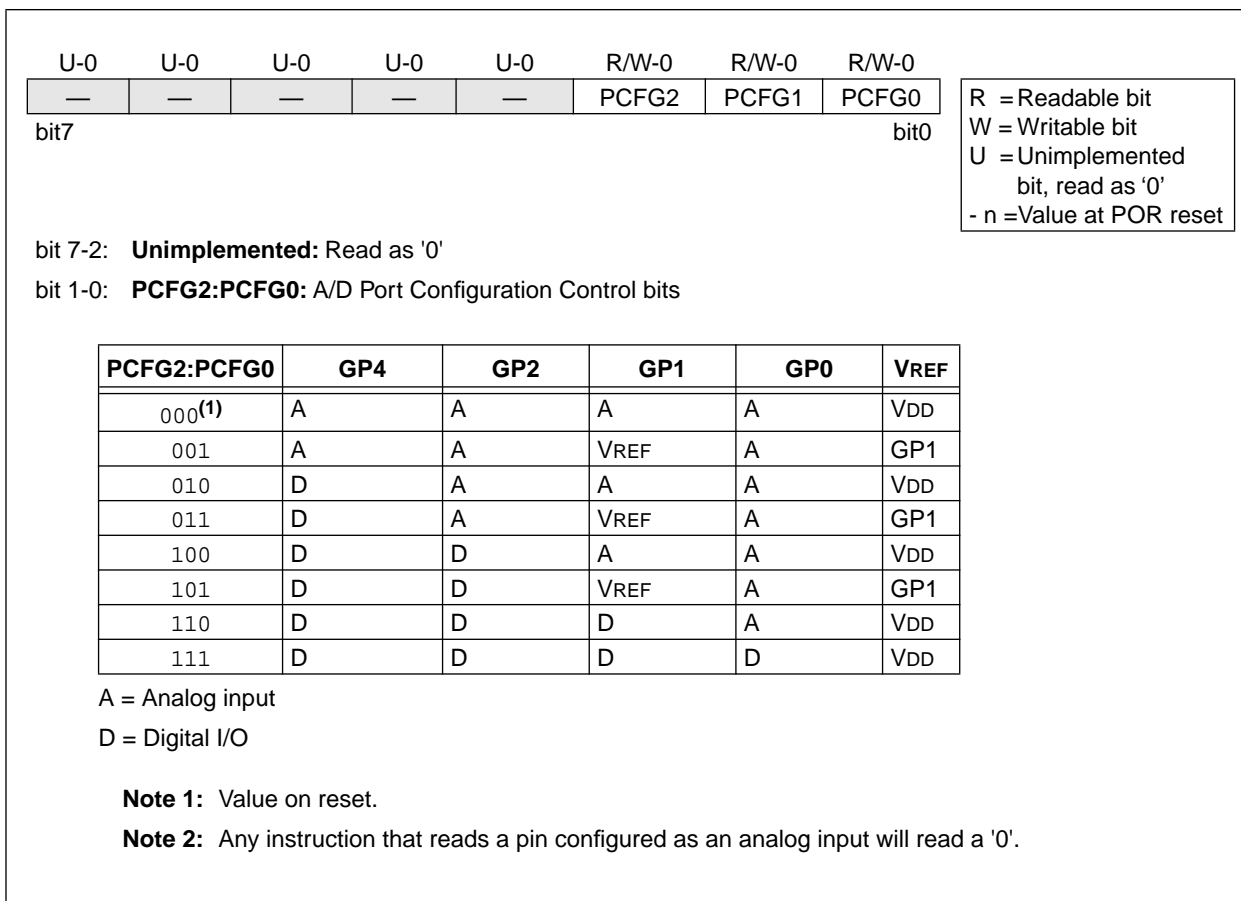
Note: Changing ADCON1 register can cause the GPIF and INTF flags to be set in the INTCON register. These interrupts should be disabled prior to modifying ADCON1.

FIGURE 8-1: ADCON0 REGISTER (ADDRESS 1Fh)



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FIGURE 8-2: ADCON1 REGISTER (ADDRESS 9Fh)

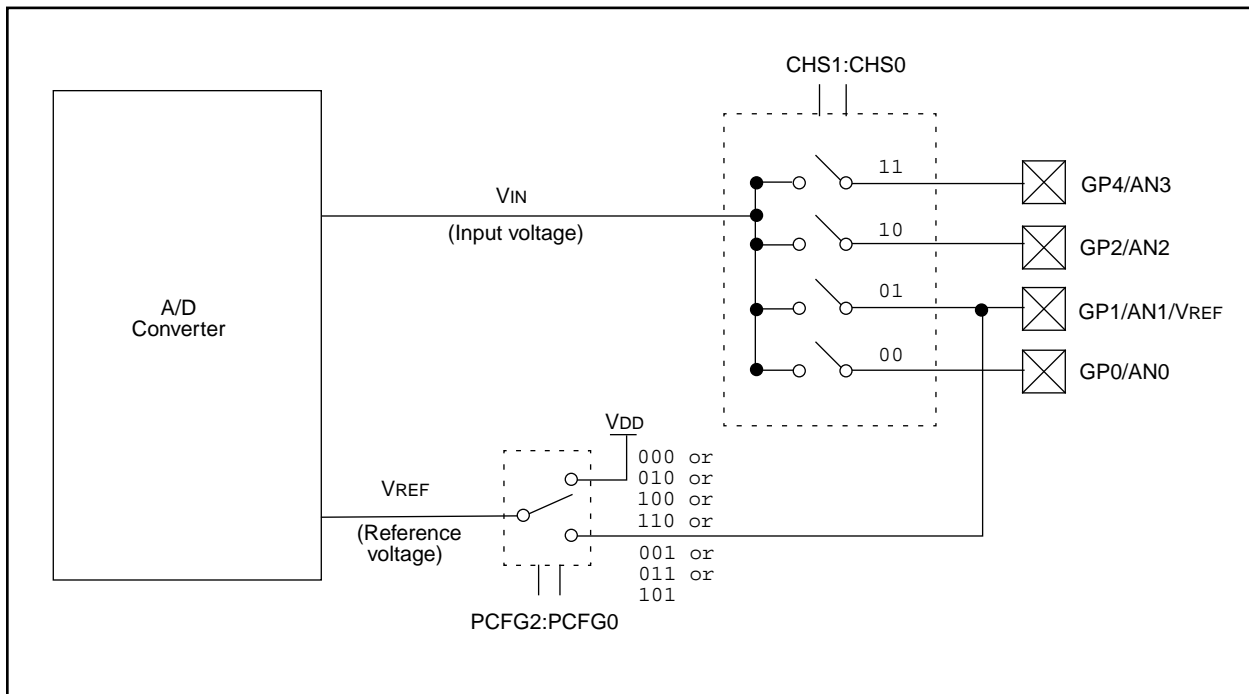


The ADRES register contains the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRES register, the GO/DONE bit (ADCON0<2>) is cleared, and A/D interrupt flag bit ADIF (PIE1<6>) is set. The block diagrams of the A/D module are shown in Figure 8-3.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine sample time, see Section 8.1. After this acquisition time has elapsed the A/D conversion can be started. The following steps should be followed for doing an A/D conversion:

1. Configure the A/D module:
 - Configure analog pins / voltage reference / and digital I/O (ADCON1)
 - Select A/D input channel (ADCON0)
 - Select A/D conversion clock (ADCON0)
 - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
 - Clear ADIF bit
 - Set ADIE bit
 - Set GIE bit
3. Wait the required acquisition time.
4. Start conversion:
 - Set GO/DONE bit (ADCON0)
5. Wait for A/D conversion to complete, by either:
 - Polling for the GO/DONE bit to be cleared
 - OR
 - Waiting for the A/D interrupt
6. Read A/D Result register (ADRES), clear bit ADIF if required.
7. For next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2TAD is required before next acquisition starts.

FIGURE 8-3: A/D BLOCK DIAGRAM



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8.1 A/D Sampling Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 8-4. The source impedance (R_s) and the internal sampling switch (R_{ss}) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (R_{ss}) impedance varies over the device voltage (V_{DD}), see Figure 8-4. **The maximum recommended impedance for analog sources is 10 k Ω .** After the analog input channel is selected (changed) this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 8-1 may be used. This equation assumes that 1/2 LSB error is used (512 steps for the A/D). The 1/2 LSB error is the maximum error allowed for the A/D to meet its specified resolution.

EQUATION 8-1: A/D MINIMUM CHARGING TIME

$$V_{HOLD} = (V_{REF} - (V_{REF}/512)) \cdot (1 - e^{-(T_c/CHOLD)(R_{IC} + R_{SS} + R_s)})$$

or

$$T_c = -(51.2 \text{ pF})(1 \text{ k}\Omega + R_{SS} + R_s) \ln(1/511)$$

Example 8-1 shows the calculation of the minimum required acquisition time T_{ACQ} . This calculation is based on the following system assumptions.

$R_s = 10 \text{ k}\Omega$

1/2 LSB error

$V_{DD} = 5V \rightarrow R_{SS} = 7 \text{ k}\Omega$

Temp (system max.) = 50°C

$V_{HOLD} = 0 @ t = 0$

Note 1: The reference voltage (V_{REF}) has no effect on the equation, since it cancels itself out.

Note 2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

Note 3: The maximum recommended impedance for analog sources is 10 k Ω . This is required to meet the pin leakage specification.

Note 4: After a conversion has completed, a 2.0 TAD delay must complete before acquisition can begin again. During this time the holding capacitor is not connected to the selected A/D input channel.

EXAMPLE 8-1: CALCULATING THE MINIMUM REQUIRED SAMPLE TIME

$T_{ACQ} =$ Amplifier Settling Time +
Holding Capacitor Charging Time +
Temperature Coefficient

$$T_{ACQ} = 5 \mu s + T_c + [(Temp - 25^\circ C)(0.05 \mu s/^\circ C)]$$

$$T_c = -CHOLD (R_{IC} + R_{SS} + R_s) \ln(1/512)$$

$$-51.2 \text{ pF} (1 \text{ k}\Omega + 7 \text{ k}\Omega + 10 \text{ k}\Omega) \ln(0.0020)$$

$$-51.2 \text{ pF} (18 \text{ k}\Omega) \ln(0.0020)$$

$$-0.921 \mu s (-6.2146)$$

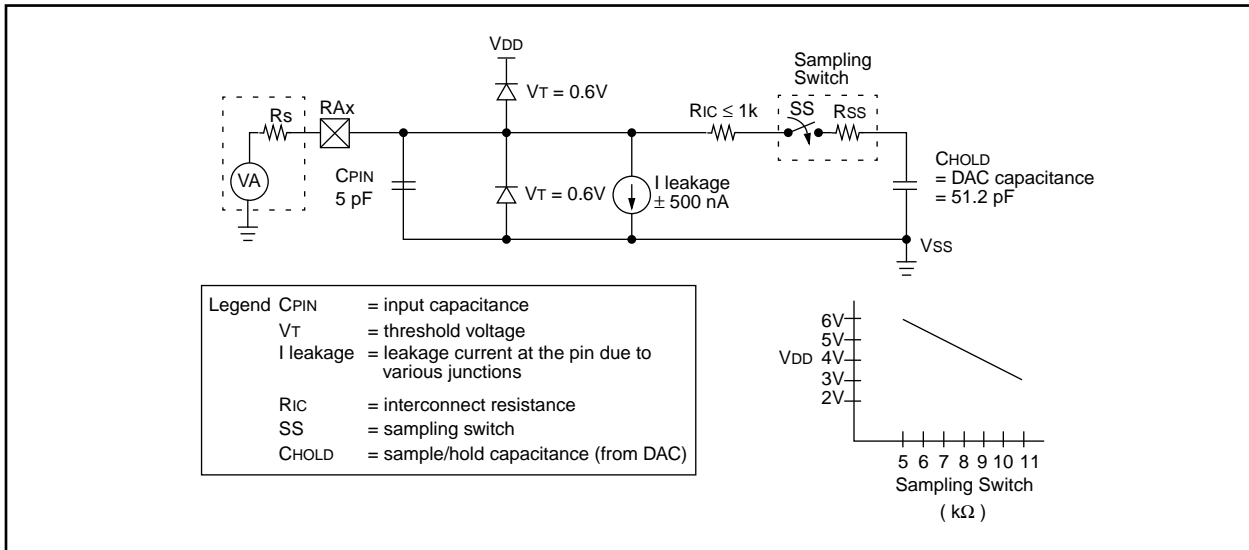
$$5.724 \mu s$$

$$T_{ACQ} = 5 \mu s + 5.724 \mu s + [(50^\circ C - 25^\circ C)(0.05 \mu s/^\circ C)]$$

$$10.724 \mu s + 1.25 \mu s$$

$$11.974 \mu s$$

FIGURE 8-4: ANALOG INPUT MODEL



8.2 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 9.5 TAD per 8-bit conversion. The source of the A/D conversion clock is software selected. The four possible options for TAD are:

- 2Tosc
- 8Tosc
- 32Tosc
- Internal ADC RC oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 μ s.

Table 8-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

8.3 Configuring Analog Port Pins

The ADCON1 and TRIS registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS2:CHS0 bits and the TRIS bits.

Note 1: When reading the port register, all pins configured as analog input channel will read as cleared (a low level). Pins configured as digital inputs, will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.

Note 2: Analog levels on any pin that is defined as a digital input (including the AN3:AN0 pins), may cause the input buffer to consume current that is out of the devices specification.

TABLE 8-1: TAD vs. DEVICE OPERATING FREQUENCIES

AD Clock Source (TAD)		Device Frequency		
Operation	ADCS1:ADCS0	4 MHz	1.25 MHz	333.33 kHz
2Tosc	00	500 ns ⁽²⁾	1.6 μ s	6 μ s
8Tosc	01	2.0 μ s	6.4 μ s	24 μ s ⁽³⁾
32Tosc	10	8.0 μ s	25.6 μ s ⁽³⁾	96 μ s ⁽³⁾
Internal ADC RC Oscillator ⁽⁵⁾	11	2 - 6 μ s ^(1,4)	2 - 6 μ s ^(1,4)	2 - 6 μ s ⁽¹⁾

Note 1: The RC source has a typical TAD time of 4 μ s.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

4: While in RC mode, with device frequency above 1 MHz, conversion accuracy is out of specification.

5: For extended voltage devices (LC), please refer to Electrical Specifications section.

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8.4 A/D Conversions

Example 8-2 show how to perform an A/D conversion. The GP pins are configured as analog inputs. The analog reference (VREF) is the device VDD. The A/D interrupt is enabled, and the A/D conversion clock is FRC. The conversion is performed on the GP0 channel.

Note: The GO/DONE bit should **NOT** be set in the same instruction that turns on the A/D.

Clearing the GO/DONE bit during a conversion will abort the current conversion. The ADRES register will NOT be updated with the partially completed A/D conversion sample. That is, the ADRES register will continue to contain the value of the last completed conversion (or the last value written to the ADRES register). After the A/D conversion is aborted, a 2TAD wait is required before the next acquisition is started. After this 2TAD wait, an acquisition is automatically started on the selected channel.

EXAMPLE 8-2: DOING AN A/D CONVERSION

```
BSF    STATUS, RP0        ; Select Page 1
CLRF   ADCON1             ; Configure A/D inputs
BSF    PIE1, ADIE         ; Enable A/D interrupts
BCF    STATUS, RP0        ; Select Page 0
MOVLW  0xC1               ; RC Clock, A/D is on, Channel 0 is selected
MOVWF  ADCON0             ;
BCF    PIR1, ADIF         ; Clear A/D interrupt flag bit
BSF    INTCON, PEIE       ; Enable peripheral interrupts
BSF    INTCON, GIE        ; Enable all interrupts
;
; Ensure that the required sampling time for the selected input channel has elapsed.
; Then the conversion may be started.
;
BSF    ADCON0, GO         ; Start A/D Conversion
:      ; The ADIF bit will be set and the GO/DONE bit
:      ; is cleared upon completion of the A/D Conversion.
```

8.5 A/D Operation During Sleep

The A/D module can operate during SLEEP mode. This requires that the A/D clock source be set to RC (ADCS1:ADCS0 = 11). When the RC clock source is selected, the A/D module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed, which eliminates all digital switching noise from the conversion. When the conversion is completed the GO/DONE bit will be cleared, and the result loaded into the ADRES register. If the A/D interrupt is enabled, the device will wake-up from SLEEP. If the A/D interrupt is not enabled, the A/D module will then be turned off, although the ADON bit will remain set.

When the A/D clock source is another clock option (not RC), a SLEEP instruction will cause the present conversion to be aborted and the A/D module to be turned off, though the ADON bit will remain set.

Turning off the A/D places the A/D module in its lowest current consumption state.

Note: For the A/D module to operate in SLEEP, the A/D clock source must be set to RC (ADCS1:ADCS0 = 11). To perform an A/D conversion in SLEEP, the GO/DONE bit must be set, followed by the SLEEP instruction.

8.6 A/D Accuracy/Error

The overall accuracy of the A/D is less than ± 1 LSB for $V_{DD} = 5V \pm 10\%$ and the analog $V_{REF} = V_{DD}$. This overall accuracy includes offset error, full scale error, and integral error. The A/D converter is guaranteed to be monotonic. The resolution and accuracy may be less when either the analog reference (V_{DD}) is less than 5.0V or when the analog reference (V_{REF}) is less than V_{DD} .

The maximum pin leakage current is $\pm 5 \mu A$.

In systems where the device frequency is low, use of the A/D RC clock is preferred. At moderate to high frequencies, T_{AD} should be derived from the device oscillator. T_{AD} must not violate the minimum and should be $\leq 8 \mu s$ for preferred operation. This is because T_{AD} , when derived from T_{OSC} , is kept away from on-chip phase clock transitions. This reduces, to a large extent, the effects of digital switching noise. This is not possible with the RC derived clock. The loss of accuracy due to digital switching noise can be significant if many I/O pins are active.

In systems where the device will enter SLEEP mode after the start of the A/D conversion, the RC clock source selection is required. In this mode, the digital noise from the modules in SLEEP are stopped. This method gives high accuracy.

8.7 Effects of a RESET

A device reset forces all registers to their reset state. This forces the A/D module to be turned off, and any conversion is aborted. The value that is in the ADRES register is not modified for a Reset. The ADRES register will contain unknown data after a Power-on Reset.

8.8 Connection Considerations

If the input voltage exceeds the rail values (V_{SS} or V_{DD}) by greater than 0.2V, then the accuracy of the conversion is out of specification.

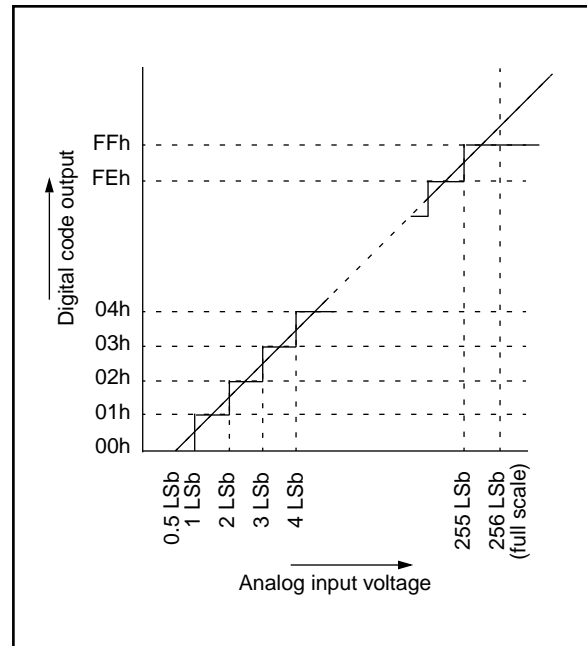
Note: For the PIC12CE67X, care must be taken when using the GP4 pin in A/D conversions due to its proximity to the OSC1 pin.

An external RC filter is sometimes added for anti-aliasing of the input signal. The R component should be selected to ensure that the total source impedance is kept under the 10 k Ω recommended specification. Any external components connected (via hi-impedance) to an analog input pin (capacitor, zener diode, etc.) should have very little leakage current at the pin.

8.9 Transfer Function

The ideal transfer function of the A/D converter is as follows: the first transition occurs when the analog input voltage (V_{AIN}) is 1 LSB (or Analog $V_{REF} / 256$) (Figure 8-5).

FIGURE 8-5: A/D TRANSFER FUNCTION



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FIGURE 8-6: FLOWCHART OF A/D OPERATION

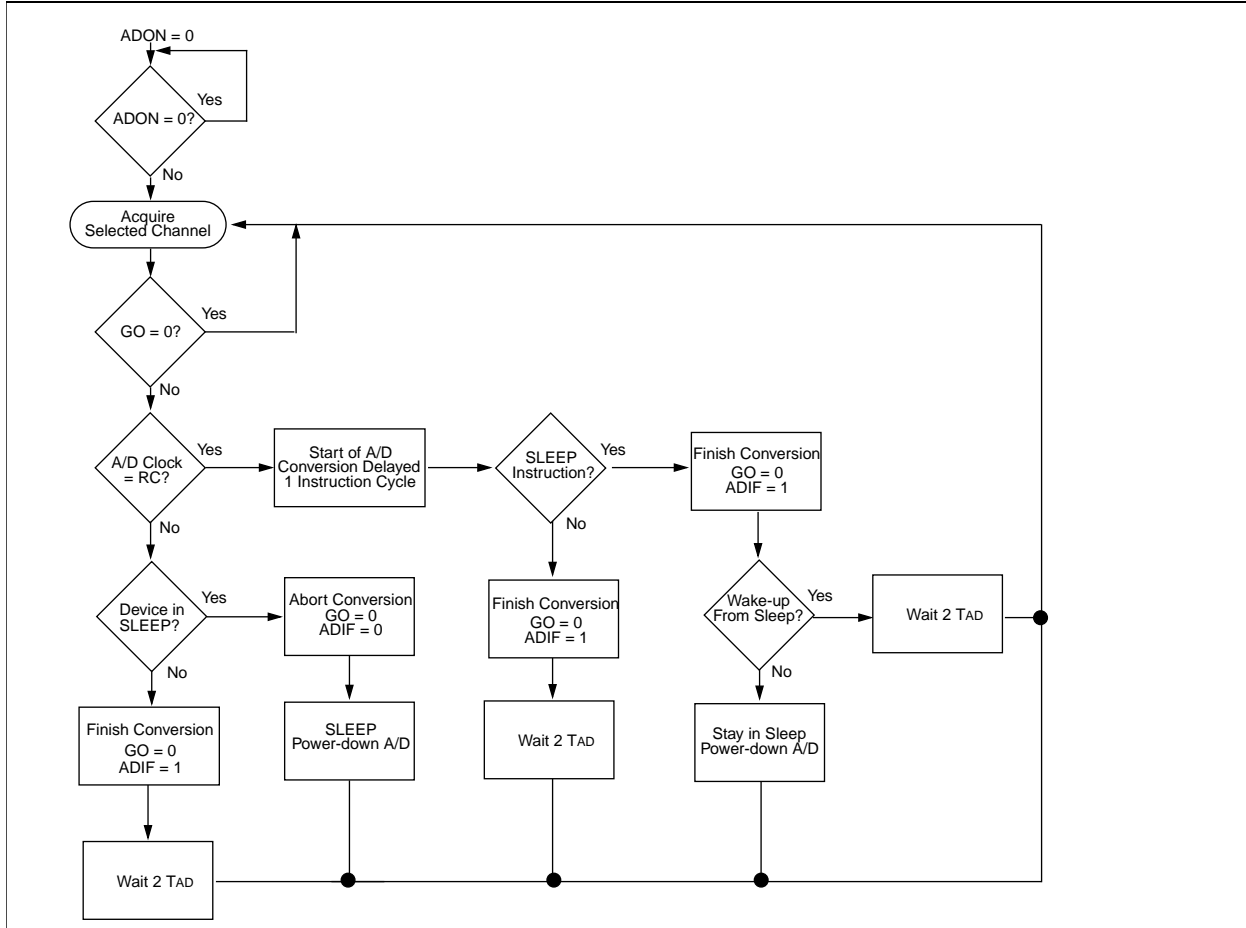


TABLE 8-2: SUMMARY OF A/D REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other Resets ⁽¹⁾
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	TOIF	INTF	GPIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF	—	—	—	—	—	—	-0-- ----	-0-- ----
8Ch	PIE1	—	ADIE	—	—	—	—	—	—	-0-- ----	-0-- ----
1Eh	ADRES	A/D Result Register								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	r	CHS1	CHS0	GO/DONE	r	ADON	0000 0000	0000 0000
9Fh	ADCON1	—	—	—	—	—	PCFG2	PCFG1	PCFG0	---- -000	---- -000
05h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	--xx xxxx	--uu uuuu
85h	TRIS	—	—	TRIS5	TRIS4	TRIS3	TRIS2	TRIS1	TRIS0	--11 1111	--11 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', r = reserved. Shaded cells are not used for A/D conversion.

Note 1: These registers can be addressed from either bank.

9.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real-time applications. The PIC12CE67X family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- Oscillator selection
- Reset
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID locations
- In-circuit serial programming

The PIC12CE67X has a Watchdog Timer which can be shut off only through configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep

the chip in reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in reset while the power supply stabilizes. With these two timers on-chip, most applications need no external reset circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external reset, Watchdog Timer Wake-up, or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The EXTRC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

9.1 Configuration Bits

The configuration bits can be programmed (read as '0') or left unprogrammed (read as '1') to select various device configurations. These bits are mapped in program memory location 2007h.

The user will note that address 2007h is beyond the user program memory space. In fact, it belongs to the special test/configuration memory space (2000h-3FFFh), which can be accessed only during programming.

FIGURE 9-1: CONFIGURATION WORD

CP1	CP0	CP1	CP0	CP1	CP0	MCLRE	CP1	CP0	PWRT \overline{E}	WDTE	FOSC2	FOSC1	FOSC0	Register: CONFIG
													Address 2007h	
													bit0	
bit13														
bit 13-8, CP1:CP0: Code Protection bit pairs ⁽¹⁾														
6-5: 11 = Code protection off														
10 = Locations 400h through 7FEh code protected (do not use for PIC12CE673)														
01 = Locations 200h through 7FEh code protected														
00 = All memory is code protected														
bit 7: MCLRE: Master Clear Reset Enable bit														
1 = Master Clear Enabled														
0 = Master Clear Disabled														
bit 4: PWRT\overline{E}: Power-up Timer Enable bit														
1 = PWRT disabled														
0 = PWRT enabled														
bit 3: WDTE: Watchdog Timer Enable bit														
1 = WDT enabled														
0 = WDT disabled														
bit 2-0: FOSC2:FOSC0: Oscillator Selection bits														
111 = EXTRC, Clockout on OSC2														
110 = EXTRC, OSC2 is I/O														
101 = INTRC, Clockout on OSC2														
100 = INTRC, OSC2 is I/O														
011 = Invalid Selection														
010 = HS Oscillator														
001 = XT Oscillator														
000 = LP Oscillator														
Note 1: All of the CP1:CP0 pairs have to be given the same value to enable the code protection scheme listed.														

PIC12CE67X

9.2 Oscillator Configurations

9.2.1 OSCILLATOR TYPES

The PIC12CE67X can be operated in seven different oscillator modes. The user can program three configuration bits (FOSC2:FOSC0) to select one of these seven modes:

- LP: Low Power Crystal
- HS: High Speed Crystal Resonator
- XT: Crystal/Resonator
- INTRC*: Internal 4 MHz Oscillator
- EXTRC*: External Resistor/Capacitor

*Can be configured to support CLKOUT

9.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, HS or LP modes, a crystal or ceramic resonator is connected to the GP5/OSC1/CLKIN and GP4/OSC2 pins to establish oscillation (Figure 9-2). The PIC12CE67X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, HS or LP modes, the device can have an external clock source drive the GP5/OSC1/CLKIN pin (Figure 9-3).

FIGURE 9-2: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (XT, HS OR LP OSC CONFIGURATION)

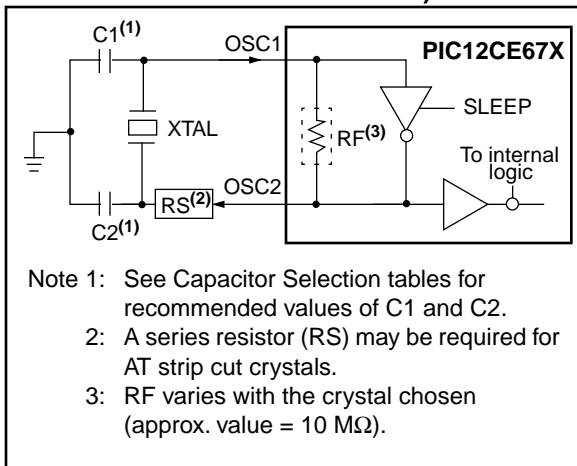


FIGURE 9-3: EXTERNAL CLOCK INPUT OPERATION (XT, HS OR LP OSC CONFIGURATION)

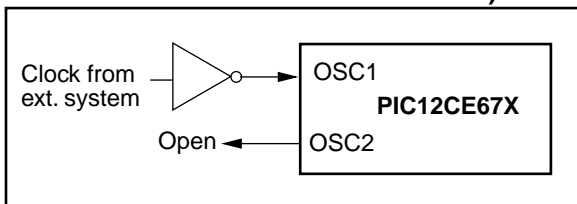


TABLE 9-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC12CE67X

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	455 kHz	22-100 pF	22-100 pF
	2.0 MHz	15-68 pF	15-68 pF
	4.0 MHz	15-68 pF	15-68 pF
HS	4.0 MHz	15-68 pF	15-68 pF
	8.0 MHz	10-68 pF	10-68 pF
	10.0 MHz	10-22 pF	10-22 pF

These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 9-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC12CE67X

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
LP	32 kHz ⁽¹⁾	15 pF	15 pF
	100 kHz	15-30 pF	30-47 pF
	200 kHz	15-30 pF	15-30 pF
XT	100 kHz	15-30 pF	200-300 pF
	200 kHz	15-30 pF	100-200 pF
	455 kHz	15-30 pF	15-100 pF
	1 MHz	15-30 pF	15-30 pF
	2 MHz	15-30 pF	15-30 pF
	4 MHz	15-47 pF	15-47 pF
HS	4 MHz	15-30 pF	15-30 pF
	8 MHz	15-30 pF	15-30 pF
	10 MHz	15-30 pF	15-30 pF

Note 1: For VDD > 4.5V, C1 = C2 ≈ 30 pF is recommended.

These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

9.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 9-4 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

FIGURE 9-4: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

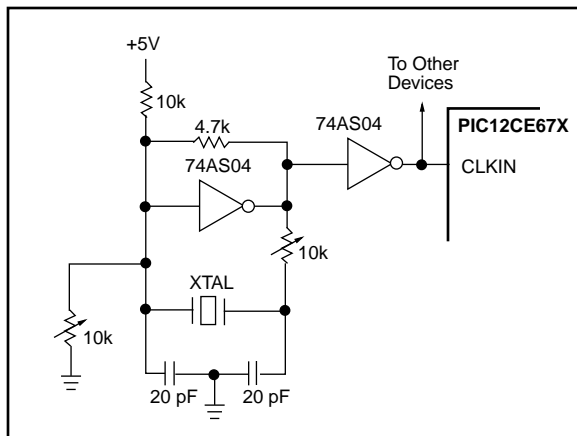
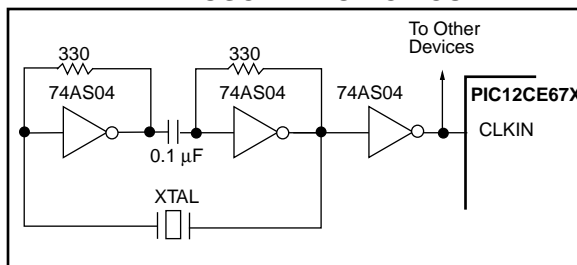


Figure 9-5 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 9-5: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



9.2.4 EXTERNAL RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (R_{ext}) and capacitor (C_{ext}) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low C_{ext} values. The user also needs to take into account variation due to tolerance of external R and C components used.

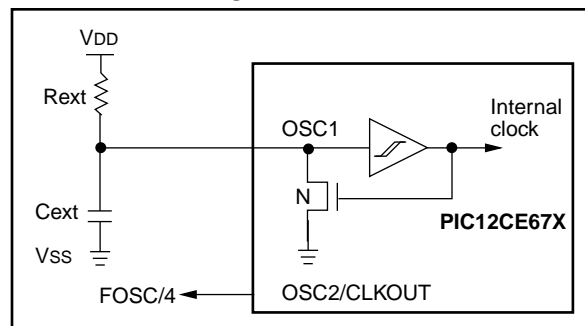
Figure 9-6 shows how the R/C combination is connected to the PIC12CE67X. For R_{ext} values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high R_{ext} values (e.g., 1 MΩ) the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping R_{ext} between 3 kΩ and 100 kΩ.

Although the oscillator will operate with no external capacitor ($C_{ext} = 0$ pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

The Electrical Specifications sections show RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

Also, see the Electrical Specifications sections for variation of oscillator frequency due to V_{DD} for given R_{ext}/C_{ext} values as well as frequency variation due to operating temperature for given R, C, and V_{DD} values.

FIGURE 9-6: EXTERNAL RC OSCILLATOR MODE



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9.2.5 INTERNAL 4 MHz RC OSCILLATOR

The internal RC oscillator provides a fixed 4 MHz (nominal) system clock at $V_{DD} = 5V$ and $25^{\circ}C$, see "Electrical Specifications" section for information on variation over voltage and temperature.

In addition, a calibration instruction is programmed into the last address of the program memory which contains the calibration value for the internal RC oscillator. This value is programmed as a `RETLW XX` instruction where XX is the calibration value. In order to retrieve the calibration value, issue a `CALL YY` instruction where YY is the last location in program memory (03FFh for the PIC12CE673, 07FFh for the PIC12CE674). Control will be returned to the user's program with the calibration value loaded into the W register. The program should then perform a `MOVWF OSCCAL` instruction to load the value into the internal RC oscillator trim register.

OSCCAL, when written to with the calibration value, will "trim" the internal oscillator to remove process variation from the oscillator frequency. Only bits <7:2> of OSCCAL are implemented, and bits <1:0> should be written as 0 for compatibility with future devices. The oscillator calibration location is not code protected.

<p>Note: Please note that erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be saved prior to erasing the part.</p>

9.2.6 CLKOUT

The PIC12CE67X can be configured to provide a clock out signal (CLKOUT) on pin 3 when the configuration word address (2007h) is programmed with FOSC2, FOSC1, FOSC0 equal to 101 for INTRC or 111 for EXTRC. The oscillator frequency, divided by 4 can be used for test purposes or to synchronize other logic.

9.3 Reset

The PIC12CE67X differentiates between various kinds of reset:

- Power-on Reset (POR)
- \overline{MCLR} reset during normal operation
- \overline{MCLR} reset during SLEEP
- WDT Reset (normal operation)

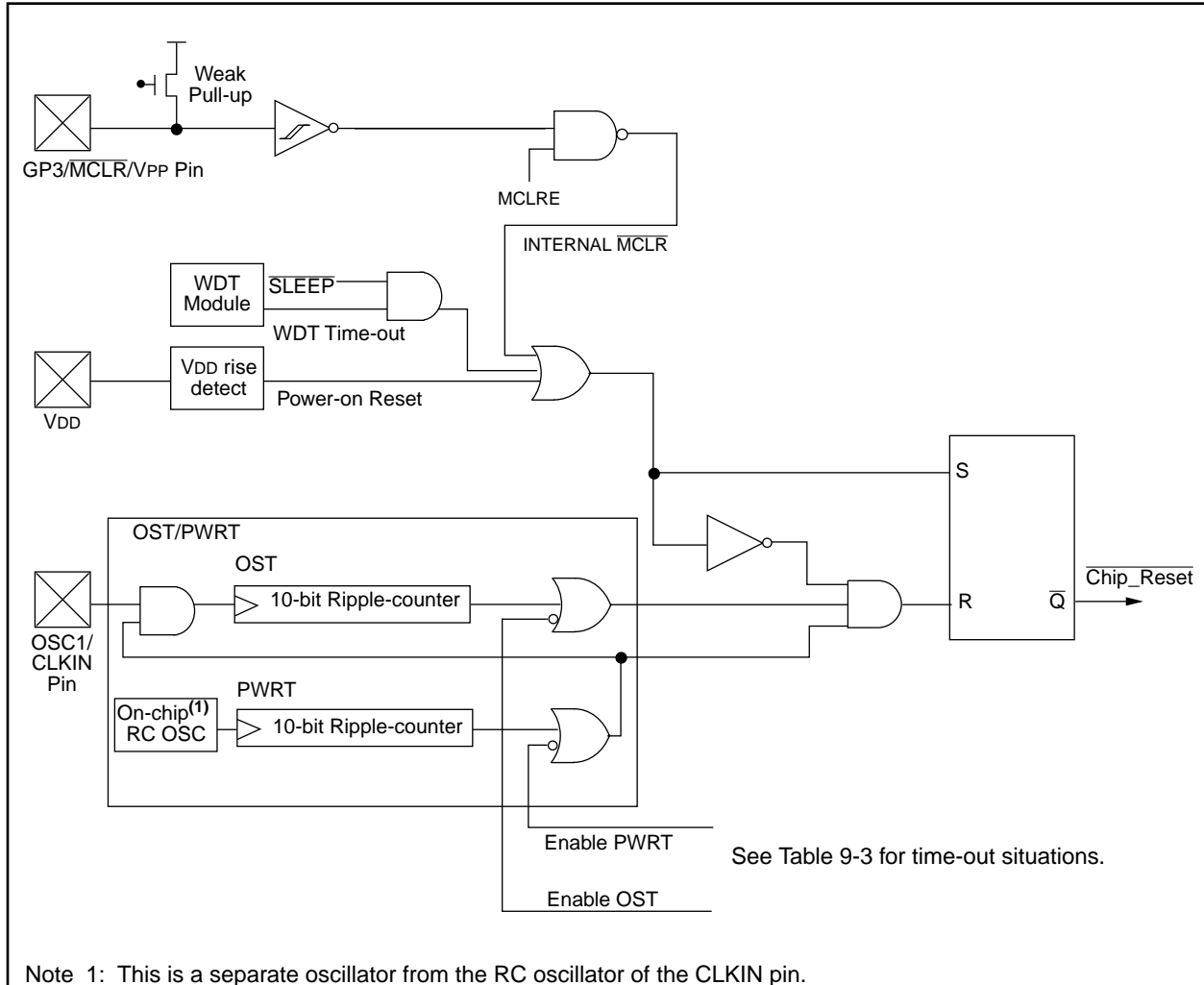
Some registers are not affected in any reset condition; their status is unknown on POR and unchanged in any other reset. Most other registers are reset to a "reset state" on Power-on Reset (POR), \overline{MCLR} Reset, WDT Reset, and \overline{MCLR} Reset during SLEEP. They are not affected by a WDT Wake-up, which is viewed as the resumption of normal operation. The \overline{TO} and \overline{PD} bits are set or cleared differently in different reset situations as indicated in Table 9-4. These bits are used in software to determine the nature of the reset. See Table 9-5 for a full description of reset states of all registers.

A simplified block diagram of the on-chip reset circuit is shown in Figure 9-7.

The PIC12CE67X has a \overline{MCLR} noise filter in the \overline{MCLR} reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive \overline{MCLR} pin low.

FIGURE 9-7: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



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9.4 Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)

9.4.1 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in reset until VDD has reached a high enough level for proper operation. To take advantage of the POR, just tie the MCLR pin through a resistor to VDD. This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See Electrical Specifications for details.

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, ...) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

For additional information, refer to Application Note AN607, "Power-up Trouble Shooting."

9.4.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms nominal time-out on power-up only, from the POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in reset as long as the PWRT is active. The PWRT's time delay allows VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT.

The power-up time delay will vary from chip to chip due to VDD, temperature, and process variation. See DC parameters for details.

9.4.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

9.4.4 TIME-OUT SEQUENCE

On power-up the time-out sequence is as follows: First PWRT time-out is invoked after the POR time delay has expired. Then OST is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there will be no time-out at all. Figure 9-8, Figure 9-9, and Figure 9-10 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, if \overline{MCLR} is kept low long enough, the time-outs will expire. Then bringing MCLR high will begin execution immediately (Figure 9-9). This is useful for testing purposes or to synchronize more than one PIC12CE67X device operating in parallel.

Table 9-5 shows the reset conditions for all the registers.

9.4.5 POWER CONTROL (PCON)/STATUS REGISTER

The power control/status register, PCON (address 8Eh) has one bit. See Figure 4-8 for register.

Bit1 is \overline{POR} (Power-on Reset). It is cleared on a Power-on Reset and is unaffected otherwise. The user set this bit following a Power-on Reset. On subsequent resets if POR is '0', it will indicate that a Power-on Reset must have occurred.

TABLE 9-3: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Wake-up from SLEEP
	$\overline{PWRT} = 0$	$\overline{PWRT} = 1$	
XT, HS, LP	72 ms + 1024TOSC	1024TOSC	1024TOSC
INTRC, EXTRC	72 ms	—	—

TABLE 9-4: STATUS/PCON BITS AND THEIR SIGNIFICANCE

POR	\overline{TO}	\overline{PD}	
0	1	1	Power-on Reset
0	0	x	Illegal, \overline{TO} is set on POR
0	x	0	Illegal, \overline{PD} is set on POR
1	0	u	WDT Reset
1	0	0	WDT Wake-up
1	u	u	\overline{MCLR} Reset during normal operation
1	1	0	\overline{MCLR} Reset during SLEEP or interrupt wake-up from SLEEP

TABLE 9-5: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- --0-
MCLR Reset during normal operation	000h	000u uuuu	---- --u-
MCLR Reset during SLEEP	000h	0001 0uuu	---- --u-
WDT Reset during normal operation	000h	0000 uuuu	---- --u-
WDT Wake-up from SLEEP	PC + 1	uuu0 0uuu	---- --u-
Interrupt wake-up from SLEEP	PC + 1 ⁽¹⁾	uuu1 0uuu	---- --u-

Legend: u = unchanged, x = unknown, - = unimplemented bit read as '0'.

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

TABLE 9-6: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Power-on Reset	MCLR Resets WDT Reset	Wake-up via WDT or Interrupt
W	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	0000 0000	0000 0000	0000 0000
TMR0	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	0000 0000	0000 0000	PC + 1 ⁽²⁾
STATUS	0001 1xxx	000q quuu ⁽³⁾	uuuq quuu ⁽³⁾
FSR	xxxx xxxx	uuuu uuuu	uuuu uuuu
GPIO	11xx xxxx	11uu uuuu	11uu uuuu
PCLATH	---0 0000	---0 0000	---u uuuu
INTCON	0000 000x	0000 000u	uuuu uqqq ⁽¹⁾
PIR1	-0-- ----	-0-- ----	-q-- ---- ⁽⁴⁾
ADCON0	0000 0000	0000 0000	uuuu uquu ⁽⁵⁾
OPTION	1111 1111	1111 1111	uuuu uuuu
TRIS	--11 1111	--11 1111	--uu uuuu
PIE1	-0-- ----	-0-- ----	-u-- ----
PCON	---- --0-	---- --u-	---- --u-
OSCCAL	1000 00--	uuuu uu--	uuuu uu--
ADCON1	---- -000	---- -000	---- -uuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON and PIR1 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 9-5 for reset value for specific condition.

4: If wake-up was due to A/D completing then bit 6 = 1, all other interrupts generating a wake-up will cause bit 6 = u.

5: If wake-up was due to A/D completing then bit 3 = 0, all other interrupts generating a wake-up will cause bit 3 = u.

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FIGURE 9-8: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 1

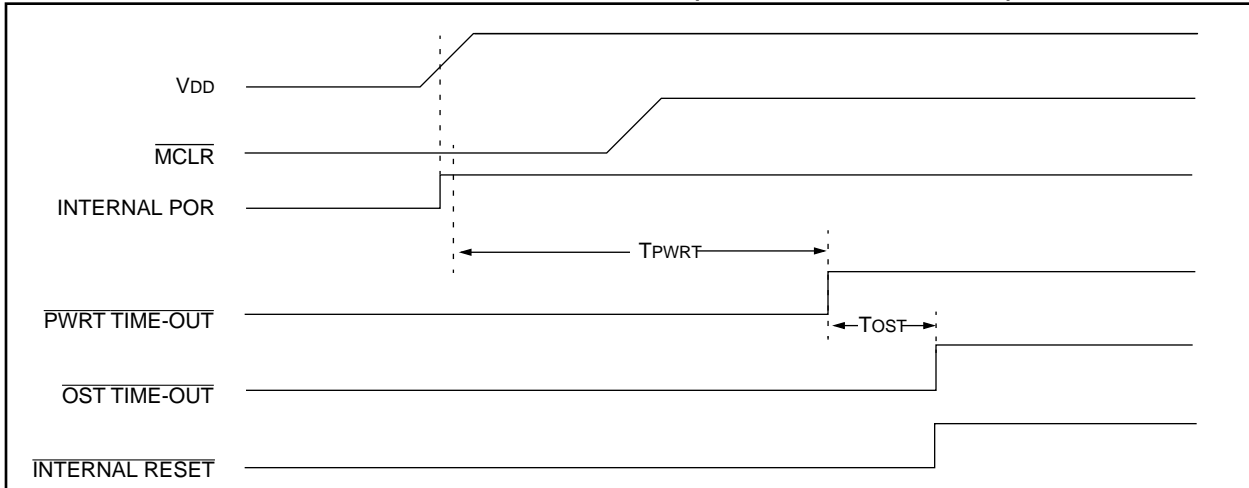


FIGURE 9-9: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 2

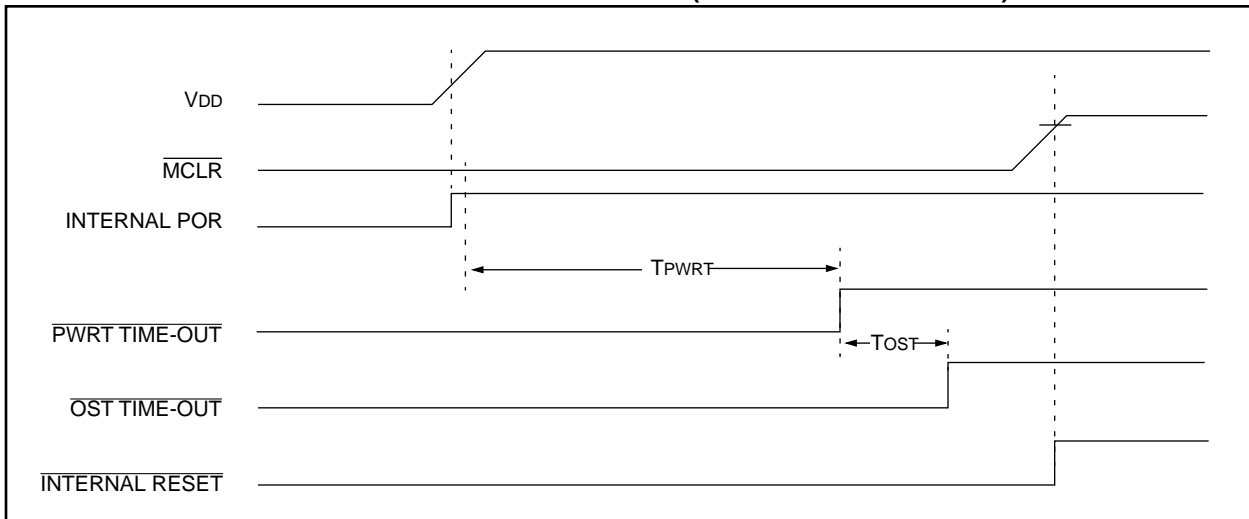


FIGURE 9-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD})

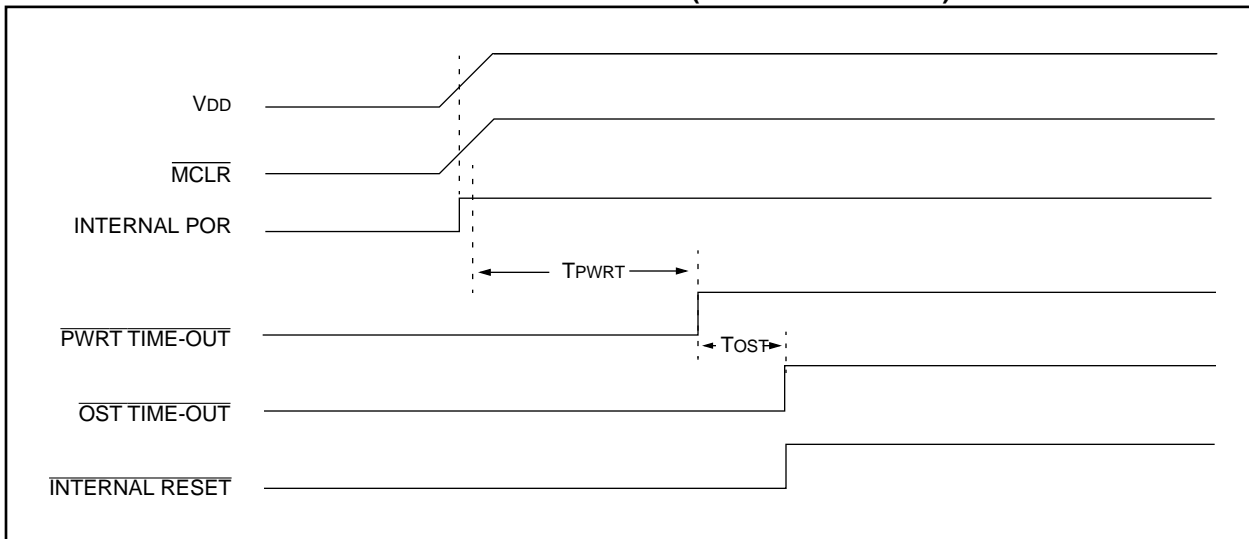


FIGURE 9-11: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)

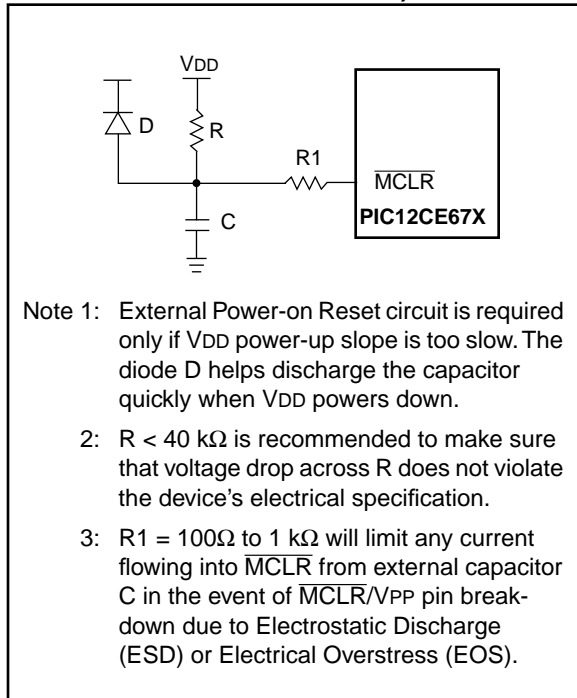


FIGURE 9-12: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1

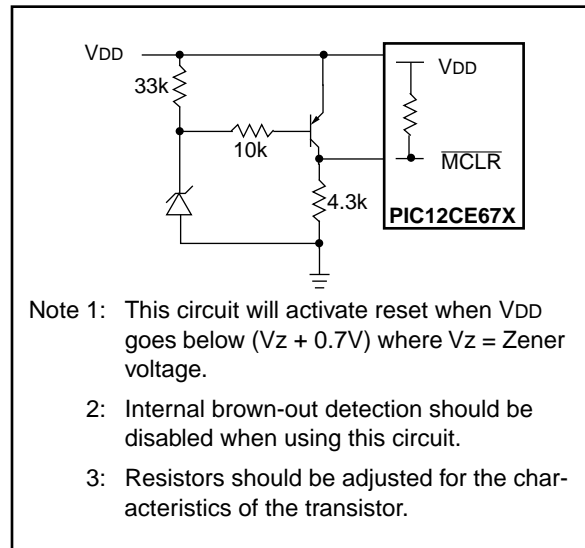
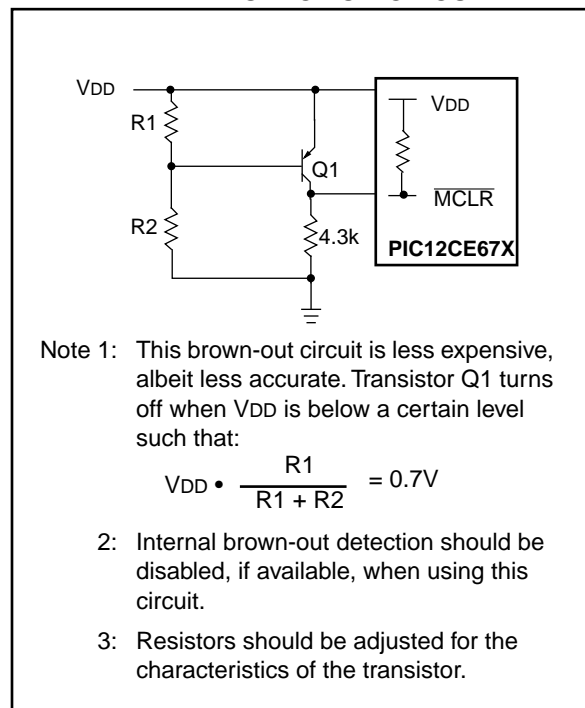


FIGURE 9-13: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



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9.5 Interrupts

There are four sources of interrupt:

Interrupt Sources
TMR0 overflow interrupt
External interrupt GP2/INT pin
GPIO Port change interrupts (pins GP0, GP1, GP3)
A/D Interrupt

The interrupt control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. When bit GIE is enabled, and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt bits are set regardless of the status of the GIE bit. The GIE bit is cleared on reset.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine as well as sets the GIE bit, which re-enables interrupts.

The GP2/INT, GPIO port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flag ADIF, is contained in the special function register PIR1. The corresponding interrupt enable bit is contained in special function register PIE1, and the peripheral interrupt enable bit is contained in special function register INTCON.

When an interrupt is responded to, the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the interrupt service routine the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as GPIO change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends when the interrupt event occurs (Figure 8-15). The latency is the same for one or two cycle instructions. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

FIGURE 9-14: INTERRUPT LOGIC

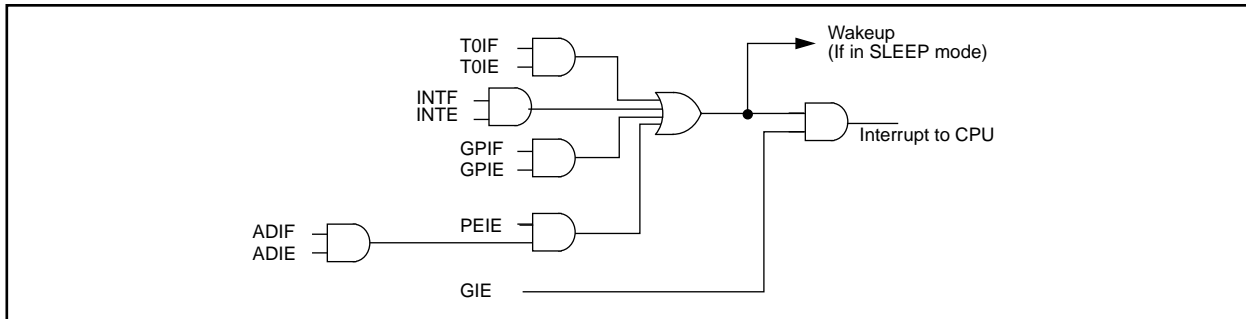
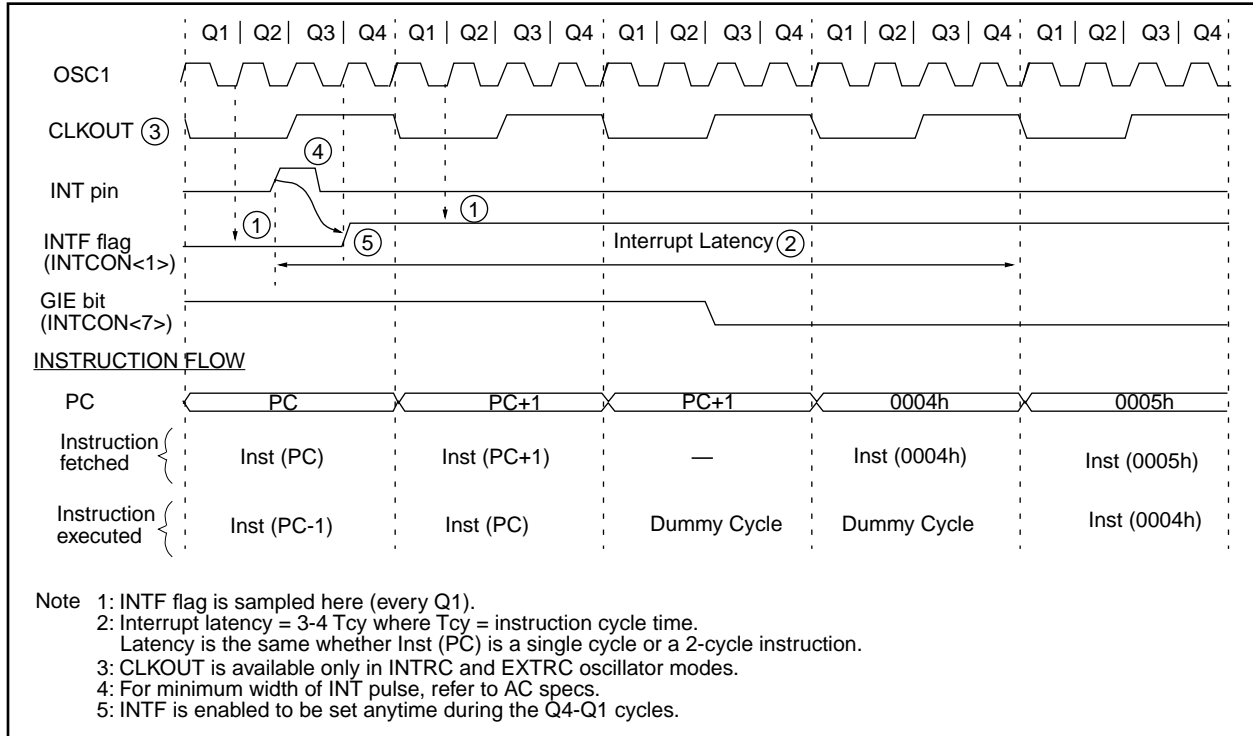


FIGURE 9-15: INT PIN INTERRUPT TIMING



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9.5.1 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register will set flag bit T0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit T0IE (INTCON<5>). (Section 7.0)

9.5.2 INT INTERRUPT

External interrupt on GP2/INT pin is edge triggered: either rising if bit INTEDG (OPTION<6>) is set, or falling, if the INTEDG bit is clear. When a valid edge appears on the GP2/INT pin, flag bit INTF (INTCON<1>) is set. This interrupt can be disabled by clearing enable bit INTE (INTCON<4>). Flag bit INTF must be cleared in software in the interrupt service routine before re-enabling this interrupt. The INT interrupt can wake-up the processor from SLEEP, if bit INTE was set prior to going into SLEEP. The status of global interrupt enable bit GIE decides whether or not the processor branches to the interrupt vector following wake-up. See Section 9.8 for details on SLEEP mode.

9.5.3 GPIO INTCON CHANGE

An input change on GP3, GP1 or GP0 sets flag bit GPIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit GPIE (INTCON<3>). (Section 5.1)

9.6 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt i.e., W register and STATUS register. This will have to be implemented in software.

Example 9-1 store and restore the STATUS and W registers. The register, W_TEMP, must be defined in both banks and must be defined at the same offset from the bank base address (i.e., if W_TEMP is defined at 0x20 in bank 0, it must also be defined at 0xA0 in bank 1).

The example:

- a) Stores the W register.
- b) Stores the STATUS register in bank 0.
- c) Executes the ISR code.
- d) Restores the STATUS register (and bank select bit).
- e) Restores the W register.

EXAMPLE 9-1: SAVING STATUS AND W REGISTERS IN RAM

```
MOVWF    W_TEMP           ;Copy W to TEMP register, could be bank one or zero
SWAPF    STATUS,W         ;Swap status to be saved into W
BCF      STATUS,RP0       ;Change to bank zero, regardless of current bank
MOVWF    STATUS_TEMP      ;Save status to bank zero STATUS_TEMP register
:
:(ISR)
:
SWAPF    STATUS_TEMP,W    ;Swap STATUS_TEMP register into W
                        ;(sets bank to original state)
MOVWF    STATUS           ;Move W into STATUS register
SWAPF    W_TEMP,F        ;Swap W_TEMP
SWAPF    W_TEMP,W        ;Swap W_TEMP into W
```


9.7 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run, even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins of the device has been stopped, for example, by execution of a `SLEEP` instruction. During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in `SLEEP` mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The WDT can be permanently disabled by clearing configuration bit `WDTE` (Section 9.1).

9.7.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, `VDD` and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the `OPTION` register. Thus, time-out periods up to 2.3 seconds can be realized.

The `CLRWDT` and `SLEEP` instructions clear the WDT and the postscaler, if assigned to the WDT, and prevent it from timing out early and generating a premature device `RESET` condition.

The `TO` bit in the `STATUS` register will be cleared upon a Watchdog Timer time-out.

9.7.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken into account that under worst case conditions (`VDD` = Min., Temperature = Max., and max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

Note: When the prescaler is assigned to the WDT, always execute a `CLRWDT` instruction before changing the prescale value, otherwise a WDT reset may occur.

FIGURE 9-16: WATCHDOG TIMER BLOCK DIAGRAM

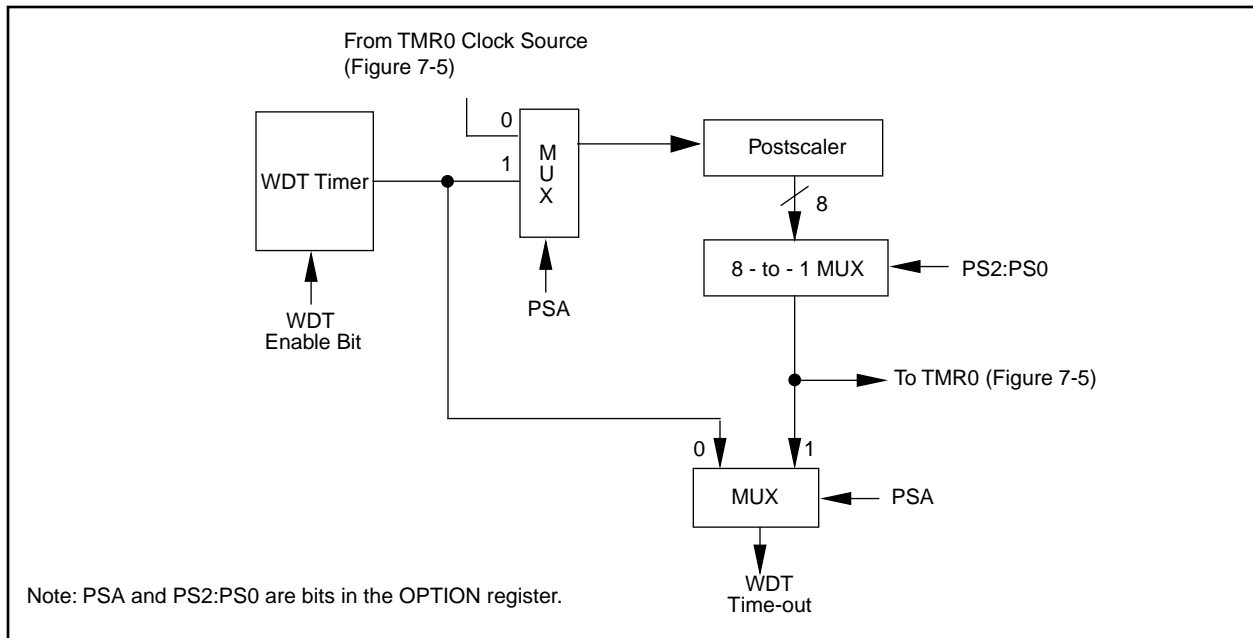


FIGURE 9-17: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits ⁽¹⁾	MCLRE	CP1	CP0	PWRTE	WDTE	FOSC2	FOSC1	FOSC0
81h	OPTION	GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Figure 9-1 for operation of these bits. Not all `CP0` and `CP1` bits are shown.

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9.8 Power-down Mode (SLEEP)

Power-down mode is entered by executing a `SLEEP` instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the \overline{PD} bit (`STATUS<3>`) is cleared, the \overline{TO} (`STATUS<4>`) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the `SLEEP` instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either V_{DD} , or V_{SS} , ensure no external circuitry is drawing current from the I/O pin, power-down the A/D, disable external clocks. Pull all I/O pins, that are hi-impedance inputs, high or low externally to avoid switching currents caused by floating inputs. The `T0CKI` input if enabled should also be at V_{DD} or V_{SS} for lowest current consumption. The contribution from on-chip pull-ups on GPIO should be considered.

The \overline{MCLR} pin if enabled must be at a logic high level (V_{IHMC}).

9.8.1 WAKE-UP FROM SLEEP

The device can wake up from `SLEEP` through one of the following events:

1. External reset input on \overline{MCLR} pin.
2. Watchdog Timer Wake-up (if `WDT` was enabled).
3. `GP2/INT` interrupt, interrupt GPIO port change, or some Peripheral Interrupts.

External \overline{MCLR} Reset will cause a device reset. All other events are considered a continuation of program execution and cause a "wake-up". The \overline{TO} and \overline{PD} bits in the `STATUS` register can be used to determine the cause of device reset. The \overline{PD} bit, which is set on power-up, is cleared when `SLEEP` is invoked. The \overline{TO} bit is cleared if a `WDT` time-out occurred (and caused wake-up).

The following peripheral interrupt can wake the device from `SLEEP`:

1. A/D conversion (when A/D clock source is RC).

Other peripherals can not generate interrupts since during `SLEEP`, no on-chip Q clocks are present.

When the `SLEEP` instruction is being executed, the next instruction (`PC + 1`) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the `GIE` bit. If the `GIE` bit is clear (disabled), the device continues execution at the instruction after the `SLEEP` instruction. If the `GIE` bit is set (enabled), the device executes the instruction after the `SLEEP` instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following `SLEEP` is not desirable, the user should have a `NOP` after the `SLEEP` instruction.

9.8.2 WAKE-UP USING INTERRUPTS

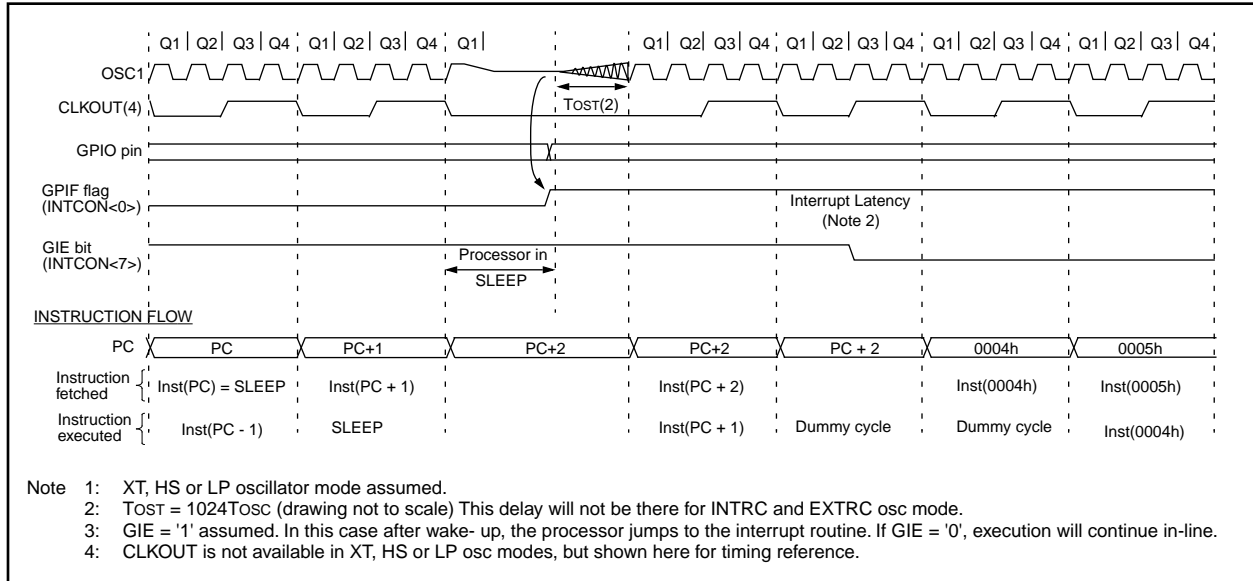
When global interrupts are disabled (`GIE` cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

- If the interrupt occurs **before** the the execution of a `SLEEP` instruction, the `SLEEP` instruction will complete as a `NOP`. Therefore, the `WDT` and `WDT` postscaler will not be cleared, the \overline{TO} bit will not be set and \overline{PD} bits will not be cleared.
- If the interrupt occurs **during or after** the execution of a `SLEEP` instruction, the device will immediately wake up from sleep . The `SLEEP` instruction will be completely executed before the wake-up. Therefore, the `WDT` and `WDT` postscaler will be cleared, the \overline{TO} bit will be set and the \overline{PD} bit will be cleared.

Even if the flag bits were checked before executing a `SLEEP` instruction, it may be possible for flag bits to become set before the `SLEEP` instruction completes. To determine whether a `SLEEP` instruction executed, test the \overline{PD} bit. If the \overline{PD} bit is set, the `SLEEP` instruction was executed as a `NOP`.

To ensure that the `WDT` is cleared, a `CLRWDT` instruction should be executed before a `SLEEP` instruction.

FIGURE 9-18: WAKE-UP FROM SLEEP THROUGH INTERRUPT



9.9 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting windowed devices.

9.10 ID Locations

Four memory locations (2000h - 2003h) are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify. It is recommended that only the 4 least significant bits of the ID location are used.

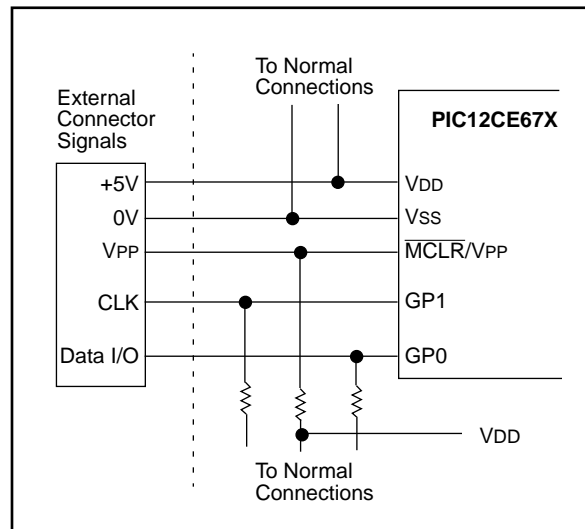
9.11 In-Circuit Serial Programming

PIC12CE67X microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground, and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a program/verify mode by holding the GP1 and GP0 pins low while raising the MCLR (VPP) pin from V_{IL} to V_{IH} (see programming specification). GP1 (clock) becomes the programming clock and GP0 (data) becomes the programming data. Both GP0 and GP1 are Schmitt Trigger inputs in this mode.

After reset, to place the device into programming/verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC12CE67X Programming Specifications.

FIGURE 9-19: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



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NOTES:

10.0 INSTRUCTION SET SUMMARY

Each PIC12CE67X instruction is a 14-bit word divided into an OPCODE which specifies the instruction type and one or more operands which further specify the operation of the instruction. The PIC12CE67X instruction set summary in Table 10-2 lists **byte-oriented**, **bit-oriented**, and **literal and control** operations. Table 10-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven bit constant or literal value.

TABLE 10-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
w	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
PCLATH	Program Counter High Latch
GIE	Global Interrupt Enable bit
WDT	Watchdog Timer/Counter
T \bar{O}	Time-out bit
P \bar{D}	Power-down bit
dest	Destination either the W register or the specified register file location
[]	Options
()	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
<i>italics</i>	User defined term (font is courier)

The instruction set is highly orthogonal and is grouped into three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles with the second cycle executed as a NOP. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Table 10-2 lists the instructions recognized by the MPASM assembler.

Figure 10-1 shows the three general formats that the instructions can have.

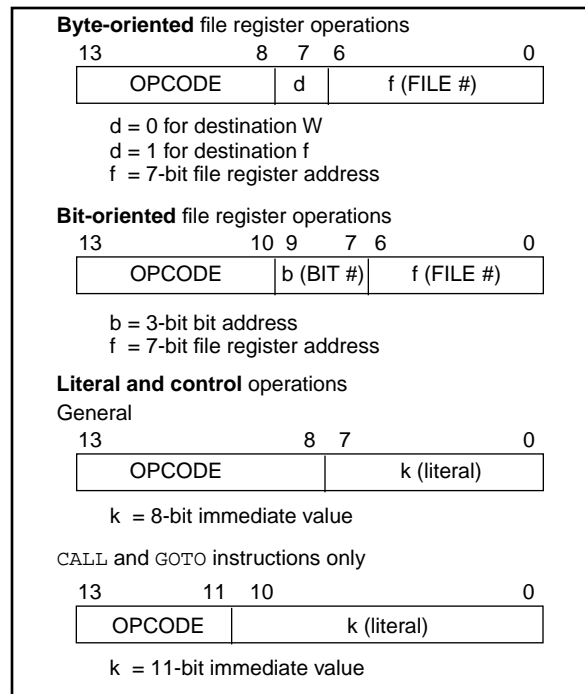
Note: To maintain upward compatibility with future PIC12CE67X products, do not use the `OPTION` and `TRIS` instructions.

All examples use the following format to represent a hexadecimal number:

0xhh

where h signifies a hexadecimal digit.

FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS



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10.1 Special Function Registers as Source/Destination

The PIC12CE67X's orthogonal instruction set allows read and write of all file registers, including special function registers. There are some special situations the user should be aware of:

10.1.1 STATUS AS DESTINATION

If an instruction writes to STATUS, the Z, C and DC bits may be set or cleared as a result of the instruction and overwrite the original data bits written. For example, executing `CLRF STATUS` will clear register STATUS, and then set the Z bit leaving `0000 0100b` in the register.

10.1.2 TRIS AS DESTINATION

Bit 3 of the TRIS register always reads as a '1' since GP3 is an input only pin. This fact can affect some read-modify-write operations on the TRIS register.

10.1.3 PCL AS SOURCE OR DESTINATION

Read, write or read-modify-write on PCL may have the following results:

Read PC: PCL → dest
Write PCL: PCLATH → PCH;
8-bit destination value → PCL
Read-Modify-Write: PCL → ALU operand
PCLATH → PCH;
8-bit result → PCL

Where PCH = program counter high byte (not an addressable register), PCLATH = Program counter high holding latch, dest = destination, WREG or f.

10.1.4 BIT MANIPULATION

All bit manipulation instructions are done by first reading the entire register, operating on the selected bit and writing the result back (read-modify-write). The user should keep this in mind when operating on special function registers, such as ports.

TABLE 10-2: INSTRUCTION SET SUMMARY

Mnemonic, Operands	Description	Cycles	14-Bit Opcode			Status Affected	Notes
			MSb	LSb			
BYTE-ORIENTED FILE REGISTER OPERATIONS							
ADDWF f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z 1,2
ANDWF f, d	AND W with f	1	00	0101	dfff	ffff	Z 1,2
CLRF f	Clear f	1	00	0001	1fff	ffff	Z 2
CLRWF -	Clear W	1	00	0001	0000	0011	Z
COMF f, d	Complement f	1	00	1001	dfff	ffff	Z 1,2
DECF f, d	Decrement f	1	00	0011	dfff	ffff	Z 1,2
DECFSZ f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff	1,2,3
INCF f, d	Increment f	1	00	1010	dfff	ffff	Z 1,2
INCFSZ f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff	1,2,3
IORWF f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z 1,2
MOVF f, d	Move f	1	00	1000	dfff	ffff	Z 1,2
MOVWF f	Move W to f	1	00	0000	1fff	ffff	
NOP -	No Operation	1	00	0000	0xx0	0000	
RLF f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C 1,2
RRF f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C 1,2
SUBWF f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z 1,2
SWAPF f, d	Swap nibbles in f	1	00	1110	dfff	ffff	1,2
XORWF f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z 1,2
BIT-ORIENTED FILE REGISTER OPERATIONS							
BCF f, b	Bit Clear f	1	01	00bb	bfff	ffff	1,2
BSF f, b	Bit Set f	1	01	01bb	bfff	ffff	1,2
BTFSC f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff	3
BTFSS f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff	3
LITERAL AND CONTROL OPERATIONS							
ADDLW k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z
ANDLW k	AND literal with W	1	11	1001	kkkk	kkkk	Z
CALL k	Call subroutine	2	10	0kkk	kkkk	kkkk	
CLRWDT -	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}, \overline{PD}$
GOTO k	Go to address	2	10	1kkk	kkkk	kkkk	
IORLW k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z
MOVLW k	Move literal to W	1	11	00xx	kkkk	kkkk	
RETFIE -	Return from interrupt	2	00	0000	0000	1001	
RETLW k	Return with literal in W	2	11	01xx	kkkk	kkkk	
RETURN -	Return from Subroutine	2	00	0000	0000	1000	
SLEEP -	Go into standby mode	1	00	0000	0110	0011	$\overline{TO}, \overline{PD}$
SUBLW k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z
XORLW k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z

- Note 1: When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- 2: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 Module.
- 3: If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

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10.2 Instruction Descriptions

ADDLW Add Literal and W

Syntax:	[<i>label</i>] ADDLW k				
Operands:	$0 \leq k \leq 255$				
Operation:	$(W) + k \rightarrow (W)$				
Status Affected:	C, DC, Z				
Encoding:	<table border="1"><tr><td>11</td><td>111x</td><td>kkkk</td><td>kkkk</td></tr></table>	11	111x	kkkk	kkkk
11	111x	kkkk	kkkk		
Description:	The contents of the W register are added to the eight bit literal 'k' and the result is placed in the W register.				
Words:	1				
Cycles:	1				
Example	<pre>ADDLW 0x15</pre> <p>Before Instruction W = 0x10</p> <p>After Instruction W = 0x25</p>				

ADDWF Add W and f

Syntax:	[<i>label</i>] ADDWF f,d				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	$(W) + (f) \rightarrow (dest)$				
Status Affected:	C, DC, Z				
Encoding:	<table border="1"><tr><td>00</td><td>0111</td><td>dfff</td><td>ffff</td></tr></table>	00	0111	dfff	ffff
00	0111	dfff	ffff		
Description:	Add the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example	<pre>ADDWF FSR, 0</pre> <p>Before Instruction W = 0x17 FSR = 0xC2</p> <p>After Instruction W = 0xD9 FSR = 0xC2</p>				

ANDLW And Literal with W

Syntax:	[<i>label</i>] ANDLW k				
Operands:	$0 \leq k \leq 255$				
Operation:	$(W) .AND. (k) \rightarrow (W)$				
Status Affected:	Z				
Encoding:	<table border="1"><tr><td>11</td><td>1001</td><td>kkkk</td><td>kkkk</td></tr></table>	11	1001	kkkk	kkkk
11	1001	kkkk	kkkk		
Description:	The contents of W register are AND'ed with the eight bit literal 'k'. The result is placed in the W register.				
Words:	1				
Cycles:	1				
Example	<pre>ANDLW 0x5F</pre> <p>Before Instruction W = 0xA3</p> <p>After Instruction W = 0x03</p>				

ANDWF AND W with f

Syntax:	[<i>label</i>] ANDWF f,d				
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$				
Operation:	$(W) .AND. (f) \rightarrow (dest)$				
Status Affected:	Z				
Encoding:	<table border="1"><tr><td>00</td><td>0101</td><td>dfff</td><td>ffff</td></tr></table>	00	0101	dfff	ffff
00	0101	dfff	ffff		
Description:	AND the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example	<pre>ANDWF FSR, 1</pre> <p>Before Instruction W = 0x17 FSR = 0xC2</p> <p>After Instruction W = 0x17 FSR = 0x02</p>				

BCF **Bit Clear f**

Syntax: [*label*] BCF f,b

Operands: $0 \leq f \leq 127$
 $0 \leq b \leq 7$

Operation: $0 \rightarrow (f)$

Status Affected: None

Encoding:

01	00bb	bfff	ffff
----	------	------	------

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example

```

BCF        FLAG_REG, 7

Before Instruction
FLAG_REG = 0xC7
After Instruction
FLAG_REG = 0x47
    
```

BTFSC **Bit Test, Skip if Clear**

Syntax: [*label*] BTFSC f,b

Operands: $0 \leq f \leq 127$
 $0 \leq b \leq 7$

Operation: skip if (f) = 0

Status Affected: None

Encoding:

01	10bb	bfff	ffff
----	------	------	------

Description: If bit 'b' in register 'f' is '0' then the next instruction is skipped.
If bit 'b' is '0' then the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a 2 cycle instruction.

Words: 1

Cycles: 1(2)

Example

```

HERE    BTFSC   FLAG, 1
FALSE   GOTO    PROCESS_CODE
TRUE     .
         .
         .
    
```

```

Before Instruction
PC =    address   HERE
After Instruction
if FLAG<1> = 0,
PC =    address   TRUE
if FLAG<1> = 1,
PC =    address   FALSE
    
```

BSF **Bit Set f**

Syntax: [*label*] BSF f,b

Operands: $0 \leq f \leq 127$
 $0 \leq b \leq 7$

Operation: $1 \rightarrow (f)$

Status Affected: None

Encoding:

01	01bb	bfff	ffff
----	------	------	------

Description: Bit 'b' in register 'f' is set.

Words: 1

Cycles: 1

Example

```

BSF        FLAG_REG, 7

Before Instruction
FLAG_REG = 0x0A
After Instruction
FLAG_REG = 0x8A
    
```

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BTFSS	Bit Test f, Skip if Set				
Syntax:	[<i>label</i>] BTFSS f,b				
Operands:	0 ≤ f ≤ 127 0 ≤ b < 7				
Operation:	skip if (f) = 1				
Status Affected:	None				
Encoding:	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="padding: 2px 10px;">01</td> <td style="padding: 2px 10px;">11bb</td> <td style="padding: 2px 10px;">bfff</td> <td style="padding: 2px 10px;">ffff</td> </tr> </table>	01	11bb	bfff	ffff
01	11bb	bfff	ffff		
Description:	If bit 'b' in register 'f' is '1' then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a 2 cycle instruction.				
Words:	1				
Cycles:	1(2)				
Example	<pre> HERE BTFSS FLAG,1 FALSE GOTO PROCESS_CODE TRUE . . . </pre> <p>Before Instruction PC = address HERE</p> <p>After Instruction if FLAG<1> = 0, PC = address FALSE if FLAG<1> = 1, PC = address TRUE</p>				

CALL	Call Subroutine				
Syntax:	[<i>label</i>] CALL k				
Operands:	0 ≤ k ≤ 2047				
Operation:	(PC)+ 1 → TOS, k → PC<10:0>, (PCLATH<4:3>) → PC<12:11>				
Status Affected:	None				
Encoding:	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="padding: 2px 10px;">10</td> <td style="padding: 2px 10px;">0kkk</td> <td style="padding: 2px 10px;">kkkk</td> <td style="padding: 2px 10px;">kkkk</td> </tr> </table>	10	0kkk	kkkk	kkkk
10	0kkk	kkkk	kkkk		
Description:	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two cycle instruction.				
Words:	1				
Cycles:	2				
Example	<pre> HERE CALL THERE </pre> <p>Before Instruction PC = Address HERE</p> <p>After Instruction PC = Address THERE TOS = Address HERE+1</p>				

CLRF	Clear f				
Syntax:	[<i>label</i>] CLRF f				
Operands:	0 ≤ f ≤ 127				
Operation:	00h → (f) 1 → Z				
Status Affected:	Z				
Encoding:	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="padding: 2px 10px;">00</td> <td style="padding: 2px 10px;">0001</td> <td style="padding: 2px 10px;">1fff</td> <td style="padding: 2px 10px;">ffff</td> </tr> </table>	00	0001	1fff	ffff
00	0001	1fff	ffff		
Description:	The contents of register 'f' are cleared and the Z bit is set.				
Words:	1				
Cycles:	1				
Example	<pre> CLRF FLAG_REG </pre> <p>Before Instruction FLAG_REG = 0x5A</p> <p>After Instruction FLAG_REG = 0x00 Z = 1</p>				

CLRW	Clear W				
Syntax:	[<i>label</i>] CLRW				
Operands:	None				
Operation:	00h → (W) 1 → Z				
Status Affected:	Z				
Encoding:	<table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="padding: 2px 10px;">00</td> <td style="padding: 2px 10px;">0001</td> <td style="padding: 2px 10px;">0000</td> <td style="padding: 2px 10px;">0011</td> </tr> </table>	00	0001	0000	0011
00	0001	0000	0011		
Description:	W register is cleared. Zero bit (Z) is set.				
Words:	1				
Cycles:	1				
Example	<pre> CLRW </pre> <p>Before Instruction W = 0x5A</p> <p>After Instruction W = 0x00 Z = 1</p>				

CLRWDT **Clear Watchdog Timer**

Syntax: [*label*] CLRWDT

Operands: None

Operation: 00h → WDT
 0 → WDT prescaler,
 1 → \overline{TO}
 1 → \overline{PD}

Status Affected: \overline{TO} , \overline{PD}

Encoding:

00	0000	0110	0100
----	------	------	------

Description: CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits \overline{TO} and \overline{PD} are set.

Words: 1

Cycles: 1

Example CLRWDT

Before Instruction
 WDT counter = ?

After Instruction
 WDT counter = 0x00
 WDT prescaler = 0
 \overline{TO} = 1
 \overline{PD} = 1

DECf **Decrement f**

Syntax: [*label*] DECf f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: (f) - 1 → (dest)

Status Affected: Z

Encoding:

00	0011	dfff	ffff
----	------	------	------

Description: Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example DECf CNT, 1

Before Instruction
 CNT = 0x01
 Z = 0

After Instruction
 CNT = 0x00
 Z = 1

COMF **Complement f**

Syntax: [*label*] COMf f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: (\bar{f}) → (dest)

Status Affected: Z

Encoding:

00	1001	dfff	ffff
----	------	------	------

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in W. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example COMf REG1, 0

Before Instruction
 REG1 = 0x13

After Instruction
 REG1 = 0x13
 W = 0xEC

DECFSZ **Decrement f, Skip if 0**

Syntax: [*label*] DECFSZ f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: (f) - 1 → (dest); skip if result = 0

Status Affected: None

Encoding:

00	1011	dfff	ffff
----	------	------	------

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1(2)

Example HERE DECFSZ CNT, 1
 GOTO LOOP
 CONTINUE •
 •
 •

Before Instruction
 PC = address HERE

After Instruction
 CNT = CNT - 1
 if CNT = 0,
 PC = address CONTINUE
 if CNT ≠ 0,
 PC = address HERE+1

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GOTO **Unconditional Branch**

Syntax: [*label*] GOTO *k*

Operands: $0 \leq k \leq 2047$

Operation: $k \rightarrow PC<10:0>$
 $PCLATH<4:3> \rightarrow PC<12:11>$

Status Affected: None

Encoding:

10	1kkk	kkkk	kkkk
----	------	------	------

Description: GOTO is an unconditional branch. The eleven bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two cycle instruction.

Words: 1

Cycles: 2

Example GOTO THERE

 After Instruction
 PC = Address THERE

INCFSZ **Increment f, Skip if 0**

Syntax: [*label*] INCFSZ *f,d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (dest)$, skip if result = 0

Status Affected: None

Encoding:

00	1111	dfff	ffff
----	------	------	------

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'. If the result is 0, the next instruction, which is already fetched, is discarded. A NOP is executed instead making it a two cycle instruction.

Words: 1

Cycles: 1(2)

Example HERE INCFSZ CNT, 1
 GOTO LOOP
 CONTINUE •
 •
 •

Before Instruction
 PC = address HERE

After Instruction
 CNT = CNT + 1
 if CNT= 0,
 PC = address CONTINUE
 if CNT≠ 0,
 PC = address HERE +1

INCF **Increment f**

Syntax: [*label*] INCF *f,d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (dest)$

Status Affected: Z

Encoding:

00	1010	dfff	ffff
----	------	------	------

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example INCF CNT, 1

 Before Instruction
 CNT = 0xFF
 Z = 0

 After Instruction
 CNT = 0x00
 Z = 1

IORLW **Inclusive OR Literal with W**

Syntax: [*label*] IORLW *k*

Operands: $0 \leq k \leq 255$

Operation: $(W) .OR. k \rightarrow (W)$

Status Affected: Z

Encoding:

11	1000	kkkk	kkkk
----	------	------	------

Description: The contents of the W register is OR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example IORLW 0x35

Before Instruction
 W = 0x9A

After Instruction
 W = 0xBF
 Z = 1

IORWF **Inclusive OR W with f**

Syntax: [*label*] IORWF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: (W) .OR. (f) → (dest)

Status Affected: Z

Encoding:

00	0100	dfff	ffff
----	------	------	------

Description: Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example IORWF RESULT, 0

Before Instruction

RESULT = 0x13

W = 0x91

After Instruction

RESULT = 0x13

W = 0x93

Z = 1

MOVF **Move f**

Syntax: [*label*] MOVF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: (f) → (dest)

Status Affected: Z

Encoding:

00	1000	dfff	ffff
----	------	------	------

Description: The contents of register f is moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example MOVF FSR, 0

After Instruction

W = value in FSR register

Z = 1

MOVLW **Move Literal to W**

Syntax: [*label*] MOVLW k

Operands: $0 \leq k \leq 255$

Operation: $k \rightarrow (W)$

Status Affected: None

Encoding:

11	00xx	kkkk	kkkk
----	------	------	------

Description: The eight bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.

Words: 1

Cycles: 1

Example MOVLW 0x5A

After Instruction

W = 0x5A

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: $0 \leq f \leq 127$

Operation: (W) → (f)

Status Affected: None

Encoding:

00	0000	1fff	ffff
----	------	------	------

Description: Move data from W register to register 'f'.

Words: 1

Cycles: 1

Example MOVWF OPTION

Before Instruction

OPTION = 0xFF

W = 0x4F

After Instruction

OPTION = 0x4F

W = 0x4F

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NOP	No Operation				
Syntax:	[<i>label</i>] NOP				
Operands:	None				
Operation:	No operation				
Status Affected:	None				
Encoding:	<table border="1"> <tr> <td>00</td> <td>0000</td> <td>0xx0</td> <td>0000</td> </tr> </table>	00	0000	0xx0	0000
00	0000	0xx0	0000		
Description:	No operation.				
Words:	1				
Cycles:	1				
Example	NOP				

RETFIE	Return from Interrupt				
Syntax:	[<i>label</i>] RETFIE				
Operands:	None				
Operation:	TOS → PC, 1 → GIE				
Status Affected:	None				
Encoding:	<table border="1"> <tr> <td>00</td> <td>0000</td> <td>0000</td> <td>1001</td> </tr> </table>	00	0000	0000	1001
00	0000	0000	1001		
Description:	Return from Interrupt. Stack is POPed and Top of Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a two cycle instruction.				
Words:	1				
Cycles:	2				
Example	<pre>RETFIE</pre> <p>After Interrupt</p> <p>PC = TOS GIE = 1</p>				

OPTION	Load Option Register				
Syntax:	[<i>label</i>] OPTION				
Operands:	None				
Operation:	(W) → OPTION				
Status Affected:	None				
Encoding:	<table border="1"> <tr> <td>00</td> <td>0000</td> <td>0110</td> <td>0010</td> </tr> </table>	00	0000	0110	0010
00	0000	0110	0010		
Description:	The contents of the W register are loaded in the OPTION register. This instruction is supported for code compatibility with PIC16C5X products. Since OPTION is a readable/writable register, the user can directly address it.				
Words:	1				
Cycles:	1				
Example	<p>To maintain upward compatibility with future PIC12C67X products, do not use this instruction.</p>				

RETLW	Return with Literal in W				
Syntax:	[<i>label</i>] RETLW k				
Operands:	0 ≤ k ≤ 255				
Operation:	k → (W); TOS → PC				
Status Affected:	None				
Encoding:	<table border="1"> <tr> <td>11</td> <td>01xx</td> <td>kkkk</td> <td>kkkk</td> </tr> </table>	11	01xx	kkkk	kkkk
11	01xx	kkkk	kkkk		
Description:	The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two cycle instruction.				
Words:	1				
Cycles:	2				
Example	<pre>CALL TABLE ;W contains table ;offset value . ;W now has table value . . TABLE ADDWF PC ;W = offset RETLW k1 ;Begin table RETLW k2 ; . . RETLW kn ; End of table</pre> <p>Before Instruction W = 0x07</p> <p>After Instruction W = value of k8</p>				

RETURN **Return from Subroutine**

Syntax: [*label*] RETURN

Operands: None

Operation: TOS → PC

Status Affected: None

Encoding:

00	0000	0000	1000
----	------	------	------

Description: Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two cycle instruction.

Words: 1

Cycles: 2

Example RETURN

After Interrupt
PC = TOS

RRF **Rotate Right f through Carry**

Syntax: [*label*] RRF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: See description below

Status Affected: C

Encoding:

00	1100	dfff	ffff
----	------	------	------

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example RRF REG1, 0

Before Instruction

REG1 = 1110 0110
C = 0

After Instruction

REG1 = 1110 0110
W = 0111 0011
C = 0

RLF **Rotate Left f through Carry**

Syntax: [*label*] RLF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: See description below

Status Affected: C

Encoding:

00	1101	dfff	ffff
----	------	------	------

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example RLF REG1, 0

Before Instruction

REG1 = 1110 0110
C = 0

After Instruction

REG1 = 1110 0110
W = 1100 1100
C = 1

SLEEP

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → \overline{TO} ,
0 → \overline{PD}

Status Affected: \overline{TO} , \overline{PD}

Encoding:

00	0000	0110	0011
----	------	------	------

Description: The power-down status bit, \overline{PD} is cleared. Time-out status bit, \overline{TO} is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped.

Words: 1

Cycles: 1

Example SLEEP

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SUBLW Subtract W from Literal

Syntax: [*label*] SUBLW *k*

Operands: $0 \leq k \leq 255$

Operation: $k - (W) \rightarrow (W)$

Status: C, DC, Z

Affected:

Encoding:

11	110x	kkkk	kkkk
----	------	------	------

Description: The W register is subtracted (2's complement method) from the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example 1: SUBLW 0x02

Before Instruction

W = 1
C = ?

After Instruction

W = 1
C = 1; result is positive

Example 2: Before Instruction

W = 2
C = ?

After Instruction

W = 0
C = 1; result is zero

Example 3: Before Instruction

W = 3
C = ?

After Instruction

W = 0xFF
C = 0; result is negative

SUBWF Subtract W from f

Syntax: [*label*] SUBWF *f,d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) - (W) \rightarrow (\text{dest})$

Status: C, DC, Z

Affected:

Encoding:

00	0010	dfff	ffff
----	------	------	------

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1: SUBWF REG1, 1

Before Instruction

REG1 = 3
W = 2
C = ?

After Instruction

REG1 = 1
W = 2
C = 1; result is positive

Example 2: Before Instruction

REG1 = 2
W = 2
C = ?

After Instruction

REG1 = 0
W = 2
C = 1; result is zero

Example 3: Before Instruction

REG1 = 1
W = 2
C = ?

After Instruction

REG1 = 0xFF
W = 2
C = 0; result is negative

SWAPF	Swap Nibbles in f				
Syntax:	[<i>label</i>] SWAPF f,d				
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]				
Operation:	(f<3:0>) → (dest<7:4>), (f<7:4>) → (dest<3:0>)				
Status Affected:	None				
Encoding:	<table border="1"> <tr> <td>00</td> <td>1110</td> <td>dfff</td> <td>ffff</td> </tr> </table>	00	1110	dfff	ffff
00	1110	dfff	ffff		
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.				
Words:	1				
Cycles:	1				
Example	<pre>SWAPF REG, 0</pre> <p>Before Instruction</p> <pre>REG1 = 0xA5</pre> <p>After Instruction</p> <pre>REG1 = 0xA5 W = 0x5A</pre>				

XORLW	Exclusive OR Literal with W				
Syntax:	[<i>label</i>] XORLW k				
Operands:	0 ≤ k ≤ 255				
Operation:	(W) .XOR. k → (W)				
Status Affected:	Z				
Encoding:	<table border="1"> <tr> <td>11</td> <td>1010</td> <td>kkkk</td> <td>kkkk</td> </tr> </table>	11	1010	kkkk	kkkk
11	1010	kkkk	kkkk		
Description:	The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.				
Words:	1				
Cycles:	1				
Example:	<pre>XORLW 0xAF</pre> <p>Before Instruction</p> <pre>W = 0xB5</pre> <p>After Instruction</p> <pre>W = 0x1A</pre>				

TRIS	Load TRIS Register				
Syntax:	[<i>label</i>] TRIS f				
Operands:	5 ≤ f ≤ 7				
Operation:	(W) → TRIS register f;				
Status Affected:	None				
Encoding:	<table border="1"> <tr> <td>00</td> <td>0000</td> <td>0110</td> <td>0fff</td> </tr> </table>	00	0000	0110	0fff
00	0000	0110	0fff		
Description:	The instruction is supported for code compatibility with the PIC16C5X products. Since TRIS registers are readable and writable, the user can directly address them.				
Words:	1				
Cycles:	1				
Example	<p>To maintain upward compatibility with future PIC12C67X products, do not use this instruction.</p>				

XORWF	Exclusive OR W with f				
Syntax:	[<i>label</i>] XORWF f,d				
Operands:	0 ≤ f ≤ 127 d ∈ [0,1]				
Operation:	(W) .XOR. (f) → (dest)				
Status Affected:	Z				
Encoding:	<table border="1"> <tr> <td>00</td> <td>0110</td> <td>dfff</td> <td>ffff</td> </tr> </table>	00	0110	dfff	ffff
00	0110	dfff	ffff		
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.				
Words:	1				
Cycles:	1				
Example	<pre>XORWF REG 1</pre> <p>Before Instruction</p> <pre>REG = 0xAF W = 0xB5</pre> <p>After Instruction</p> <pre>REG = 0x1A W = 0xB5</pre>				

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NOTES:

11.0 DEVELOPMENT SUPPORT

11.1 Development Tools

The PICmicro™ microcontrollers are supported with a full range of hardware and software development tools:

- MPLAB™-ICE Real-Time In-Circuit Emulator
- ICEPIC™ Low-Cost PIC16C5X and PIC16CXXX In-Circuit Emulator
- PRO MATE® II Universal Programmer
- PICSTART® Plus Entry-Level Prototype Programmer
- SIMICE
- PICDEM-1 Low-Cost Demonstration Board
- PICDEM-2 Low-Cost Demonstration Board
- PICDEM-3 Low-Cost Demonstration Board
- MPASM Assembler
- MPLAB™ SIM Software Simulator
- MPLAB-C17 (C Compiler)
- Fuzzy Logic Development System (*fuzzyTECH*®-MP)
- KEELOQ® Evaluation Kits and Programmer

11.2 MPLAB-ICE: High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB-ICE Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers (MCUs). MPLAB-ICE is supplied with the MPLAB Integrated Development Environment (IDE), which allows editing, "make" and download, and source debugging from a single environment.

Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB-ICE allows expansion to support all new Microchip microcontrollers.

The MPLAB-ICE Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC compatible 386 (and higher) machine platform and Microsoft Windows® 3.x or Windows 95 environment were chosen to best make these features available to you, the end user.

MPLAB-ICE is available in two versions. MPLAB-ICE 1000 is a basic, low-cost emulator system with simple trace capabilities. It shares processor modules with the MPLAB-ICE 2000. This is a full-featured emulator system with enhanced trace, trigger, and data monitoring features. Both systems will operate across the entire operating speed range of the PICmicro MCU.

11.3 ICEPIC: Low-Cost PICmicro™ In-Circuit Emulator

ICEPIC is a low-cost in-circuit emulator solution for the Microchip PIC12CXXX, PIC16C5X and PIC16CXXX families of 8-bit OTP microcontrollers.

ICEPIC is designed to operate on PC-compatible machines ranging from 386 through Pentium™ based machines under Windows 3.x, Windows 95, or Windows NT environment. ICEPIC features real time, non-intrusive emulation.

11.4 PRO MATE II: Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode. PRO MATE II is CE compliant.

The PRO MATE II has programmable VDD and VPP supplies which allows it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for displaying error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode the PRO MATE II can read, verify or program PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices. It can also set configuration and code-protect bits in this mode.

11.5 PICSTART Plus Entry Level Development System

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. PICSTART Plus is not recommended for production programming.

PICSTART Plus supports all PIC12CXXX, PIC14C000, PIC16C5X, PIC16CXXX and PIC17CXX devices with up to 40 pins. Larger pin count devices such as the PIC16C923, PIC16C924 and PIC17C756 may be supported with an adapter socket. PICSTART Plus is CE compliant.

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11.6 SIMICE Entry-Level Hardware Simulator

SIMICE is an entry-level hardware development system designed to operate in a PC-based environment with Microchip's simulator MPLAB™-SIM. Both SIMICE and MPLAB-SIM run under Microchip Technology's MPLAB Integrated Development Environment (IDE) software. Specifically, SIMICE provides hardware simulation for Microchip's PIC12C5XX, PIC12CE5XX, and PIC16C5X families of PICmicro™ 8-bit microcontrollers. SIMICE works in conjunction with MPLAB-SIM to provide non-real-time I/O port emulation. SIMICE enables a developer to run simulator code for driving the target system. In addition, the target system can provide input to the simulator code. This capability allows for simple and interactive debugging without having to manually generate MPLAB-SIM stimulus files. SIMICE is a valuable debugging tool for entry-level system development.

11.7 PICDEM-1 Low-Cost PICmicro Demonstration Board

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-Plus programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the MPLAB-ICE emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

11.8 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-Plus, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I²C bus and separate headers for connection to an LCD module and a keypad.

11.9 PICDEM-3 Low-Cost PIC16CXXX Demonstration Board

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

11.10 MPLAB Integrated Development Environment Software

The MPLAB IDE Software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a windows based application which contains:

- A full featured editor
- Three operating modes
 - editor
 - emulator
 - simulator
- A project manager
- Customizable tool bar and key mapping
- A status bar with project information
- Extensive on-line help

MPLAB allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PICmicro tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file

The ability to use MPLAB with Microchip's simulator allows a consistent platform and the ability to easily switch from the low cost simulator to the full featured emulator with minimal retraining due to development tools.

11.11 Assembler (MPASM)

The MPASM Universal Macro Assembler is a PC-hosted symbolic assembler. It supports all microcontroller series including the PIC12C5XX, PIC14000, PIC16C5X, PIC16CXXX, and PIC17CXX families.

MPASM offers full featured Macro capabilities, conditional assembly, and several source and listing formats. It generates various object code formats to support Microchip's development tools as well as third party programmers.

MPASM allows full symbolic debugging from MPLAB-ICE, Microchip's Universal Emulator System.

MPASM has the following features to assist in developing software for specific use applications.

- Provides translation of Assembler source code to object code for all Microchip microcontrollers.
- Macro assembly capability.
- Produces all the files (Object, Listing, Symbol, and special) required for symbolic debug with Microchip's emulator systems.
- Supports Hex (default), Decimal and Octal source and listing formats.

MPASM provides a rich directive language to support programming of the PICmicro. Directives are helpful in making the development of your assemble source code shorter and more maintainable.

11.12 Software Simulator (MPLAB-SIM)

The MPLAB-SIM Software Simulator allows code development in a PC host environment. It allows the user to simulate the PICmicro series microcontrollers on an instruction level. On any given instruction, the user may examine or modify any of the data areas or provide external stimulus to any of the pins. The input/output radix can be set by the user and the execution can be performed in; single step, execute until break, or in a trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C17 and MPASM. The Software Simulator offers the low cost flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

11.13 MPLAB-C17 Compiler

The MPLAB-C17 Code Development System is a complete ANSI 'C' compiler and integrated development environment for Microchip's PIC17CXXX family of microcontrollers. The compiler provides powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compiler provides symbol information that is compatible with the MPLAB IDE memory display.

11.14 Fuzzy Logic Development System (fuzzyTECH-MP)

fuzzyTECH-MP fuzzy logic development tool is available in two versions - a low cost introductory version, MP Explorer, for designers to gain a comprehensive working knowledge of fuzzy logic system design; and a full-featured version, *fuzzyTECH-MP*, Edition for implementing more complex systems.

Both versions include Microchip's *fuzzyLAB*[™] demonstration board for hands-on experience with fuzzy logic systems implementation.

11.15 SEEVAL[®] Evaluation and Programming System

The SEEVAL SEEPROM Designer's Kit supports all Microchip 2-wire and 3-wire Serial EEPROMs. The kit includes everything necessary to read, write, erase or program special features of any Microchip SEEPROM product including Smart Serials[™] and secure serials. The Total Endurance[™] Disk is included to aid in trade-off analysis and reliability calculations. The total kit can significantly reduce time-to-market and result in an optimized system.

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11.16 KEELOQ® Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

TABLE 11-1: DEVELOPMENT TOOLS FROM MICROCHIP

	PIC12C5XX	PIC14000	PIC16C5X	PIC16CXX	PIC16C6X	PIC16C7XX	PIC16C8X	PIC16C9XX	PIC17C4X	PIC17C7XX	24CXX 25CXX 93CXX	HCS200 HCS300 HCS301
Emulator Products												
MPLAB™-ICE	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
ICEPIC™ Low-Cost In-Circuit Emulator			✓	✓	✓	✓	✓	✓				
Software Tools												
MPLAB™ Integrated Development Environment	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
MPLAB™ C17* Compiler									✓	✓		
fuzzyTECH®-MP Explorer/Edition Fuzzy Logic Dev. Tool	✓	✓	✓	✓	✓	✓	✓	✓	✓			
Total Endurance™ Software Model											✓	
PICSTART®Plus Low-Cost Universal Dev. Kit	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Programmers												
PRO MATE® II Universal Programmer	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
KEELOQ® Programmer												✓
SEEVAL® Designers Kit											✓	
Demo Boards												
SIMICE	✓		✓									
PICDEM-14A		✓										
PICDEM-1			✓	✓			✓		✓			
PICDEM-2					✓	✓						
PICDEM-3								✓				
KEELOQ® Evaluation Kit												✓
KEELOQ Transponder Kit												✓

PIC12CE67X

NOTES:

12.0 ELECTRICAL CHARACTERISTICS FOR PIC12CE67X

Absolute Maximum Ratings †

Ambient temperature under bias	-40° to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to VSS (except VDD and MCLR).....	-0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS	0 to +7.0V
Voltage on MCLR with respect to VSS (Note 2).....	0 to +14V
Total power dissipation (Note 1).....	700 mW
Maximum current out of VSS pin	150 mA
Maximum current into VDD pin	125 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > VDD).....	± 20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > VDD).....	± 20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by GPIO pins combined.....	100 mA
Maximum current sourced by GPIO pins combined.....	100 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} + \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum \{V_{OL} \times I_{OL}\}$.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 12-1: CROSS REFERENCE OF DEVICE SPECS FOR OSCILLATOR CONFIGURATIONS AND FREQUENCIES OF OPERATION (COMMERCIAL DEVICES)

OSC	PIC12CE673-04 PIC12CE674-04	PIC12CE673-10 PIC12CE674-10	PIC12LCE673-04 PIC12LCE674-04	PIC12CE673/JW PIC12CE674/JW
INTRC	VDD: 3.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 21 μ A max. at 4V Freq: 4 MHz max.	VDD: 3.0V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μ A typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 5.5V IDD: 2.0 mA typ. at 2.5V IPD: 0.9 μ A typ. at 2.5V Freq: 4 MHz max.	VDD: 3.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 21 μ A max. at 4V Freq: 4 MHz max.
EXTRC	VDD: 3.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 21 μ A max. at 4V Freq: 4 MHz max.	VDD: 3.0V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μ A typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 5.5V IDD: 2.0 mA typ. at 2.5V IPD: 0.9 μ A typ. at 2.5V Freq: 4 MHz max.	VDD: 3.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 21 μ A max. at 4V Freq: 4 MHz max.
XT	VDD: 3.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 21 μ A max. at 4V Freq: 4 MHz max.	VDD: 3.0V to 5.5V IDD: 2.7 mA typ. at 5.5V IPD: 1.5 μ A typ. at 4V Freq: 4 MHz max.	VDD: 2.5V to 5.5V IDD: 2.0 mA typ. at 2.5V IPD: 0.9 μ A typ. at 2.5V Freq: 4 MHz max.	VDD: 3.0V to 5.5V IDD: 5 mA max. at 5.5V IPD: 21 μ A max. at 4V Freq: 4 MHz max.
HS	VDD: 4.5V to 5.5V IDD: 13.5 mA typ. at 5.5V IPD: 1.5 μ A typ. at 4.5V Freq: 4 MHz max.	VDD: 4.5V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 μ A typ. at 4.5V Freq: 10 MHz max.	N/A	VDD: 3.0V to 5.5V IDD: 30 mA max. at 5.5V IPD: 1.5 μ A typ. at 4.5V Freq: 10 MHz max.
LP	VDD: 3.0V to 5.5V IDD: 52.5 μ A typ. at 32 kHz, 4.0V IPD: 0.9 μ A typ. at 4.0V Freq: 200 kHz max.	N/A	VDD: 2.5V to 5.5V IDD: 48 μ A max. at 32 kHz, 2.5V IPD: 5.0 μ A max. at 2.5V Freq: 200 kHz max.	VDD: 3.0V to 5.5V IDD: 48 μ A max. at 32 kHz, 2.5V IPD: 5.0 μ A max. at 2.5V Freq: 200 kHz max.

The shaded sections indicate oscillator selections which are tested for functionality, but not for MIN/MAX specifications. It is recommended that the user select the device type that ensures the specifications required.

12.1 DC Characteristics: PIC12CE673-04 (Commercial, Industrial, Extended)⁽⁵⁾
 PIC12CE673-10 (Commercial, Industrial, Extended)⁽⁵⁾
 PIC12CE674-04 (Commercial, Industrial, Extended)⁽⁵⁾
 PIC12CE674-10 (Commercial, Industrial, Extended)⁽⁵⁾

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise specified)					
		Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended)					
Parm No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D001	Supply Voltage	VDD	3.0	-	5.5	V	XT, INTRC, EXTRC and LP osc configuration
D001A			4.5	-	5.5	V	HS osc configuration
D002	RAM Data Retention Voltage (Note 1)	VDR	-	1.5	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	VSS	-	VSS	V	See section on Power-on Reset for details
D004	VDD rise rate to ensure internal Power-on Reset signal	SVD	0.05	-	-	V/ms	See section on Power-on Reset for details
D010	Supply Current (Note 2) No read/write to EEPROM peripheral	IDD	-	2.7	3.3	mA	XT, EXTRC osc configuration (PIC12CE67X-04) FOSC = 4 MHz, VDD = 5.5V (Note 4)
D010A			-	2.7	3.3	mA	INTRC osc configuration FOSC = 4 MHz, VDD = 5.5V (Note 6)
D013			-	TBD	15	mA	HS osc configuration (PIC12CE67X-10) FOSC = 10 MHz, VDD = 5.5V
D028	ΔIEE			0.1	0.2		VDD = 5.5V SCL = 400 kHz
D020	Power-down Current (Note 3)	IPD	-	5.5	32	μA	VDD = 4.0V, WDT enabled, -40°C to +85°C
D021			-	1.5	16	μA	VDD = 4.0V, WDT disabled, 0°C to +70°C
D021A			-	1.5	14	μA	VDD = 4.0V, WDT disabled, -40°C to +85°C
D021B			-	1.5	TBD	μA	VDD = 4.0V, WDT disabled, -40°C to +125°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD

MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For EXTRC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{ext}$ (mA) with Rext in kOhm.

5: Extended operating range is Advance Information for this device.

6: INTRC calibration value is for 4 MHz nominal at 5V, 35°C.

PIC12CE67X

12.2 DC Characteristics: PIC12LCE673-04 (Commercial, Industrial) PIC12LCE674-04 (Commercial, Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise specified)					
		Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial)					
Param No.	Characteristic	Sym	Min	Typ†	Max	Units	Conditions
D001	Supply Voltage	VDD	2.5	-	5.5	V	XT, INTRC, EXTRC and LP osc configuration (DC - 4 MHz)
D002*	RAM Data Retention Voltage (Note 1)	VDR	-	TBD	-	V	Device in SLEEP mode
D003	VDD start voltage to ensure internal Power-on Reset signal	VPOR	-	VSS	-	V	See section on Power-on Reset for details
D004*	VDD rise rate to ensure internal Power-on Reset signal	SVDD	TBD	-	-	V/ms	See section on Power-on Reset for details
D010	Supply Current (Note 2)	IDD	-	TBD	TBD	mA	XT, EXTRC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 4)
D010B				TBD	TBD	mA	INTRC osc configuration FOSC = 4 MHz, VDD = 3.0V (Note 5)
D010A				TBD	TBD	μA	LP osc configuration FOSC = 32 kHz, VDD = 3.0V, WDT disabled
D020	Power-down Current (Note 3)	IPD	-	TBD		μA	VDD = 3.0V, WDT enabled, -40°C to +85°C
D021				TBD		μA	VDD = 3.0V, WDT disabled, 0°C to +70°C
D021A				TBD		μA	VDD = 3.0V, WDT disabled, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail to rail; all I/O pins tristated, pulled to VDD
MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

4: For EXTRC osc configuration, current through Rext is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{ext}$ (mA) with Rext in kOhm.

5: INTRC calibration value is for 4 MHz nominal at 5V, 25°C.

12.3 DC Characteristics: PIC12CE673-04 (Commercial, Industrial, Extended)⁽⁴⁾
 PIC12CE673-10 (Commercial, Industrial, Extended)⁽⁴⁾
 PIC12CE674-04 (Commercial, Industrial, Extended)⁽⁴⁾
 PIC12CE674-10 (Commercial, Industrial, Extended)⁽⁴⁾

Standard Operating Conditions (unless otherwise specified)							
DC CHARACTERISTICS							
				Operating temperature 0°C ≤ TA ≤ +70°C (commercial) -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended)			
				Operating voltage VDD range as described in DC spec Section 12.1 and Section 12.2.			
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
D030	Input Low Voltage I/O ports with TTL buffer	VIL	VSS	-	0.5V	V	
D031	with Schmitt Trigger buffer		VSS	-	0.2VDD	V	
D032	MCLR, GP2/T0CKI/AN2/INT (in EXTRC mode)		VSS	-	0.2VDD	V	
D033	OSC1 (in XT, HS and LP)		VSS	-	0.3VDD	V	
D040	Input High Voltage I/O ports with TTL buffer	VIH	2.0	-	VDD	V	4.5 ≤ VDD ≤ 5.5V
D040A			0.8VDD	-	VDD	V	For VDD > 5.5V or VDD < 4.5V
D041	with Schmitt Trigger buffer		0.8VDD	-	VDD	V	For entire VDD range
D042	MCLR, GP2/T0CKI/AN2/INT		0.8VDD	-	VDD	V	
D042A	OSC1 (XT, HS and LP)		0.7VDD	-	VDD	V	Note1
D043	OSC1 (in EXTRC mode)		0.9VDD	-	VDD	V	
D070	GPIO weak pull-up current	IPUR	50	250	400	µA	VDD = 5V, VPIN = VSS
D060	Input Leakage Current (Notes 2, 3) I/O ports	IIL	-	-	±1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
D061	MCLR, GP2/T0CKI		-	-	±5 ⁽⁵⁾	µA	VSS ≤ VPIN ≤ VDD
D063	OSC1		-	-	±5	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
D080	Output Low Voltage I/O ports/CLKOUT	VOL	-	-	0.6	V	IOL = 8.5 mA, VDD = 4.5V, -40°C to +85°C
D080A			-	-	0.6	V	IOL = 7.0 mA, VDD = 4.5V, -40°C to +125°C
D083	OSC2		-	-	0.6	V	IOL = 1.6 mA, VDD = 4.5V, -40°C to +85°C
D083A			-	-	0.6	V	IOL = 1.2 mA, VDD = 4.5V, -40°C to +125°C

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C67X be driven with external clock in RC mode.
- 2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3: Negative current is defined as coming out of the pin.
- 4: **Extended operating range is Advance Information for this device.**
- 5: When configured as external reset, the input leakage current is the weak pull-up current of -10mA minimum. This pull-up is weaker than the standard I/O pull-up.

PIC12CE67X

Standard Operating Conditions (unless otherwise specified)							
DC CHARACTERISTICS Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial) $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended) Operating voltage V_{DD} range as described in DC spec Section 12.1 and Section 12.2.							
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
D090	Output High Voltage I/O ports/CLKOUT (Note 3)	V_{OH}	$V_{DD} - 0.7$	-	-	V	$I_{OH} = -3.0\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+85^{\circ}\text{C}$
D090A			$V_{DD} - 0.7$	-	-	V	$I_{OH} = -2.5\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+125^{\circ}\text{C}$
D092	OSC2		$V_{DD} - 0.7$	-	-	V	$I_{OH} = -1.3\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+85^{\circ}\text{C}$
D092A			$V_{DD} - 0.7$	-	-	V	$I_{OH} = -1.0\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+125^{\circ}\text{C}$
D100	Capacitive Loading Specs on Output Pins OSC2 pin	C_{OSC2}	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2	C_{IO}	-	-	50	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C67X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: Extended operating range is Advance Information for this device.

5: When configured as external reset, the input leakage current is the weak pull-up current of -10mA minimum. This pull-up is weaker than the standard I/O pull-up.

PRELIMINARY

12.4 DC Characteristics: PIC12LCE671-04 (Commercial, Industrial) PIC12LCE672-04 (Commercial, Industrial)

Standard Operating Conditions (unless otherwise specified)								
DC CHARACTERISTICS								
Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial)								
Operating voltage V_{DD} range as described in DC spec Section 12.1 and Section 12.2.								
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions	
D030	Input Low Voltage I/O ports with TTL buffer	V_{IL}	V_{SS}	-	TBD	V	Note 1	
D031	with Schmitt Trigger buffer		V_{SS}	-	TBD	V		
D032	$\overline{\text{MCLR}}$, GP2/T0CKI/AN2/INT (in EXTRC mode)		V_{SS}	-	TBD	V		
D033	OSC1 (in XT, HS and LP)		V_{SS}	-	TBD	V		
D040	Input High Voltage I/O ports with TTL buffer	V_{IH}	TBD	-	V_{DD}	V	4.5 ≤ V_{DD} ≤ 5.5V For $V_{DD} > 5.5\text{V}$ or $V_{DD} < 4.5\text{V}$ For entire V_{DD} range Note 1	
D040A			TBD	-	V_{DD}	V		
D041	with Schmitt Trigger buffer		TBD	-	V_{DD}	V		
D042	$\overline{\text{MCLR}}$, GP2/T0CKI/AN2/INT		TBD	-	V_{DD}	V		
D042A	OSC1 (XT, HS and LP)		TBD	-	V_{DD}	V		
D043	OSC1 (in EXTRC mode)		TBD	-	V_{DD}	V		
D070	GPIO weak pull-up current	IPUR	TBD	TBD	TBD	μA	$V_{DD} = 5\text{V}$, $V_{PIN} = V_{SS}$	
D060	Input Leakage Current (Notes 2, 3) I/O ports	I_{IL}	-	TBD	TBD	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, Pin at hi-impedance	
D061	$\overline{\text{MCLR}}$, GP3		TBD	TBD	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$		
D063	OSC1		TBD	TBD	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, XT, HS and LP osc configuration		
D080	Output Low Voltage I/O ports/CLKOUT	V_{OL}	-	TBD	0.6	V	$I_{OL} = \text{TBD}$, $V_{DD} = 4.5\text{V}$, -40°C to +85°C	
D080A			-	TBD	0.6	V		$I_{OL} = \text{TBD}$, $V_{DD} = 4.5\text{V}$, -40°C to +125°C
D083	OSC2		-	TBD	0.6	V		$I_{OL} = \text{TBD}$, $V_{DD} = 4.5\text{V}$, -40°C to +85°C
D083A			-	TBD	0.6	V		$I_{OL} = \text{TBD}$, $V_{DD} = 4.5\text{V}$, -40°C to +125°C
D090	Output High Voltage I/O ports/CLKOUT (Note 3)	V_{OH}	$V_{DD} - 0.7$	-	-	V	$I_{OH} = \text{TBD}$, $V_{DD} = 4.5\text{V}$, -40°C to +85°C	
D090A			$V_{DD} - 0.7$	-	-	V		$I_{OH} = \text{TBD}$, $V_{DD} = 4.5\text{V}$, -40°C to +125°C
D092	OSC2		$V_{DD} - 0.7$	-	-	V		$I_{OH} = \text{TBD}$, $V_{DD} = 4.5\text{V}$, -40°C to +85°C
D092A			$V_{DD} - 0.7$	-	-	V		$I_{OH} = \text{TBD}$, $V_{DD} = 4.5\text{V}$, -40°C to +125°C

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C67X be driven with external clock in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: **Extended operating range is Advance Information for this device.**

PIC12CE67X

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise specified)					
		Operating temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial) $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial)					
		Operating voltage V_{DD} range as described in DC spec Section 12.1 and Section 12.2.					
Param No.	Characteristic	Sym	Min	Typ †	Max	Units	Conditions
D100	Capacitive Loading Specs on Output Pins OSC2 pin	Cosc2	-	-	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	All I/O pins and OSC2	Cio	-	-	50	pF	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C67X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: **Extended operating range is Advance Information for this device.**

PRELIMINARY

12.5 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I²C specifications only)
4. Ts (I²C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	RD
cs	CS	rw	RD or WR
di	SDI	sc	SCK
do	SDO	ss	SS
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	MCLR	wr	WR

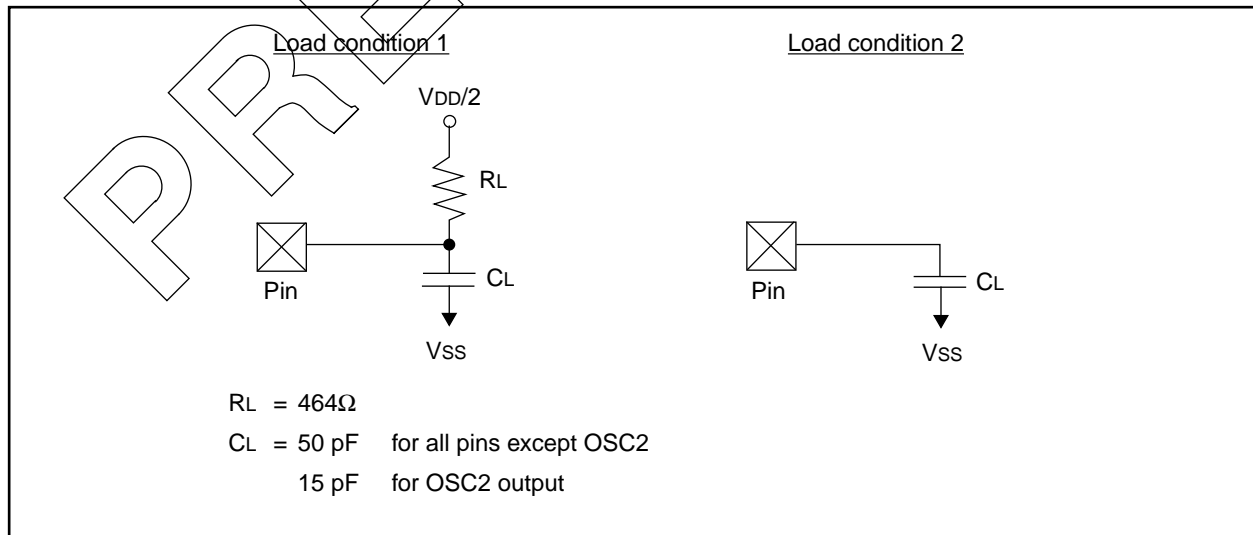
Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	Y	Valid
L	Low	Z	Hi-impedance
I²C only		High	High
AA	output access	Low	Low
BUF	Bus free		

TCC:ST (I²C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	STOP condition
STA	START condition		

FIGURE 12-1: LOAD CONDITIONS



PIC12CE67X

12.6 Timing Diagrams and Specifications

FIGURE 12-2: EXTERNAL CLOCK TIMING

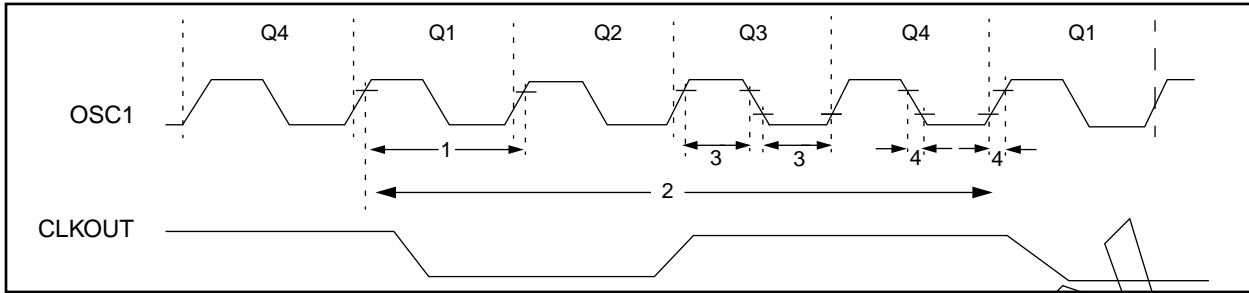


TABLE 12-2: CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	External CLKIN Frequency (Note 1)	DC	—	4	MHz	XT and EXTRC osc mode
			DC	—	4	MHz	HS osc mode (PIC12CE67X-04)
			DC	—	10	MHz	HS osc mode (PIC12CE67X-10)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	EXTRC osc mode
			.455	—	4	MHz	XT osc mode
1	Tosc	External CLKIN Period (Note 1)	4	—	4	MHz	HS osc mode (PIC12CE67X-04)
			4	—	10	MHz	HS osc mode (PIC12CE67X-10)
			5	—	200	kHz	LP osc mode
			250	—	—	ns	XT and EXTRC osc mode
		Oscillator Period (Note 1)	250	—	—	ns	EXTRC osc mode
			250	—	10,000	ns	XT osc mode
2	Tcy	Instruction Cycle Time (Note 1)	250	—	250	ns	HS osc mode (PIC12CE67X-04)
			100	—	250	ns	HS osc mode (PIC12CE67X-10)
			5	—	—	μs	LP osc mode
			400	—	DC	ns	Tcy = 4/Fosc
3	TosL, TosH	External Clock in (OSC1) High or Low Time	50	—	—	ns	XT oscillator
			2.5	—	—	μs	LP oscillator
			10	—	—	ns	HS oscillator
4	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "Max." cycle time limit is "DC" (no clock) for all devices. OSC2 is disconnected (has no loading) for the PIC12CE67X.

TABLE 12-3: CALIBRATED INTERNAL RC FREQUENCIES - PIC12C508/C509

AC Characteristics		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial), $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial), $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ (extended)					
		Operating Voltage V_{DD} range is described in Section 10.1					
Parameter No.	Sym	Characteristic	Min*	Typ ⁽¹⁾	Max*	Units	Conditions
		Internal Calibrated RC Frequency	TBD	4.00	TBD	MHz	$V_{DD} = 5.0\text{V}$
		Internal Calibrated RC Frequency	TBD	4.00	TBD	MHz	$V_{DD} = 2.5\text{V}$

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PRELIMINARY

PIC12CE67X

FIGURE 12-3: CLKOUT AND I/O TIMING

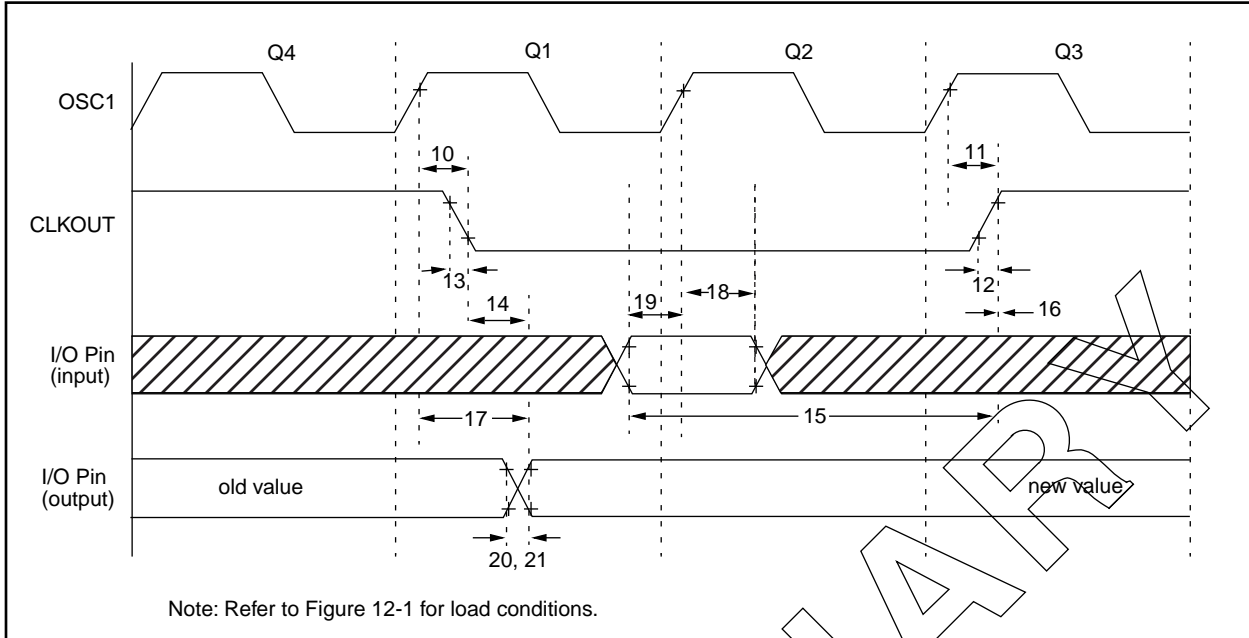


TABLE 12-4: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1↑ to CLKOUT↓	—	15	30	ns	Note 1
11*	TosH2ckH	OSC1↑ to CLKOUT↑	—	15	30	ns	Note 1
12*	TckR	CLKOUT rise time	—	5	15	ns	Note 1
13*	TckF	CLKOUT fall time	—	5	15	ns	Note 1
14*	TckL2ioV	CLKOUT ↓ to Port out valid	—	—	0.5T _{CY} + 20	ns	Note 1
15*	TioV2ckH	Port in valid before CLKOUT ↑	0.25T _{CY} + 25	—	—	ns	Note 1
16*	TckH2ioI	Port in hold after CLKOUT ↑	0	—	—	ns	Note 1
17*	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	—	—	80 - 100	ns	
18*	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns	
19*	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns	
20*	TioR	Port output rise time	—	10	25	ns	PIC12CE67X
21*	TioF	Port output fall time	—	10	25	ns	PIC12CE67X
22††*	Tinp	INT pin high or low time	20	—	—	ns	
23††*	Trbp	GPIO change INT high or low time	20	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in EXTRC and INTRC modes where CLKOUT output is 4 x T_{osc}.

FIGURE 12-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, AND POWER-UP TIMER TIMING

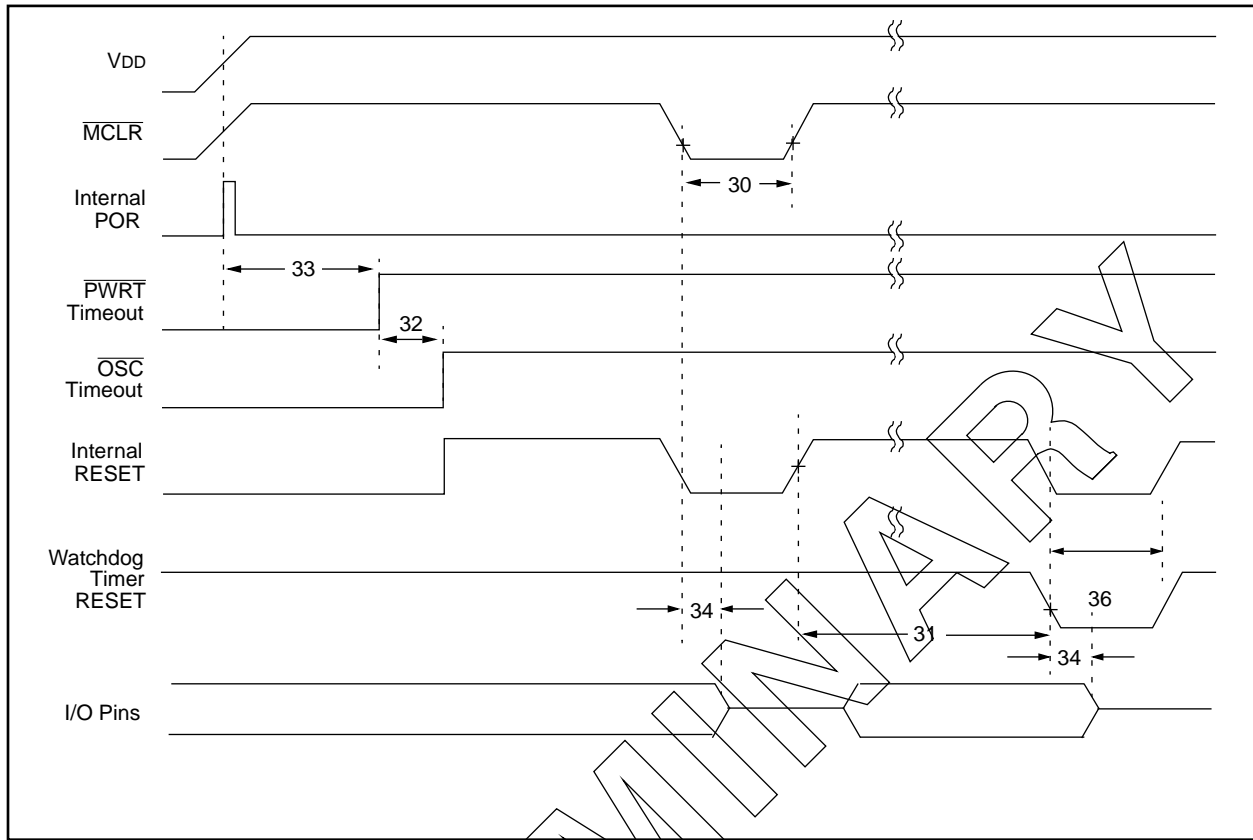


TABLE 12-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	2	—	—	μs	VDD = 5V, -40°C to +125°C
31*	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7	18	33	ms	VDD = 5V, -40°C to +125°C
32	Tost	Oscillation Start-up Timer Period	—	1024Tosc	—	—	Tosc = OSC1 period
33*	Tpwrt	Power up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +125°C
34	Tioz	I/O Hi-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.1	μs	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC12CE67X

FIGURE 12-5: TIMER0 CLOCK TIMINGS

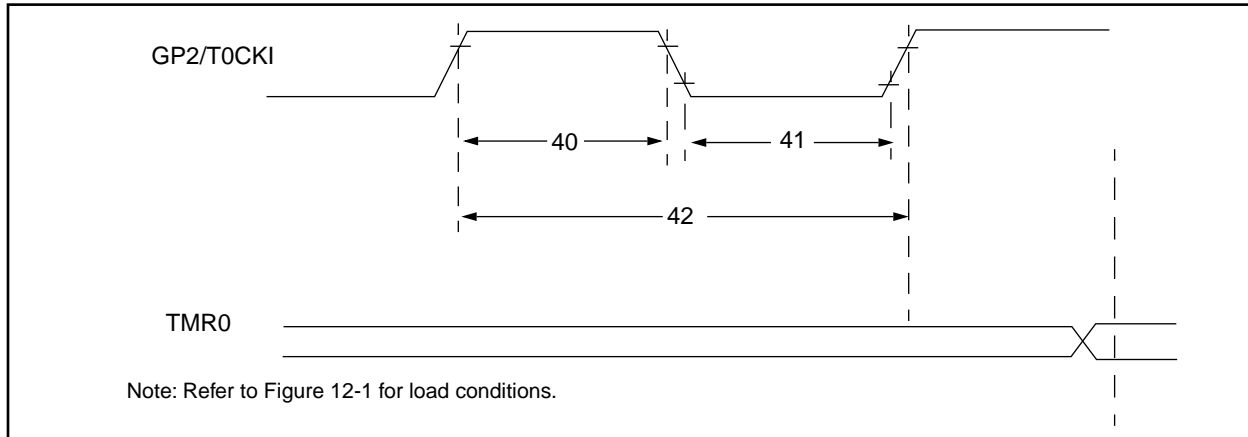


TABLE 12-6: TIMER0 CLOCK REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions	
40	Tt0H	T0CKI High Pulse Width	No Prescaler	$0.5T_{CY} + 20^*$	—	—	ns	
		With Prescaler	10*	—	—	ns		
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	$0.5T_{CY} + 20^*$	—	—	ns	
		With Prescaler	10*	—	—	ns		
42	Tt0P	T0CKI Period	Greater of: $20\mu s$ or $\frac{T_{CY} + 40^*}{N}$		—	—	ns	N = prescale value (1, 2, 4, ..., 256)
48	Tcke2tmrl	Delay from external clock edge to timer increment	2Tosc	—	7Tosc	—		

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

TABLE 12-7: GPIO PULL-UP RESISTOR RANGES

VDD (Volts)	Temperature (°C)	Min	Typ	Max	Units
GP0/GP1					
2.5	-40	38K	42K	63K	Ω
	25	42K	48K	63K	Ω
	85	42K	49K	63K	Ω
	125	50K	55K	63K	Ω
5.5	-40	15K	17K	20K	Ω
	25	18K	20K	23K	Ω
	85	19K	22K	25K	Ω
	125	22K	24K	28K	Ω
GP3					
2.5	-40	285K	346K	417K	Ω
	25	343K	414K	532K	Ω
	85	368K	457K	532K	Ω
	125	431K	504K	593K	Ω
5.5	-40	247K	292K	360K	Ω
	25	288K	341K	437K	Ω
	85	306K	371K	448K	Ω
	125	351K	407K	500K	Ω

* These parameters are characterized but not tested.

TABLE 12-8: A/D CONVERTER CHARACTERISTICS:
PIC12CE673-04 (COMMERCIAL, INDUSTRIAL, EXTENDED⁽³⁾)
PIC12CE673-10 (COMMERCIAL, INDUSTRIAL, EXTENDED⁽³⁾)
PIC12CE674-04 (COMMERCIAL, INDUSTRIAL, EXTENDED⁽³⁾)
PIC12CE674-10 (COMMERCIAL, INDUSTRIAL, EXTENDED⁽³⁾)

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	—	—	8-bits	—	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \leq A_{IN} \leq V_{REF}$ (Notes 4,5)
	NINT	Integral error	—	—	less than ± 1 LSB	—	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \leq A_{IN} \leq V_{REF}$ (Notes 4,5)
	NDIF	Differential error	—	—	less than ± 1 LSB	—	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \leq A_{IN} \leq V_{REF}$ (Notes 4,5)
	NFS	Full scale error	—	—	less than ± 1 LSB	—	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \leq A_{IN} \leq V_{REF}$ (Notes 4,5)
	NOFF	Offset error	—	—	less than ± 1 LSB	—	$V_{REF} = V_{DD} = 5.12V$, $V_{SS} \leq A_{IN} \leq V_{REF}$ (Notes 4,5)
	—	Monotonicity	—	Typ	—	—	$V_{SS} \leq A_{IN} \leq V_{REF}$
	VREF	Reference voltage	3.0V	—	$V_{DD} + 0.3$	V	
	VAIN	Analog input voltage	$V_{SS} - 0.3$	—	$V_{REF} + 0.3$	V	
	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	k Ω	
	IAD	A/D conversion current (VDD)	—	180	—	μA	Average current consumption when A/D is on. (Note 1)
	IREF	VREF input current (Note 2)	—	—	1 10	mA μA	During sampling All other times

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from GP1 pin or VDD pin, whichever is selected as reference input.

3: Extended operating range is Advance Information for this device.

4: These specifications apply if $V_{REF} = 3.0V$ and if $V_{DD} \geq 3.0V$. V_{IN} must be between V_{SS} and V_{REF}

5: When using external VREF, VDD must be greater than 3V for ± 1 LSB accuracy. If VDD is less than 3V, you must use internal VREF for ± 1 LSB.

PIC12CE67X

**TABLE 12-9: A/D CONVERTER CHARACTERISTICS:
PIC12LCE673-04 (COMMERCIAL, INDUSTRIAL)
PIC12LCE674-04 (COMMERCIAL, INDUSTRIAL)**

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	NR	Resolution	—	—	8-bits	—	$V_{REF} = V_{DD} = 3.0V$ (Notes 1,4)
	NINT	Integral error	—	—	less than ± 1 LSb	—	$V_{REF} = V_{DD} = 3.0V$ (Notes 1,4)
	NDIF	Differential error	—	—	less than ± 1 LSb	—	$V_{REF} = V_{DD} = 3.0V$ (Notes 1,4)
	NFS	Full scale error	—	—	less than ± 1 LSb	—	$V_{REF} = V_{DD} = 3.0V$ (Notes 1,4)
	NOFF	Offset error	—	—	less than ± 1 LSb	—	$V_{REF} = V_{DD} = 3.0V$ (Notes 1,4)
	—	Monotonicity	—	Typ	—	—	$V_{SS} \leq A_{IN} \leq V_{REF}$
	VREF	Reference voltage	TBD	—	$V_{DD} + 0.3$	V	
	VAIN	Analog input voltage	$V_{SS} - 0.3$	—	$V_{REF} + 0.3$	V	
	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	k Ω	
	IAD	A/D conversion current (V_{DD})	—	TBD	—	μA	Average current consumption when A/D is on. (Note 2)
	IREF	V_{REF} input current (Note 3)	—	—	TBD TBD	mA μA	During sampling All other times

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1: These specifications apply if $V_{REF} = 3.0V$ and if $V_{DD} \geq 3.0V$. V_{IN} must be between V_{SS} and V_{REF}
- Note 2: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.
- Note 3: V_{REF} current is from GP1 pin or V_{DD} pin, whichever is selected as reference input.
- Note 4: When using external V_{REF} , V_{DD} must be greater than 3V for ± 1 LSB accuracy. If V_{DD} is less than 3V, you must use internal V_{REF} for ± 1 LSB.

FIGURE 12-6: A/D CONVERSION TIMING

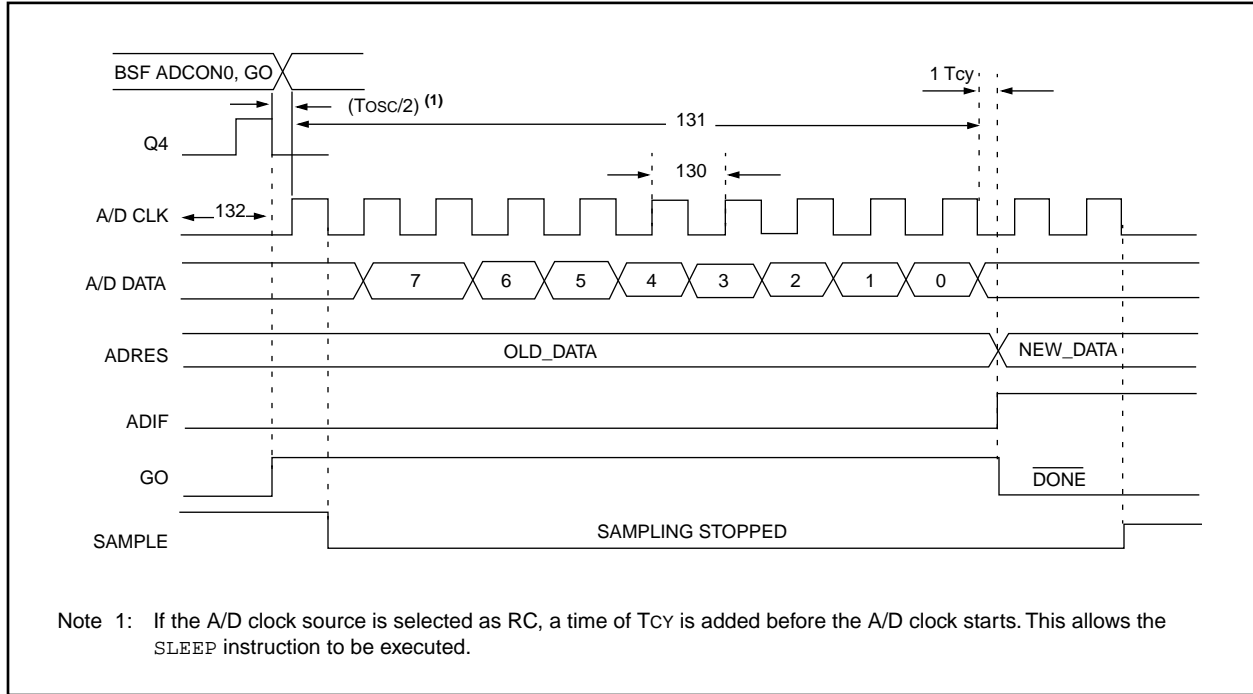


TABLE 12-10: A/D CONVERSION REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	1.6 2.0		— —	μ s μ s	$V_{REF} \geq 3.0V$ V_{REF} full range
130	TAD	A/D Internal RC Oscillator source	3.0 2.0	6.0 4.0	9.0 6.0	μ s μ s	ADCS1:ADCS0 = 11 (RC oscillator source) PIC12LCE67X, $V_{DD} = 3.0V$ PIC12CE67X
131	TCNV	Conversion time (not including S/H time). Note 1	—	$9.5T_{AD}$	—	—	
132	TACQ	Acquisition time	Note 2	20	—	μ s	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: **ADRES** register may be read on the following T_{CY} cycle.

PIC12CE67X

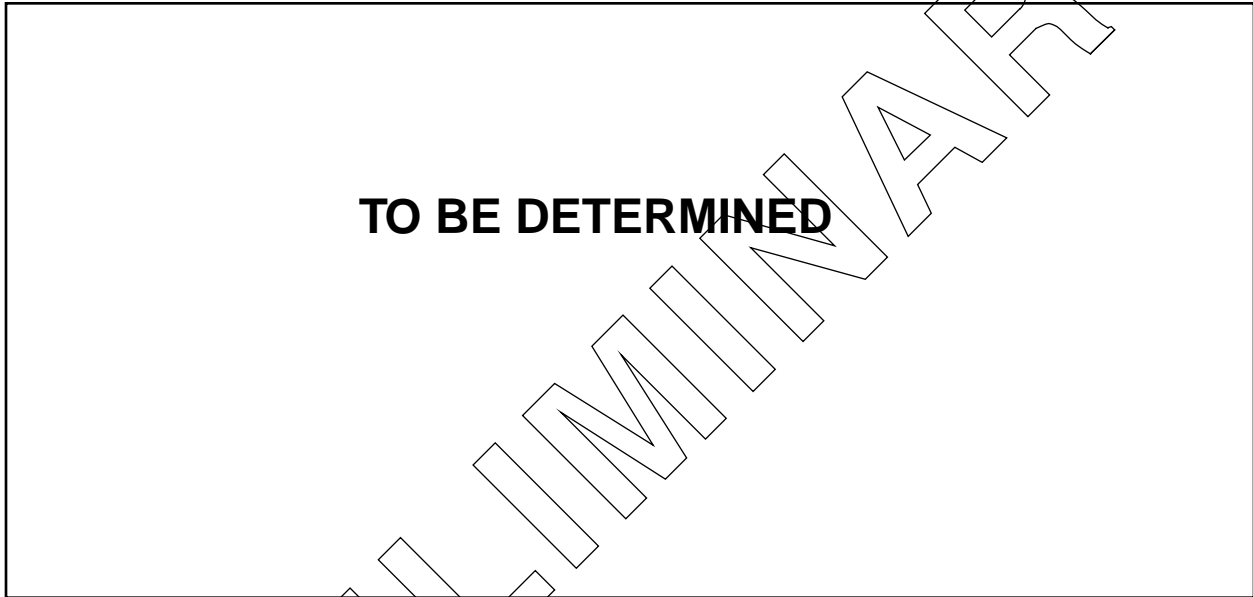
NOTES:

13.0 DC AND AC CHARACTERISTICS - PIC12CE67X

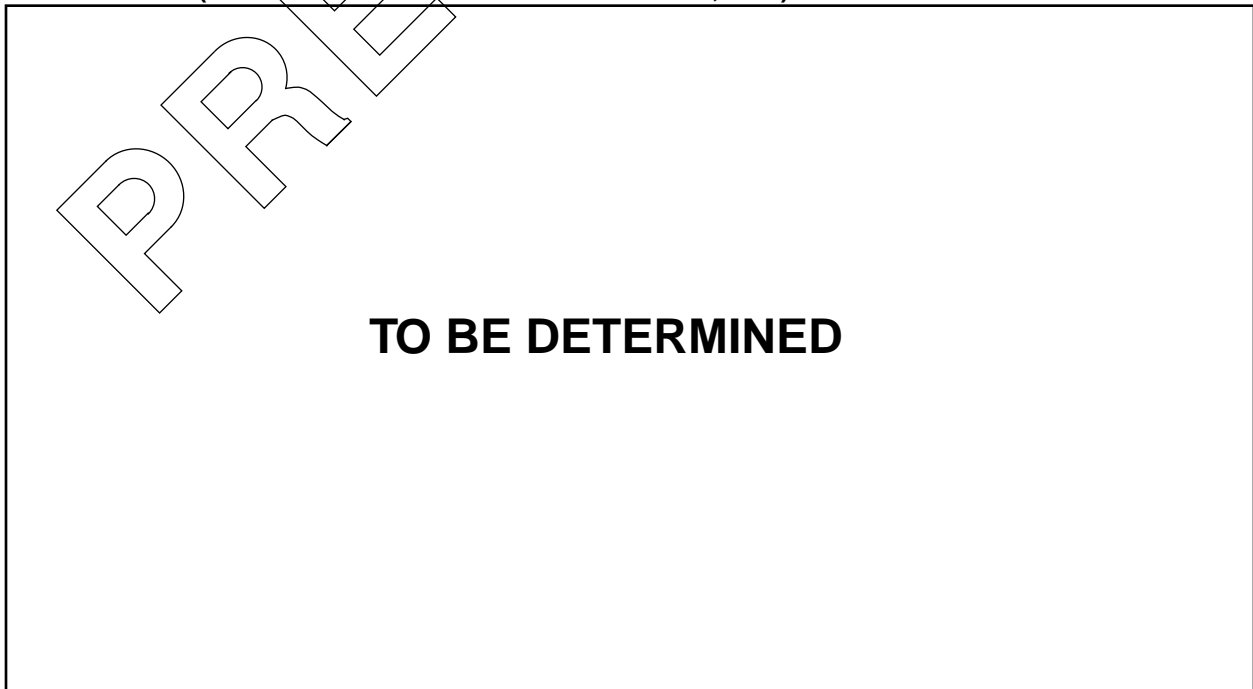
The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified V_{DD} range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3 σ) and (mean - 3 σ) respectively, where σ is standard deviation.

**FIGURE 13-1: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (V_{DD} = 5.0V)
(INTERNAL RC IS CALIBRATED TO 25°C, 5.0V)**



**FIGURE 13-2: CALIBRATED INTERNAL RC FREQUENCY RANGE VS. TEMPERATURE (V_{DD} = 3.0V)
(INTERNAL RC IS CALIBRATED TO 25°C, 5.0V)**



PIC12CE67X

TABLE 13-1: DYNAMIC I_{DD} (TYPICAL) - WDT ENABLED, 25°C

Oscillator	Frequency	V _{DD} = 2.5V	V _{DD} = 5.5V
External RC	4 MHz	TBD μ A*	620 μ A*
Internal RC	4 MHz	TBD μ A	1.1 mA
XT	4 MHz	TBD μ A	775 μ A
LP	32 KHz	TBD μ A	37 μ A

*Does not include current through external R&C.

FIGURE 13-3: WDT TIMER TIME-OUT PERIOD vs. V_{DD}

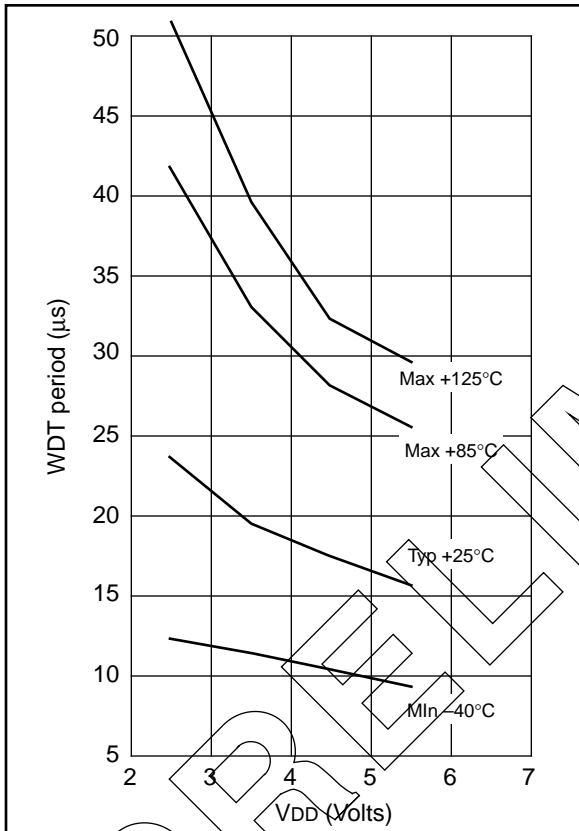


FIGURE 13-4: I_{OH} vs. V_{OH} , $V_{DD} = 2.5$ V

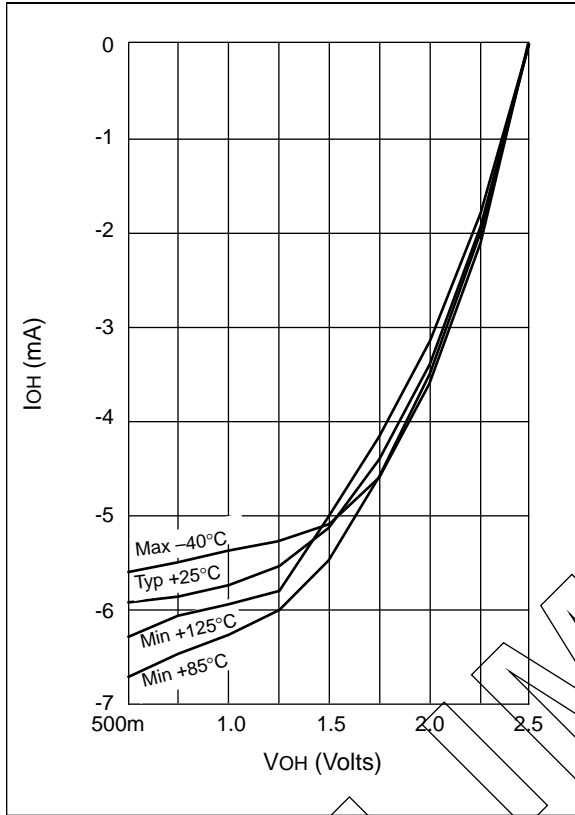


FIGURE 13-6: I_{OL} vs. V_{OL} , $V_{DD} = 2.5$ V

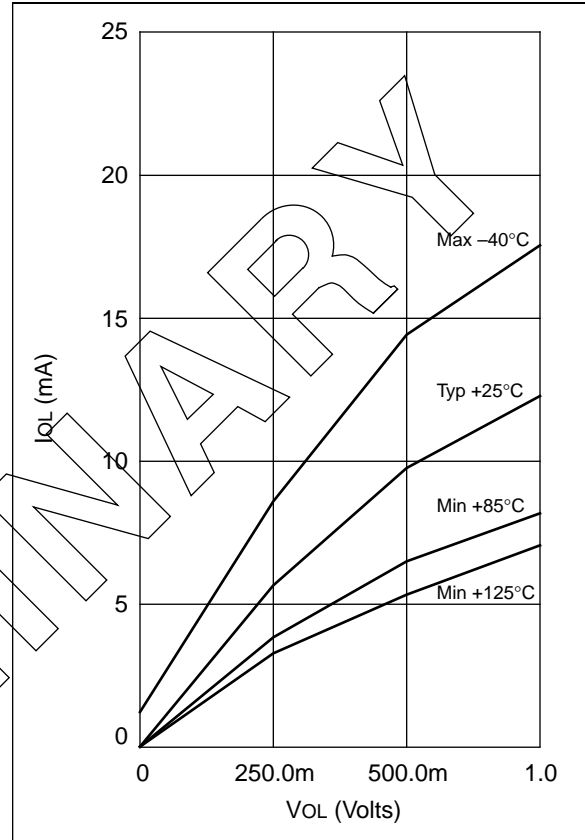


FIGURE 13-5: I_{OH} vs. V_{OH} , $V_{DD} = 3.5$ V

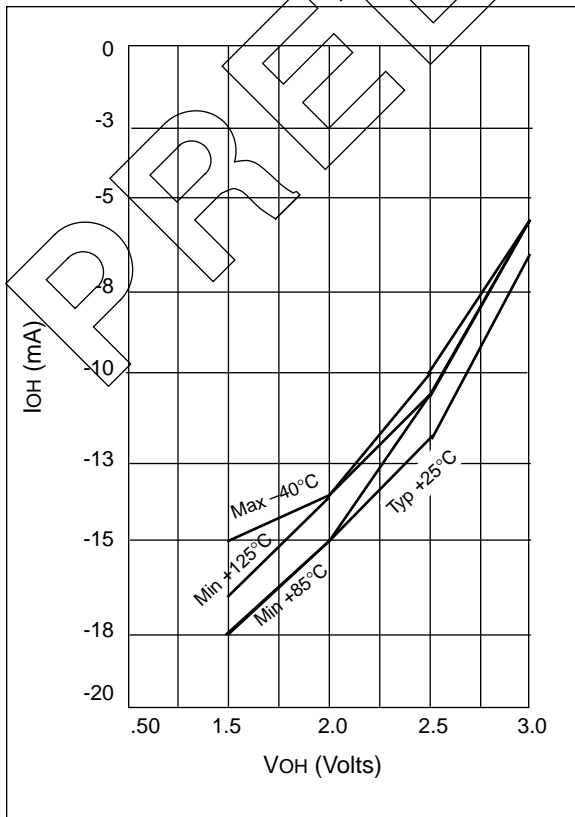
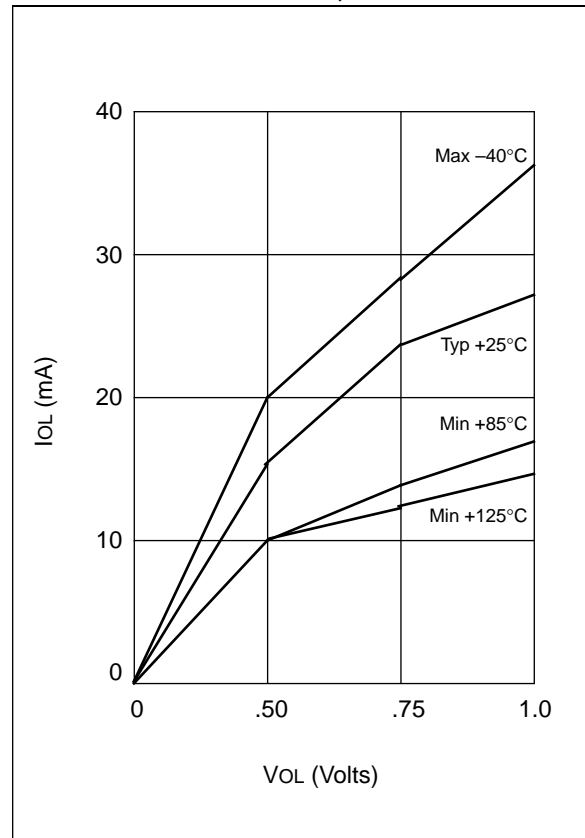


FIGURE 13-7: I_{OL} vs. V_{OL} , $V_{DD} = 3.5$ V



PIC12CE67X

FIGURE 13-8: I_{OH} vs. V_{OH} , $V_{DD} = 5.5\text{ V}$

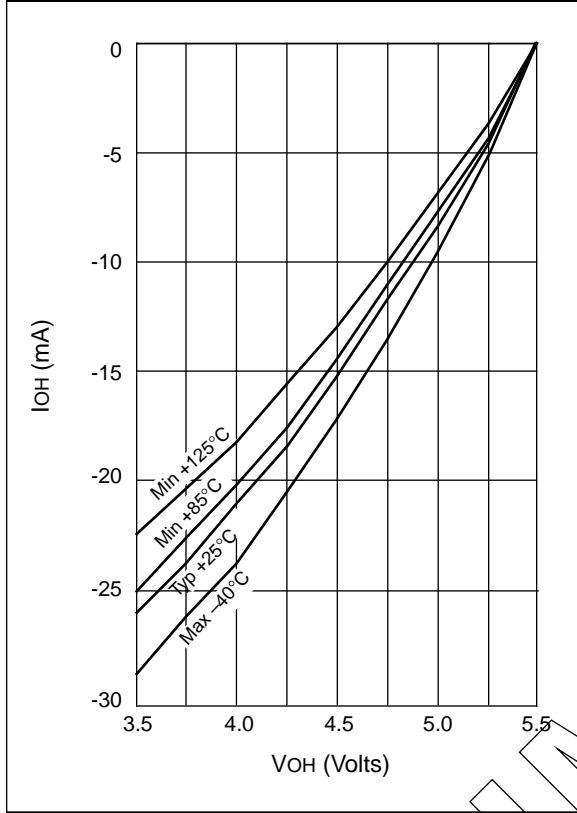
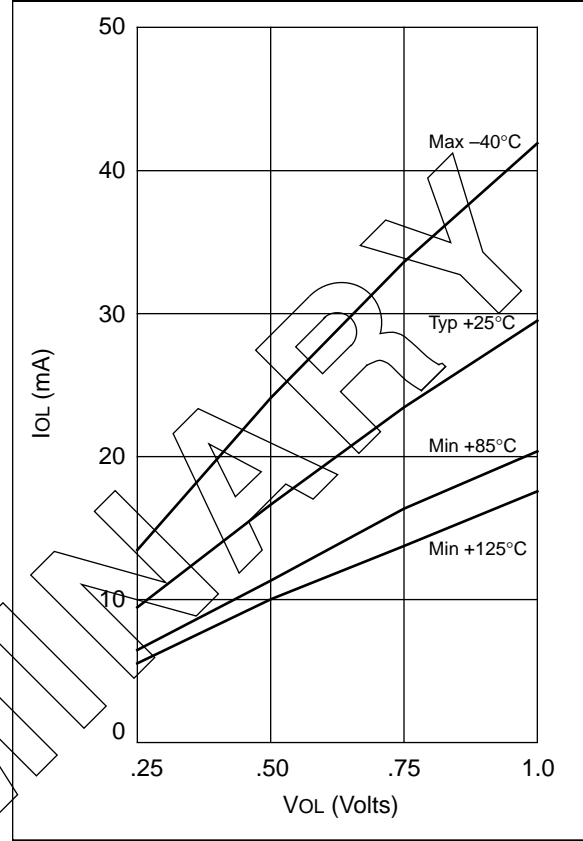


FIGURE 13-9: I_{OL} vs. V_{OL} , $V_{DD} = 5.5\text{ V}$



PRELIMINARY

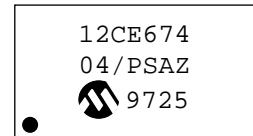
14.0 PACKAGING INFORMATION

14.1 Package Marking Information

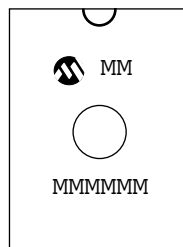
8-Lead PDIP (300 mil)



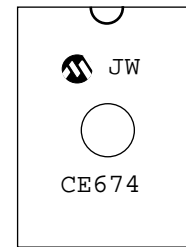
Example



8-Lead Windowed Ceramic Side Brazed (300 mil)



Example

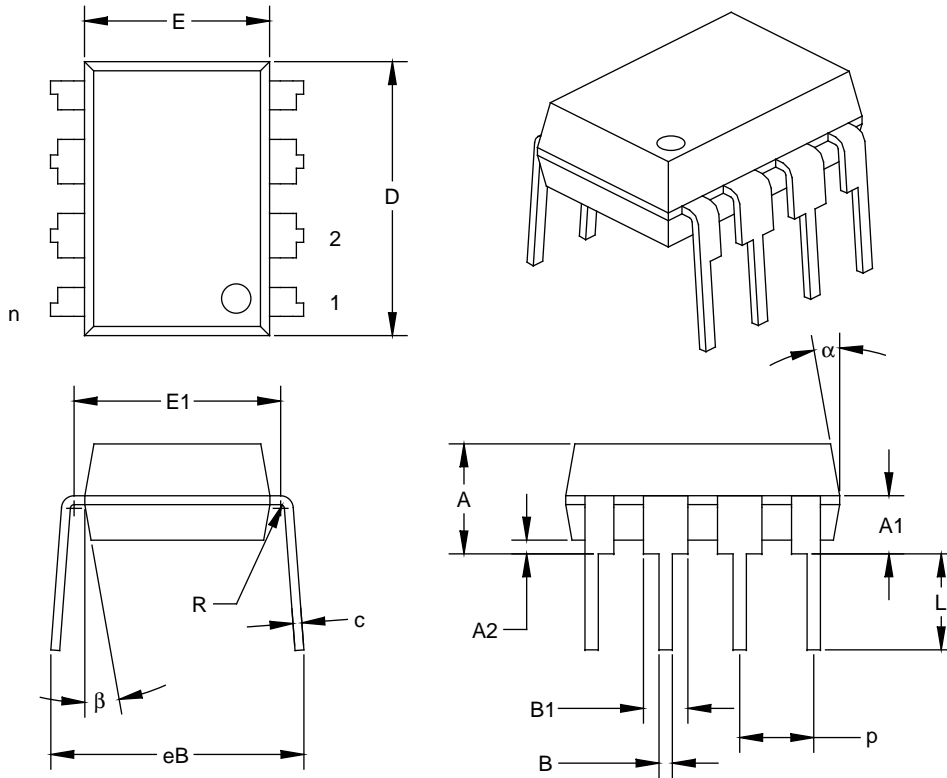


Legend:	MM...M	Microchip part number information
	XX...X	Customer specific information*
	AA	Year code (last 2 digits of calendar year)
	BB	Week code (week of January 1 is week '01')
	C	Facility code of the plant at which wafer is manufactured
		O = Outside Vendor
		C = 5" Line
		S = 6" Line
		H = 8" Line
	D	Mask revision number
	E	Assembly code of the plant or country of origin in which part was assembled
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.		

* Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

PIC12CE67X

Package Type: K04-018 8-Lead Plastic Dual In-line (P) – 300 mil



Units		INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Dimension Limits							
PCB Row Spacing			0.300			7.62	
Number of Pins	n		8			8	
Pitch	p		0.100			2.54	
Lower Lead Width	B	0.014	0.018	0.022	0.36	0.46	0.56
Upper Lead Width	B1 [†]	0.055	0.060	0.065	1.40	1.52	1.65
Shoulder Radius	R	0.000	0.005	0.010	0.00	0.13	0.25
Lead Thickness	c	0.006	0.012	0.015	0.20	0.29	0.38
Top to Seating Plane	A	0.140	0.150	0.160	3.56	3.81	4.06
Top of Lead to Seating Plane	A1	0.060	0.080	0.100	1.52	2.03	2.54
Base to Seating Plane	A2	0.005	0.020	0.035	0.13	0.51	0.89
Tip to Seating Plane	L	0.120	0.130	0.140	3.05	3.30	3.56
Package Length	D [‡]	0.355	0.370	0.385	9.02	9.40	9.78
Molded Package Width	E [‡]	0.245	0.250	0.260	6.22	6.35	6.60
Radius to Radius Width	E1	0.267	0.280	0.292	6.78	7.10	7.42
Overall Row Spacing	eB	0.310	0.342	0.380	7.87	8.67	9.65
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

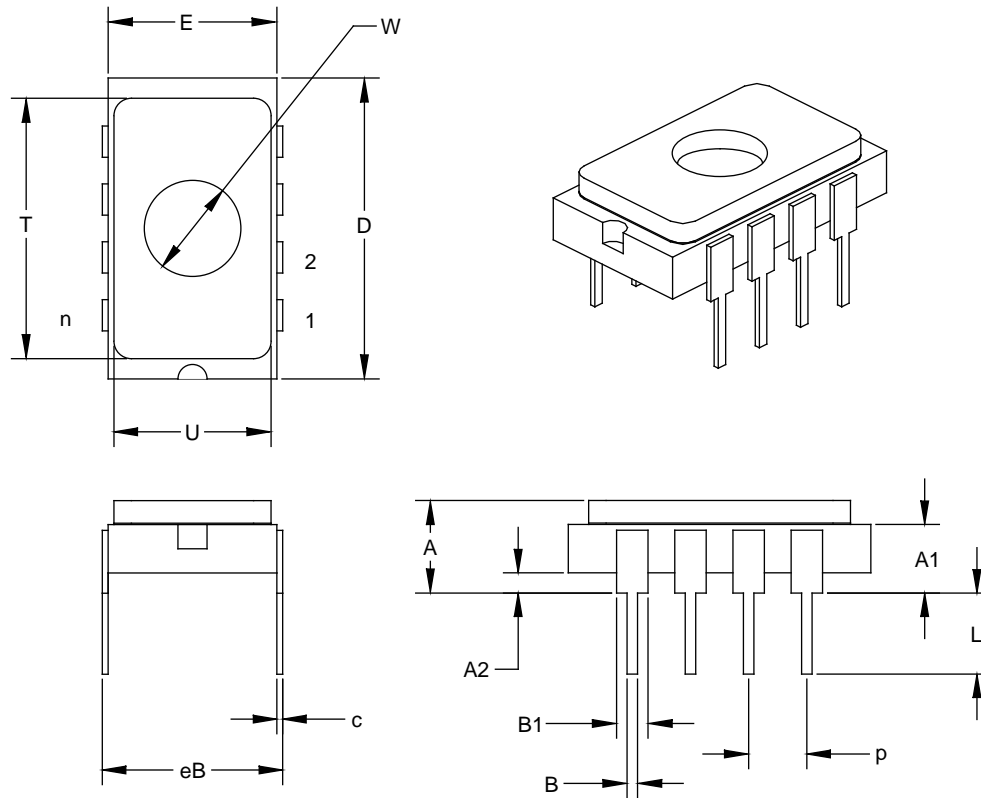
* Controlling Parameter.

[†] Dimension "B1" does not include dam-bar protrusions. Dam-bar protrusions shall not exceed 0.003" (0.076 mm) per side or 0.006" (0.152 mm) more than dimension "B1."

[‡] Dimensions "D" and "E" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.254 mm) per side or 0.020" (0.508 mm) more than dimensions "D" or "E."

PIC12CE67X

Package Type: K04-084 8-Lead Ceramic Side Brazed Dual In-line with Window (JW) – 300 mil



Units		INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Dimension Limits			0.300			7.62	
PCB Row Spacing			0.300			7.62	
Number of Pins	n		8			8	
Pitch	p	0.098	0.100	0.102	2.49	2.54	2.59
Lower Lead Width	B	0.016	0.018	0.020	0.41	0.46	0.51
Upper Lead Width	B1	0.050	0.055	0.060	1.27	1.40	1.52
Lead Thickness	c	0.008	0.010	0.012	0.20	0.25	0.30
Top to Seating Plane	A	0.145	0.165	0.185	3.68	4.19	4.70
Top of Body to Seating Plane	A1	0.103	0.123	0.143	2.62	3.12	3.63
Base to Seating Plane	A2	0.025	0.035	0.045	0.64	0.89	1.14
Tip to Seating Plane	L	0.130	0.140	0.150	3.30	3.56	3.81
Package Length	D	0.510	0.520	0.530	12.95	13.21	13.46
Package Width	E	0.280	0.290	0.300	7.11	7.37	7.62
Overall Row Spacing	eB	0.310	0.338	0.365	7.87	8.57	9.27
Window Diameter	W	0.161	0.166	0.171	4.09	4.22	4.34
Lid Length	T	0.440	0.450	0.460	11.18	11.43	11.68
Lid Width	U	0.260	0.270	0.280	6.60	6.86	7.11

* Controlling Parameter.

PIC12CE67X

NOTES:

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A

A/D

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