DMARD07 Low-g Tri-Axial Digital Accelerometer

General Description

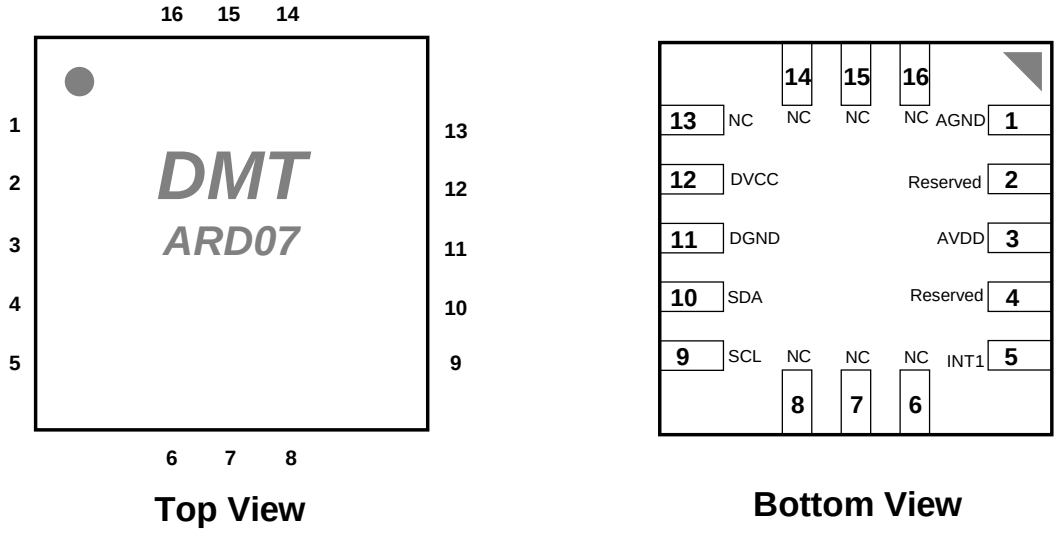
DMARD07 is a low-g tri-axial digital accelerometer of small 3×3×1 mm^3 form-factor with special power saving modes suitable for consumer mobile application. DMARD07 contains in a compact plastic LGA package a sensing element and a conditioning CMOS IC. The sensing element is a MEMS device by proprietary piezoresistive technology. The CMOS IC provides I2C digital interface and interrupt signals with build-in functionalities. DMARD07 can be deployed without further user interference in many applications.

Features

- Tri-axial digital accelerometer with selectable ±2/4/8g dynamic range
- Embedded 8 bit ADC, I2C digital interface, and temperature sensor for internal compensation
- Low operation voltage of +2.4V ~ +3.6V with minimum interface voltage of +1.7V
- Special low-power operation mode with current consumption below 30uA
- One interrupt pin configurable from two interrupt sources with high-G, freefall, and position change events
- User programmable thresholds and timing for interrupt event configurations
- Built-in high- and low-pass filter with user configurable cutoff frequency
- Auto-Awake function that auto-transit from low-power to normal mode upon interrupt events
- 5000g shock tolerance
- 16-pin LGA package with RoHS compliance and lead-free. Footprint 3mm×3mm, height 1mm.

Applications

Smart user interface, motion-enabled gaming, pedometer, and toys



Top View **Bottom View**

Figure 1: DMARD07

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Specifications

Table 1: Pin Descriptions

Pin	Name	Description	Pin	Name	Description
1	AGND	Analog ground	9	SCL	I2C serial clock
2	Reserved	Reserved	10	SDA	I2C serial data
3	AVDD	Analog power	11	DGND	Digital ground
4	Reserved	Reserved	12	DVCC	Digital power
5	INT1	Interrupt signal 1	13	NC	No connection inside
6	NC	No connection inside	14	NC	No connection inside
7	NC	No connection inside	15	NC	No connection inside
8	NC	No connection inside	16	NC	No connection inside

Table 2: General Specification

Operation voltage V_{op} = 3V, environment temperature T_a = 25℃ if not specified otherwise

Parameter	Conditions	Min.	Typ.	Max.	Unit
Operating Voltage V_{op} (AVDD)	T_a = -40℃ ~ +85℃	2.4	3.0	3.6	V
Interface Voltage DVCC	T_a = -40℃ ~ +85℃	1.7	—	3.6	V
Normal Operating current	Data rate = 342 Hz Data rate = 85 Hz Data rate = 42 Hz Data rate = 21 Hz	—	300 170 150 140	—	uA
Low Power Operating current	Data rate = 32 Hz Data rate = 16 Hz Data rate = 8 Hz Data rate = 4 Hz Data rate = 2 Hz	—	30 25 20 15 15	—	uA
Power down current		—	2	—	uA
Dynamic range		—	±2 ±4 ±8	—	g
Sensitivity	±2g ±4g ±8g	Typ.-10%	64 32 16	Typ.+10%	LSB/g

Zero-g offset, calibrated	±2g ±4g ±8g	—	±60	—	mg
Sensitivity to temp. dependency	T_a = -40℃ ~ +85℃	—	±5	—	%FS
Zero-g offset temp. dependency	T_a = -40℃ ~ +85℃	—	±3	—	%FS
Nonlinearity		—	±2	—	%FS
Cross axis sensitivity		—	2	—	%
Turn on time	From power down	—	—	1	ms
Noise	T_a = 25℃	—	1.1	—	mg/√Hz
Operation temperature T_a		-40	—	+85	℃
Storage temperature range		-40	—	+125	℃
Data Rate DR	Normal Mode (NMDR) Low-power Mode	342, 85, 42, 21 32, 16, 8, 4, 2			Hz
Bandwidth	Mechanical resonance	—	1000	—	Hz
	Digital filter	Table 9			Hz
Temperature sensor sensitivity		—	2	—	LSB/℃
Temperature sensor accuracy	T_a = -40℃ ~ +85℃	—	5	—	℃
Digital interface		I2C			
I2C clock frequency		—	—	400	kHz
Low level input voltage	DA, SCL, SDA, AZ	-0.3	—	$0.2\times V_{if}$	V
High level input voltage	DA, SCL, SDA, AZ	$0.8\times V_{if}$	—	$V_{if}+0.3$	V
Low level output voltage	SDA	—	—	$0.1\times V_{if}$	V
High level output voltage	SDA	$0.9\times V_{if}$	—	—	V

Maximum Ratings

Please note that stress above the absolute maximum rating as listed in Table 3 may cause permanent damage to the device. User precaution is advised.

Table 3: Absolute Maximum Rating

Parameter	Rating
V_{op}-GND	-0.3 ~ 4 V
Any other pin voltage	GND-0.3 to V_{op}+0.3 V
Temperature Range (Storage)	−40℃ to +125℃
ESD	2000V (HBM)

Mechanical Shock (unpowered)	5,000 g for 0.2ms
Freefall on concrete surface	1.5 m

Block Diagram and Connection Description

The block diagram of DMARD07 is shown in Figure 2. An I2C connection example is show in the Figure 3.

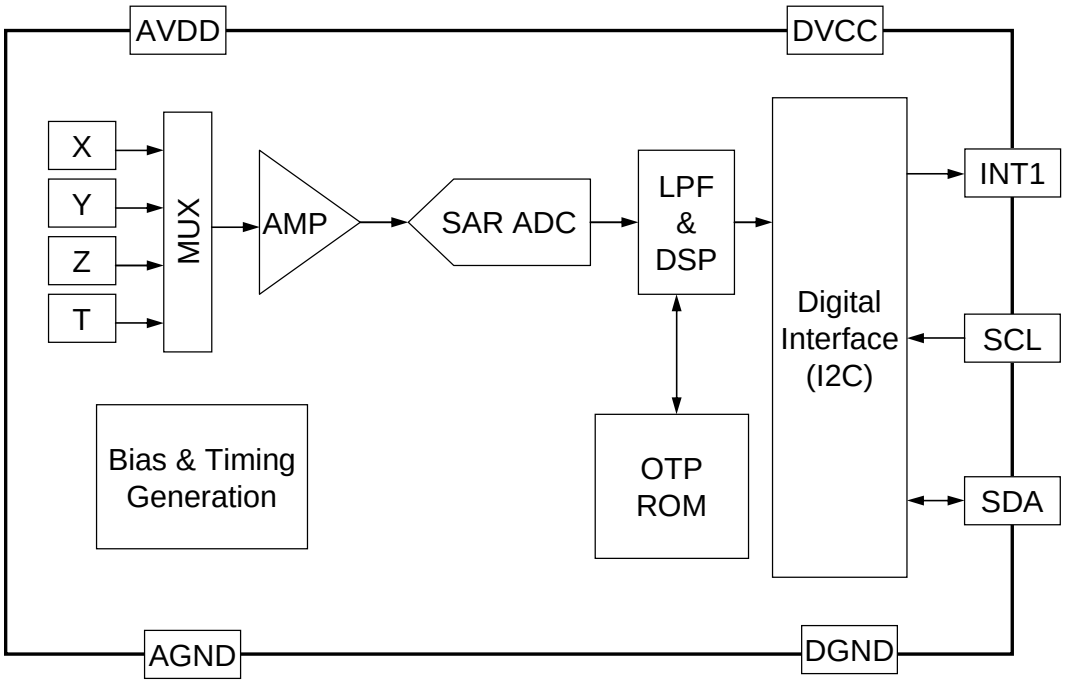


Figure 2: Block Diagram of DMARD07

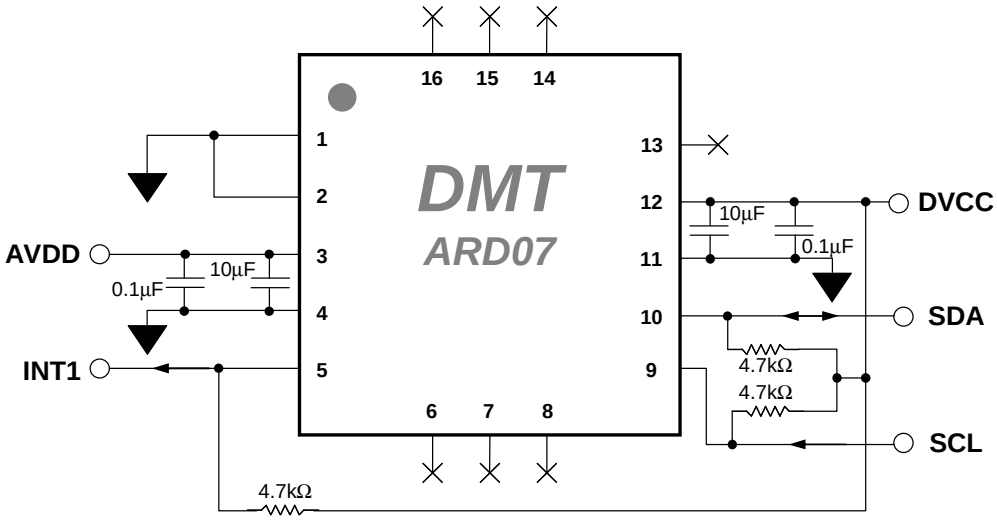


Figure 3: I2C Connection Example: pin#2 may optionally be left unconnected

User Registers

The overall internal registers of the DMARD07 are listed in Table 4: User Register Map. An attempt to access data from address marked with “Not used” is generally ignored. Please note registers marked with “Reserved” are reserved for internal purpose. Access to reserved registers may cause adverse abrupt to normal sensor operation. User precaution is advised.

User Register Map

Table 4: User Register Map Table

Register Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default Value
00h~0Eh	**Reserved**								—	—
0Fh	WHO_AM_I								R	07h
10h~16h	**Reserved**								—	—
17h~1Eh	Not used								—	—
1Fh~22h	**Reserved**								—	—
23h~3Fh	Not used								—	—
40h	TOUT								R	NA
41h	XOUT								R	NA
42h	YOUT								R	NA
43h	ZOUT								R	NA
44h	PM[2:0]			DR[1:0]		XEN	YEN	ZEN	RW	27h
45h	FS[1:0]		DFS[1:0]		I1FS[1:0]		I2FS[1:0]		RW	20h
46h	Not used					LPCF	HPCF[1:0]		RW	00h
47h	Not used	IHL	LIR1	LIR2	I1CFG[1:0]		**Reserved**		RW	00h
48h	Not used						TurnOn[1:0]		RW	00h
49h	XYZOR	XOR	YOR	ZOR	XYZDA	XDA	YDA	ZDA	R	NA
4Ah	I1AOI	I16D	I1XHIE	I1XLIE	I1YHIE	I1YLIE	I1ZHIE	I1ZLIE	RW	00h
4Bh	Not used	I1IA	I1XH	I1XL	I1YH	I1YL	I1ZH	I1ZL	R	NA
4Ch	Not used	I1THS[6:0]							RW	00h
4Dh	Not used	I1DUR[6:0]							RW	00h
4Eh	**Reserved**								—	—
4Fh	**Reserved**								—	—
50h	**Reserved**								—	—

51h	**Reserved**	—	—
52h	FILTER_RESET	R	NA
53h	SW_RESET	R	NA
54h~58h	**Reserved**	—	—
59h~7Fh	Not used	—	—
80h~82h	**Reserved**	—	—
83h~FFh	Not used	—	—

Description of Registers

WHO_AM_I: Device ID

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
0Fh	WHO_AM_I								R	07h

The WHO_AM_I register indicates the DMARD07 device ID. The value is fixed to 07h.

Data Registers: TOUT, XOUT, YOUT, ZOUT

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
40h	TOUT								R	NA
41h	XOUT								R	NA
42h	YOUT								R	NA
43h	ZOUT								R	NA

Temperature and acceleration output values can be read from the data registers. The sensor output is encoded to an 8-bit value and stored to respective register bytes. Data representation is 2's complement, i.e. MSB (bit7) is the sign bit with 1 represents negative value. Data is periodically updated according to user-settable sampling period. Data registers are protected from updating when user is accessing the data via the I2C digital interface.

A thermometer is embedded in DMARD07. The temperature sensitivity is 2 LSB/℃ and the central value (00h) stands for 25℃. For example a TOUT[7:0] reading of 10h means temperature to be 25+10h/2=33℃.

The acceleration sensing has three user-selectable sensitivity of 64/32/16 LSB/g with full measurable range of ±2/4/8g respectively. The central value (00h) stands for 0g. For example a XOUT[7:0] reading of 20h when sensitivity is set to 32 LSB/g means the acceleration to be 20h/32=1g.

Control Register 1: PM, DR, XEN, YEN, ZEN

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
44h	PM[2:0]			DR[1:0]		XEN	YEN	ZEN	RW	27h

DMARD07 provides a special low-power mode to increase battery time for mobile application. User can operate the sensor in one of the low-power modes by properly setting the power mode bits PM[2:0], Table 5. The sensing frequency is put to a slow rate for power saving. If desired, user may optionally configure the sensor to automatically restore to normal mode operation when designated interrupt event occurred.

DMARD07 will operate in normal mode when PM[2:0] is set to 1. The normal mode data rate can be further configured by the Normal Mode Data Rate (NMDR) bits DR[1:0], Table 6. Maximum data rate is 342 Hz.

DMARD07 can be put in power down mode when PM[2:0] is set to 0. The sensor is dormant, but the digital interface will still be alive. The registers values are kept so long as the power is connected.

Table 5: Power Mode

PM[2]	PM[1]	PM[0]	Power Mode	Data Rate (Hz)
0	0	0	Power down	NA
0	0	1	Normal	NMDR, Table 6
0	1	0	Low power	32
0	1	1	Low power	16
1	0	0	Low power	8
1	0	1	Low power	4
1	1	0	Low power	2
1	1	1	Reserved	NA

Table 6: Normal Mode Data Rate (NMDR)

DR[1]	DR[0]	NMDR (Hz)
0	0	342
0	1	85
1	0	42
1	1	21

XEN, YEN and ZEN are the global interrupt enable bits. They control the global interrupt enabling along respective X, Y, and Z axes. Set to 1 will make further interrupt setting effective. Otherwise any further interrupt setting will be ignored along the said axis.

Control Register 2: FS, DFS, I1FS, I2FS

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
45h	FS[1:0]		DFS[1:0]		I1FS[1:0]		I2FS[1:0]		RW	20h

User can configure DMARD07 to one of the three dynamic ranges of ±2/4/8g by setting FS[1:0] bits, Table 7. Because the ADC resolution is fixed at 8-bit, the dynamic range setting is inversely proportional to the available sensor sensitivity as shown in the Table 7. In general if user requires higher resolution then the full scale will be smaller, and vice versa.

Table 7: Full Scale Dynamic Range and Sensitivity Selection

FS[1]	FS[0]	Full Scale Dynamic Range (g)	Sensitivity (LSB/g)
0	0	±2	64
0	1	±4	32
1	0	Reserved	Reserved

1	1	±8	16

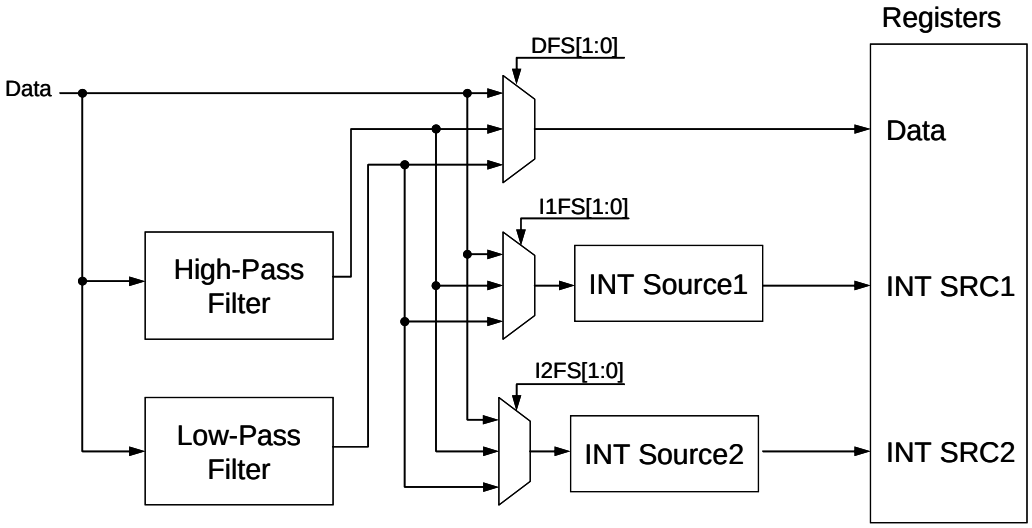
Additionally user may be interested in further conditioning the measurement prior output. DMARD07 provides two built-in simple filters to suit user's purpose. User can selectively add high- or low-pass filter to the signal path by properly setting DFS[1:0], I1FS[1:0], and I2FS[1:0], Table 8. DFS, I1FS and I2FS works on different signal path respectively, that is data, INT Source 1, and INT Source 2 signal path, Figure 4. Despite that, they function in identical way. The filter cutoff frequency can be further configured. Please refer to "Control Register 3" for more information.

Table 8: Filter Selection

*x*FS[1]	*x*FS[0]	Filter Mode
0	0	No filter
0	1	High-pass Filter
1	0	Low-pass Filter
1	1	Reserved

Note: *x* stand for D, I1 or I2. For example when *x* = I1, *x*FS = I1FS

Figure 4: Filter Selection Block Diagram



Control Register 3: LPCF, HPCF

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
46h	Not used					LPCF	HPCF[1:0]		RW	00h

User can configure the built-in high- and low-pass filter cutoff frequency by setting the LPCF and HPCF bits accordingly, Table 9 and Table 10. User need to select desired filter along targeted signal path to make such filtered signal available. Please refer to "Control Register 2" for filter selection configuration.

Table 9: Low-pass Filter Cutoff Frequency Configuration

LPCF	NMDR 21Hz	NMDR 42Hz	NMDR 85Hz	NMDR 342Hz

0	0.47 Hz	0.94 Hz	1.88 Hz	7.5 Hz
1	0.94 Hz	1.88 Hz	3.75 Hz	15 Hz

Table 10: High-pass Filter Cutoff Frequency Configuration

HPCF[1]	HPCF[0]	NMDR 21Hz	NMDR 42Hz	NMDR 85Hz	NMDR 342Hz
0	0	0.4 Hz	0.8 Hz	1.6 Hz	6.4 Hz
0	1	0.2 Hz	0.4 Hz	0.8 Hz	3.2 Hz
1	0	0.1 Hz	0.2 Hz	0.4 Hz	1.6 Hz
1	1	0.05 Hz	0.1 Hz	0.2 Hz	0.8 Hz

Control Register 4: IHL, LIR1, LIR2, I1CFG

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
47h	Not used	IHL	LIR1	LIR2	I1CFG[1:0]		**Reserved**		RW	00h

DMARD07 has one interrupt output pin, INT1, which can be configured to source from two interrupt sources, INT SRC1 and INT SRC2, by setting I1CFG bits, Table 11. The block diagram of interrupt source loop for INT1 pin is shown in Figure 5. Every interrupt source can be further configured to detect high-G, freefall, position change, or combination. See “Interrupt Source Configuration Registers” for details.

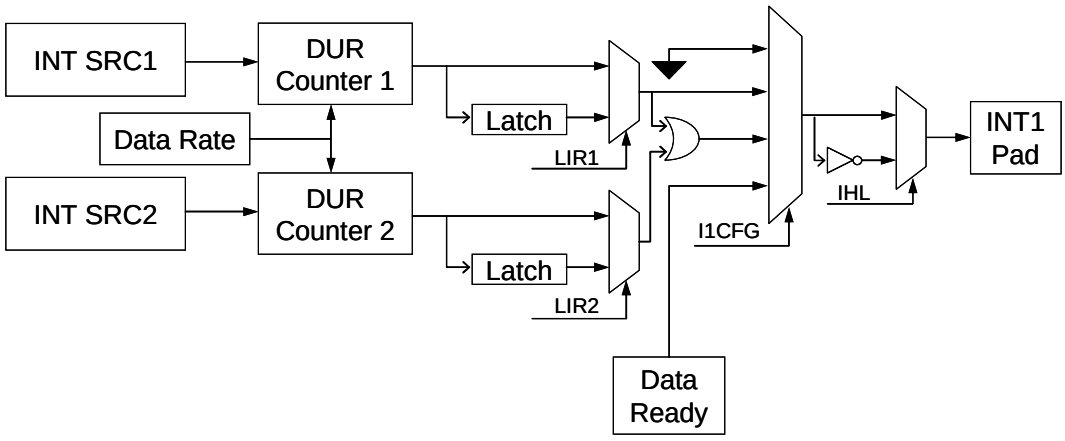
The interrupt source loop has the following additional options:

- IHL: define the interrupt signal active level. 0 (default): active low; 1: active high.
- LIR1/2: interrupt signal latch selection. 0 (default): latch disabled; 1: latch enabled.

Table 11: INT1 Pin Interrupt Source Loop Configuration

I1CFG[1]	I1CFG[0]	INT1 Pin Interrupt Source
0	0	Ground
0	1	INT SRC1
1	0	INT SRC1 + INT SRC2
1	1	Data Ready

Figure 5: INT1 Interrupt Source Loop Block Diagram



Control Register 5: TurnOn

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
48h	Not used						TurnOn[1:0]		RW	00h

DMARD07 has a special Auto-Awake mode that balances the power saving and fast response time. When the Auto-Awake function is activated, DMARD07 is first put to a low-power mode for power saving, while continuing sensing at a slow data rate and capable of generating interrupts. As soon as the appropriate interrupt event has been detected, DMARD07 automatically wake up to the normal mode with fast output data rate. This Auto-Wake feature enables DMARD07 to automatically transit from low-power mode to normal mode upon user-selectable posture or acceleration events.

To activate the Auto-Awake function, TurnOn[1:0] bits need to be set to 11b, Table 12. The device will be sensing at low-power mode data rate configured by “Control Register 1”, Table 5. When an intended event is detected and interrupt generated, the device will do auto-awake by automatically transiting from the low-power mode to the normal mode, with the normal mode data rate configured by “Control Register 1”, Table 6. The TurnOn bits are then set to 01b to indicate the Auto-Awake completion. To return to normal mode or low-power mode, the TurnOn bits should be set back to 00b.

Table 12: Low-power to Normal Mode Auto-Awake Configuration

TurnOn[1]	TurnOn[0]	Sleep to wake status
0	0	Auto-Awake function disabled
0	1	Device Auto-Awake done
1	0	Reserved
1	1	Auto-Awake function enabled

Status Register: XYZOR, XOR, YOR, ZOR, XYZDA, XDA, YDA, ZDA

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
49h	XYZOR	XOR	YOR	ZOR	XYZDA	XDA	YDA	ZDA	R	NA

Status register provides information on measurement data overrun and data availability. See Table 13 for details.

An overrun marks the situation when the new sensing data has been written to the data register before the previous one being read by the user.

Table 13: Status Register Bit Description

XYZOR	X-, Y- and Z-axis data overrun, default 0 0: no overrun 1: overrun occurs at either X-, Y-, or Z-axis
XOR	X-axis data overrun, default 0 0: no overrun 1: overrun occurs at X-axis
YOR	Y-axis data overrun, default 0 0: no overrun 1: overrun occurs at Y-axis

ZOR	Z-axis data overrun, default 0 0: no overrun 1: overrun occurs at Z-axis
XYZDA	X-, Y- and Z-axis data availability, default 0 0: data not available at either X-, Y-, or Z-axis 1: data available at X-, Y-, and Z-axis
XDA	X-axis data availability, default 0 0: data not available 1: data available at X-axis
YDA	Y-axis data availability, default 0 0: data not available 1: data available at Y-axis
ZDA	Z-axis data availability, default 0 0: data not available 1: data available at Z-axis

INT SRC1 Configure Register: I1AOI, I16D, I1XHIE, I1YHIE, I1YLIE, I1ZHIE, I1ZLIE

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
4Ah	I1AOI	I16D	I1XHIE	I1XLIE	I1YHIE	I1YLIE	I1ZHIE	I1ZLIE	RW	00h

INT SRC1 provides several interrupt events that can be configured by INT SRC1 Configure Register. There are three basic interrupt events: high-G, low-G (freefall), and position change that user may selectively activate and combine if necessary. The threshold and duration can be further configured by the INT SRC1 Threshold and Duration Registers.

A high-G event is called when the absolute acceleration value exceeds some threshold value for some minimum duration. On the other hand, a low-G (freefall) event is called when the absolute acceleration value fall within some threshold value for some minimum duration. A position change event is called when the device moves from one position to a different position.

The position change detection can be activated by setting I16D bit to 1. High- or low-G detection can be activated by setting I16D bit to 0. Additionally I1AOI controls the “OR” or “AND” combination of all turn-on’ed high-/low-G events from all axes. See Table 14 for details.

The high-/low-G interrupt events along each axis can be individually controlled as shown in Table 15.

Table 14: INT SRC1 Configuration

I1AOI	I16D	Interrupt Mode
0	0	OR all interrupt events
0	1	6D movement detection
1	0	AND all interrupt events
1	1	6D position detection

Table 15: INT SRC1 Interrupt Event Configuration

I1XHIE	X-axis high-G event interrupt enabling, default 0 0: disable 1: enable
I1XLIE	X-axis low-G (freefall) event interrupt enabling, default 0 0: disable 1: enable
I1YHIE	Y-axis high-G event interrupt enabling, default 0 0: disable 1: enable
I1YLIE	Y-axis low-G (freefall) event interrupt enabling, default 0 0: disable 1: enable
I1ZHIE	Z-axis high-G event interrupt enabling, default 0 0: disable 1: enable
I1ZLIE	Z-axis low-G (freefall) event interrupt enabling, default 0 0: disable 1: enable

INT SRC1 Status Register: I1IA, I1XH, I1XL, I1YH, I1YL, I1ZH, I1ZL

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
4Bh	Not used	I1IA	I1XH	I1XL	I1YH	I1YL	I1ZH	I1ZL	R	NA

INT SRC1 interrupt status is recorded in this register as shown in the Table 16.

Table 16: INT SRC1 Status Registe Bit Description

I1IA	Overall interrupt status, default 0 0: no interrupt generated 1: at least one interrupt generated
I1XH	X-axis high-G interrupt status, default 0 0: no interrupt generated 1: interrupt generated
I1XL	X-axis low-G interrupt status, default 0 0: no interrupt generated 1: interrupt generated
I1YH	Y-axis high-G interrupt status, default 0 0: no interrupt generated 1: interrupt generated
I1YL	Y-axis low-G interrupt status, default 0 0: no interrupt generated

	1: interrupt generated
I1ZH	Z-axis high-G interrupt status, default 0 0: no interrupt generated 1: interrupt generated
I1ZL	Z-axis low-G interrupt status, default 0 0: no interrupt generated 1: interrupt generated

INT SRC1 Threshold Register: I1THS

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
4Ch	Not used	I1THS[6:0]							RW	00h

The acceleration threshold value for INT SRC1 interrupt events can be set by the I1THS bits. The threshold resolution will depend on the dynamic range. In general, under ±r g dynamic range operation, the acceleration threshold resolution can be calculated by r×7.87 mg, as illustrated below.

- ±2g dynamic range: one code ~ 15.7 mg
- ±4g dynamic range: one code ~ 31.5 mg
- ±8g dynamic range: one code ~ 63 mg

INT SRC1 Duration Register: I1DUR

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
4Dh	Not used	I1DUR[6:0]							RW	00h

The time duration value for INT SRC1 interrupt events can be set by the I1DUR bits. The time duration resolution will depend on the data rate. In general, under ±d Hz data rate operation, the time duration resolution can be calculated by 1000/d ms, as illustrated below for the normal mode data rate.

- NMDR 342 Hz: one code ~ 2.9 ms
- NMDR 85 Hz: one code ~ 11.8 ms
- NMDR 42 Hz: one code ~ 23.8 ms
- NMDR 21 Hz: one code ~ 47.6 ms

Filter Reset Register: FILTER_RESET

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
52h	FILTER_RESET								R	NA

By reading FILTER_RESET register, DMARD07 will clear out the prior state memory of embedded high- and low-pass filters.

Soft Reset Register: SW_RESET

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Type	Default
53h	SW_RESET								R	NA

By reading SW_RESET register, DMARD07 will carry out circuitry initialization and restore all registers to default values.

Digital Interface

DMARD07 provides I2C digital interface for easy device configuration and data/status query. The digital interface can be used to regularly read the data registers of acceleration and temperature output. The DMARD07 can also be configured by setting up proper control registers via the digital interface. For example, the interrupt pin can be configured to response to freefall or click event. Upon triggered interrupt, user can use the digital interface to check the interrupt status register for proper interrupt source verification.

I2C Interface

DMARD07 includes a slave I2C interface. The I2C bus takes master clock through SCL pin and exchanges serial data via SDA. SDA is bidirectional (input/output) with open drain. It must be connected externally to DVCC via a pull-up resistor.

I2C Slave Address

DMARD07 has a 7-bit slave address fixed at 1Ch. Additional RW bit sets the chip in read or write mode, RW = 0 for write and 1 for read. Table 17 summaries the I2C slave address and RW.

Table 17: I2C slave address & RW

Slave Address							bit0 (RW)	Hex	Read/Write
bit7	bit6	bit5	Bit4	bit3	bit2	bit1			
0	0	1	1	1	0	0	0	38h	Write
							1	39h	Read

I2C Access Format

Data transfer begins by bus master indicating a start condition (ST) of a falling edge on SDA when SCL is high. Stop condition (SP) also indicated by bus master is a rising edge on SDA when SCL is high.

After a start condition, the slave address + RW bit must be sent by master. If the slave address does not match with DMARD07, there is no acknowledge and the following data transfer will not affect DMARD07. If the slave address corresponds to DMARD07, it will acknowledge by pulling SDA to low and the SDA line is let free enabling the data transfer. The master should let the SDA high (no pull down) and generate a high SCL pulse for DMARD07 acknowledge.

Table 18: I2C access format

Single Write

ST	Slave Address + RW	A	Reg Address	A	Data	A	SP

Multiple Write

ST	Slave Address + RW	A	Reg Address	A	Data	A	Data	NA	SP

Single Read

ST	Slave Address + RW	A	Reg Address	A	SR	Slave Address + RW	A
Data	NA	SP					

Multiple Read

ST	Slave Address + RW	A	Reg Address	A	SR	Slave Address + RW	A
Data	A	Data	NA	SP			

Master to Slave

Slave to Master

A = acknowledge (SDA Low)
NA = not acknowledge (SDA High)
ST = START condition
SR = repeated START condition
SP = STOP condition

I2C Specifications

Table 19: I2C Timing Specification

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SCL clock frequency	SCL	—	—	400	kHz
Clock low period	t_{LOW}	1.2	—	—	us
Clock high period	t_{HIGH}	0.6	—	—	us
Bus free to new start	t_{BUF}	1.2	—	—	us
Start hold time	$t_{HD.STA}$	0.6	—	—	us
Start setup time	$t_{SU.STA}$	0.6	—	—	us
Data-in hold time	$t_{HD.DAT}$	0	—	—	us
Data-in setup time	$t_{SU.DAT}$	100	—	—	us
Stop setup time	$t_{SU.STO}$	0.6	—	—	us
Data-out hold time	t_{DH}	50	—	—	us

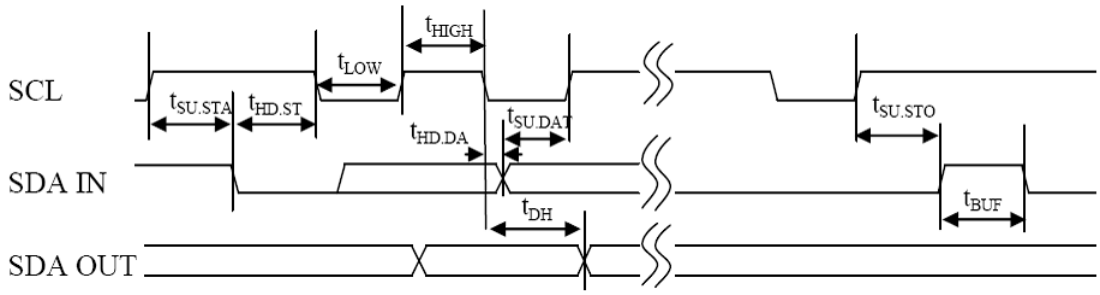


Figure 6: I2C Timing Diagram

Package

Outline Dimension

Unit: mm

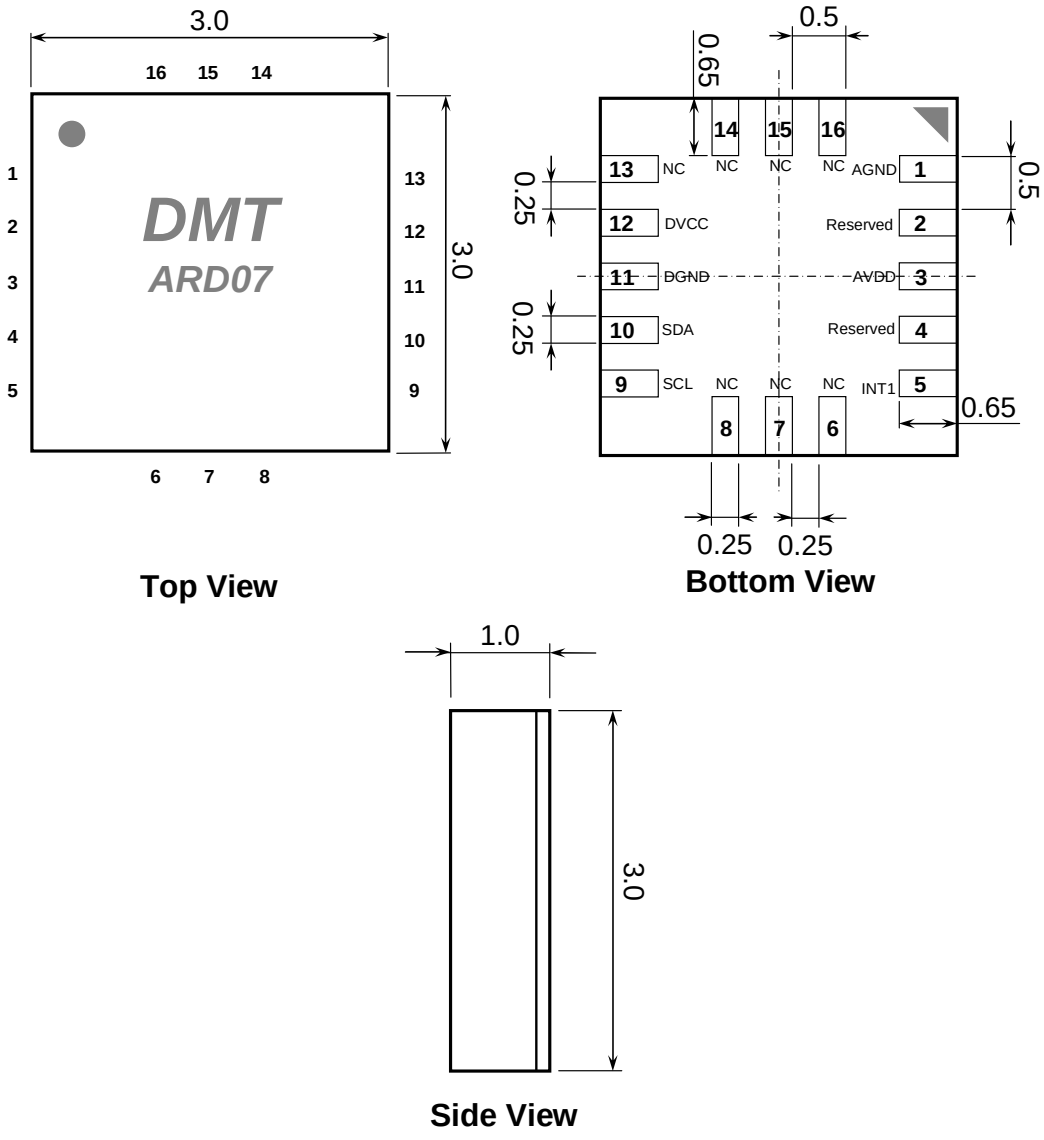


Figure 7: Package Outline Dimension

Axes Orientation

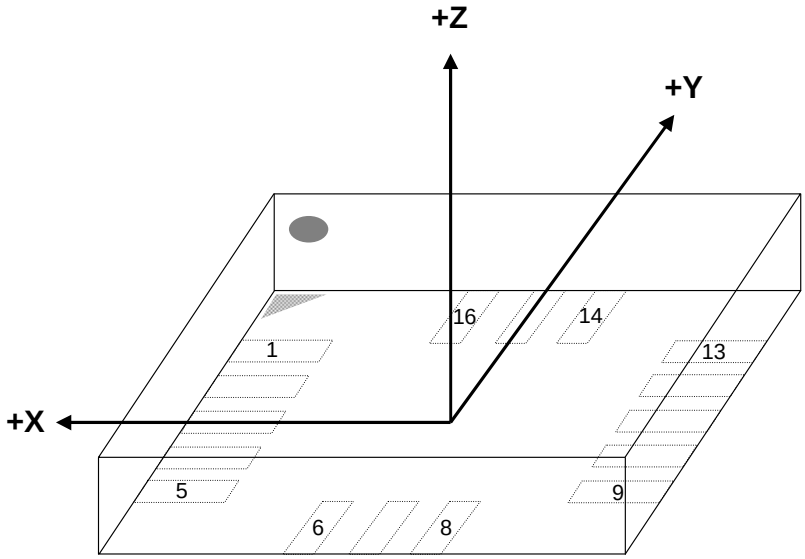


Figure 8: Axes Orientation of DMARD07

RoHS Compliance

The 16-pin LGA package conforms to the EU directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment 2002/95/EC.

Surface Mounting Information

The accelerometer is a delicate device that is sensitive to the mechanical and thermal stress. Proper PCB board design and well-executed soldering processes are crucial to ensure consistent performance. A recommended land pad layout can be found in the Figure 9. For more SMT information, please refer to application note “AN004: SMT Guide for Accelerometer in LGA Package”.

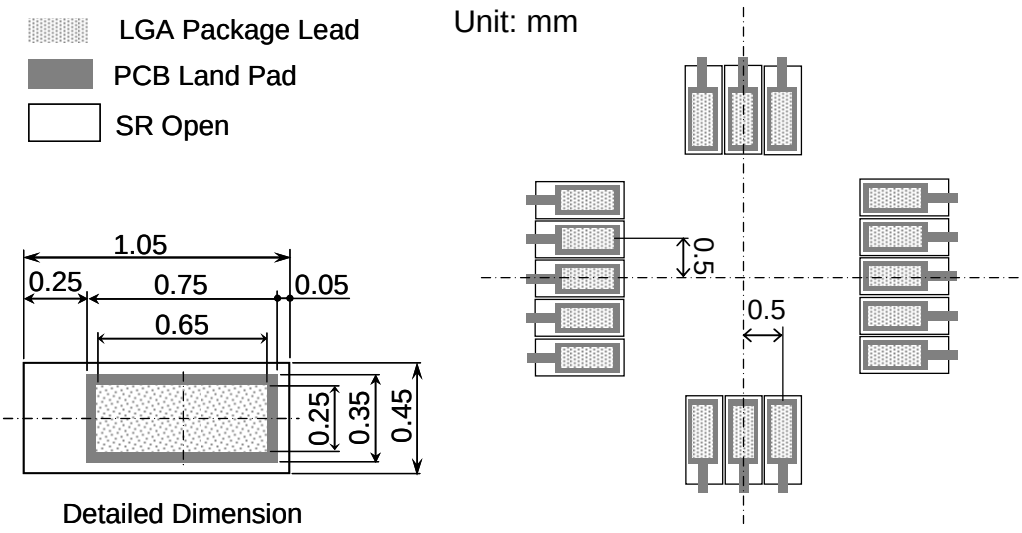


Figure 9: Layout Recommendation for PCB Land Pad and SR Open