DATA SHEET

MOS FIELD EFFECT POWER TRANSISTORS

2SJ494

SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

This product is P-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super Low On-State Resistance
  $R_{DS(on)1}$ = 50 mΩ Max. (V_{GS} = –10 V, I_D = –10 A)
  $R_{DS(on)2}$ = 88 mΩ Max. (V_{GS} = –4 V, I_D = –10 A)
- Low C_{iss} C_{iss} = 2360 pF Typ.
- Built-in Gate Protection Diode

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

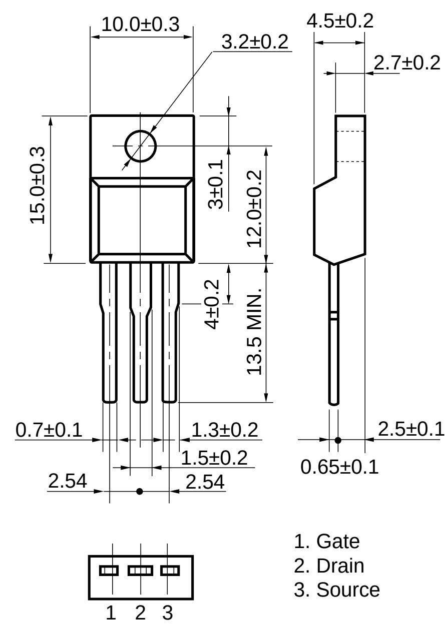
Drain to Source Voltage	V_{DSS}	–60	V
Gate to Source Voltage*	$V_{GSS (AC)}$	∓20	V
Gate to Source Voltage	$V_{GSS (DC)}$	–20, 0	V
Drain Current (DC)	$I_{D (DC)}$	∓20	A
Drain Current (pulse)**	$I_{D (pulse)}$	∓80	A
Total Power Dissipation (T_C = 25 °C)	P_T	35	W
Total Power Dissipation (T_A = 25 °C)	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

* f = 20 kHz, Duty Cycle ≤ 10% (+Side)
** PW ≤ 10 μs, Duty Cycle ≤ 1%

THERMAL RESISTANCE

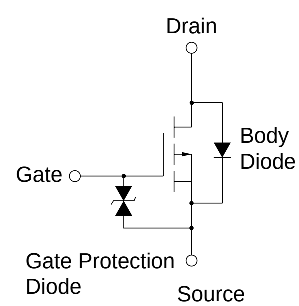
Channel to Case	$R_{th (ch-C)}$	3.57 °C/W
Channel to Ambient	$R_{th (ch-A)}$	62.5 °C/W

PACKAGE DIMENSIONS (in millimeter)



1. Gate
2. Drain
3. Source

ISOLATED TO-220 (MP-45F)



The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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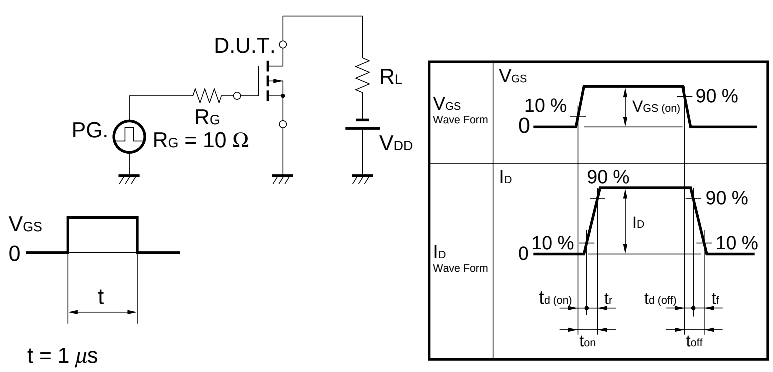
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

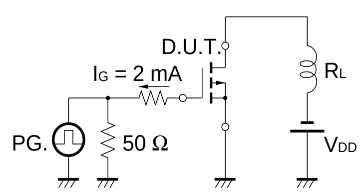
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –10 A		39	50	mΩ
	$R_{DS(on)2}$	V_{GS} = –4 V, I_D = –10 A		61	88	mΩ
Gate to Source Cutoff Voltage	$V_{GS\ (off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.0	–1.5	–2.0	V
Forward Transfer Admittance	$\lvert y_{fs} \rvert$	V_{DS} = –10 V, I_D = –10 A	8.0	15		S
Drain Leakage Current	I_{DSS}	V_{DS} = –60 V, V_{GS} = 0			–10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ∓20 V, V_{DS} = 0			∓10	μA
Input Capacitance	C_{iss}	V_{DS} = –10 V V_{GS} = 0 f = 1 MHz		2360		pF
Output Capacitance	C_{oss}			1060		pF
Reverse Transfer Capacitance	C_{rss}			350		pF
Turn-On Delay Time	$t_{d(on)}$	I_D = –10 A $V_{GS(on)}$ = –10 V V_{DD} = –30 V R_G = 10 Ω		25		ns
Rise Time	t_r			160		ns
Turn-Off Delay Time	$t_{d(off)}$			310		ns
Fall Time	t_f			240		ns
Total Gate Charge	Q_G	I_D = –20 A V_{DD} = –48 V V_{GS} = –10 V		74		nC
Gate to Source Charge	Q_{GS}			12		nC
Gate to Drain Charge	Q_{GD}			16		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 20 A, V_{GS} = 0		1.0	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 20 A, V_{GS} = 0 di/dt = 100 A/μs		130		ns
Reverse Recovery Charge	Q_{rr}			290		nC

Test Circuit 1 Switching Time

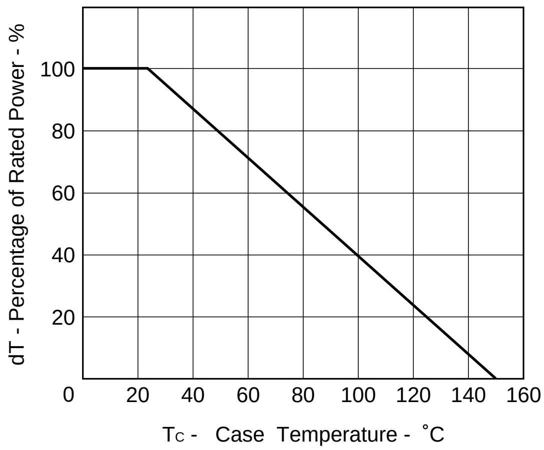


t = 1 μs
Duty Cycle ≤ 1 %

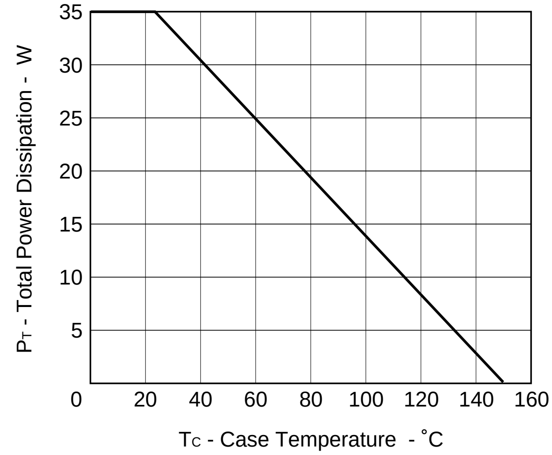
Test Circuit 2 Gate Charge



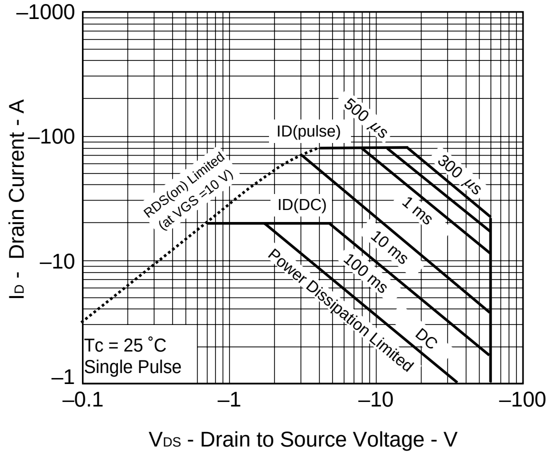
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



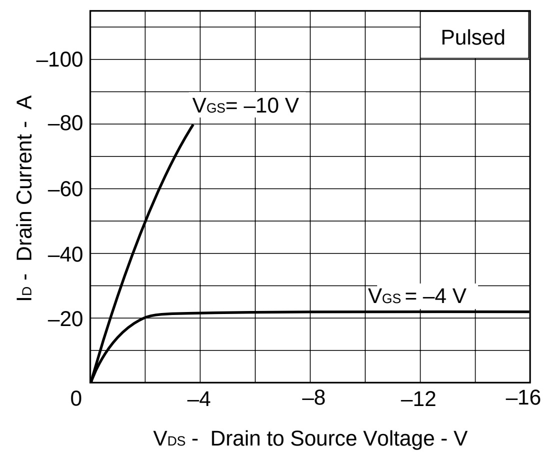
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



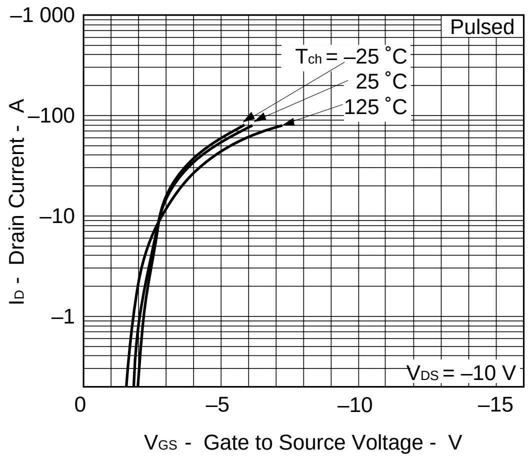
FORWARD BIAS SAFE OPERATING AREA



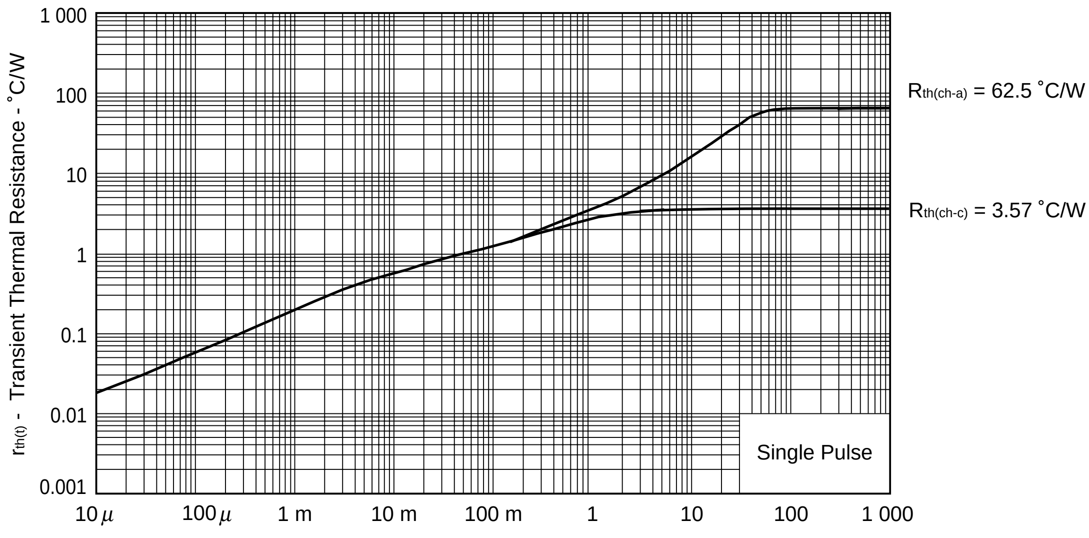
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



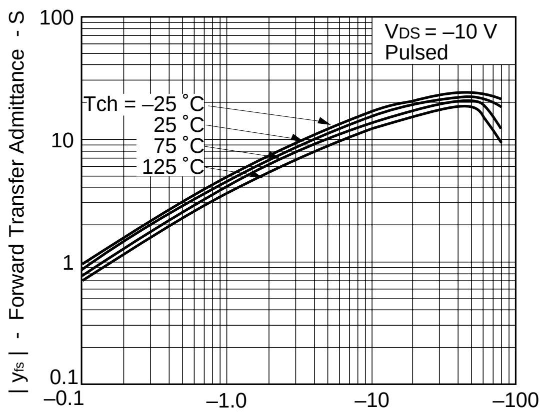
FORWARD TRANSFER CHARACTERISTICS



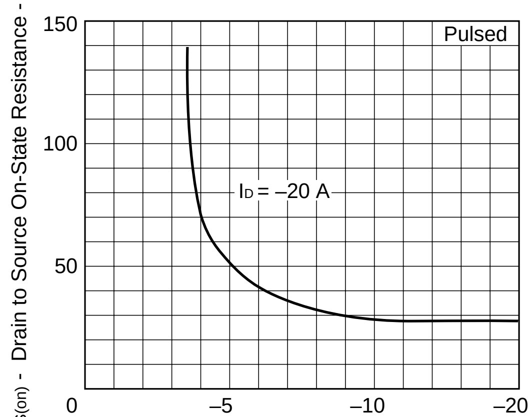
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



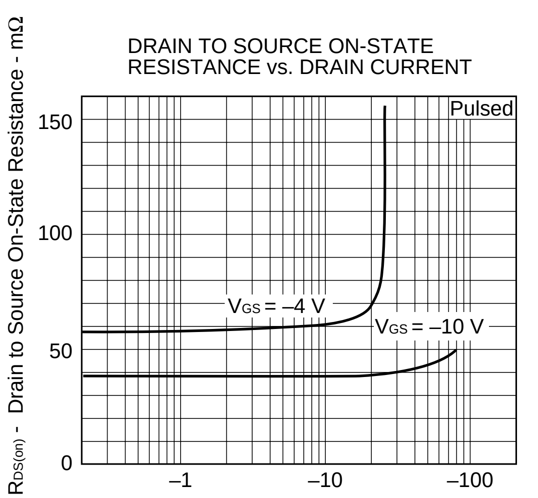
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



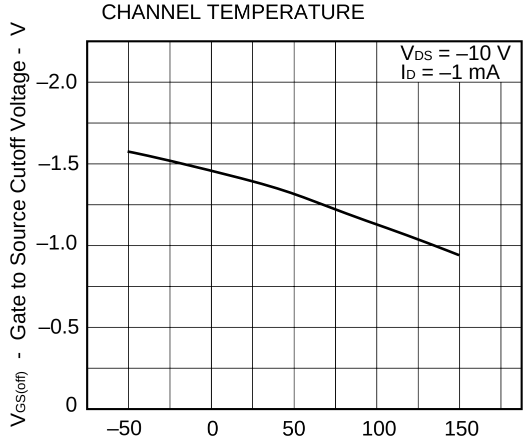
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

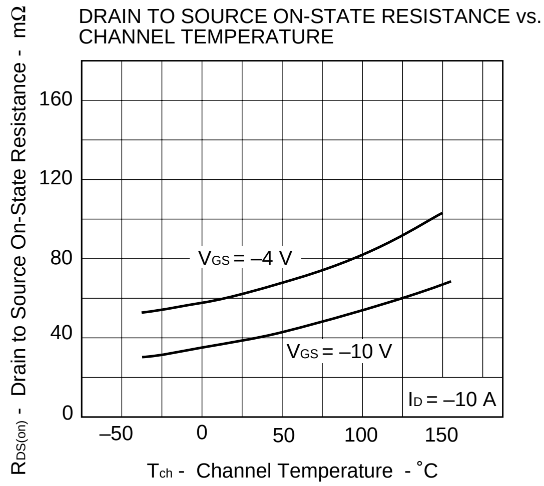


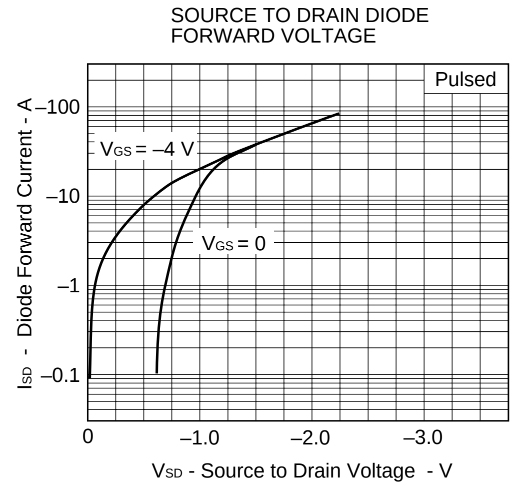
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

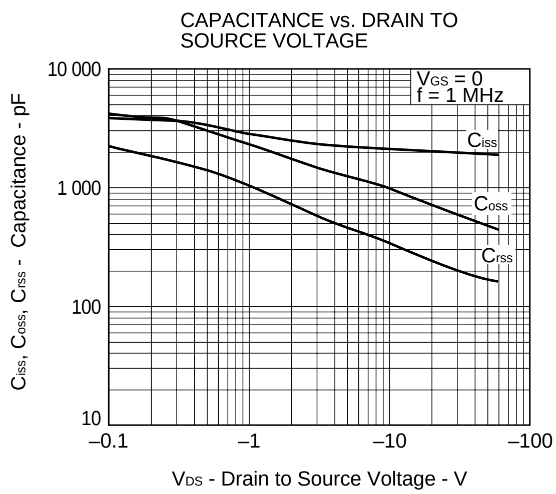


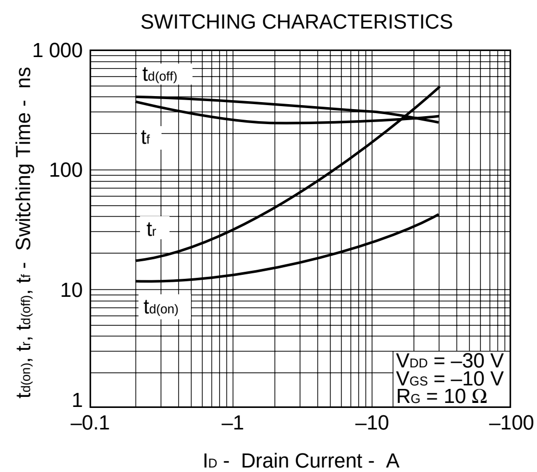
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

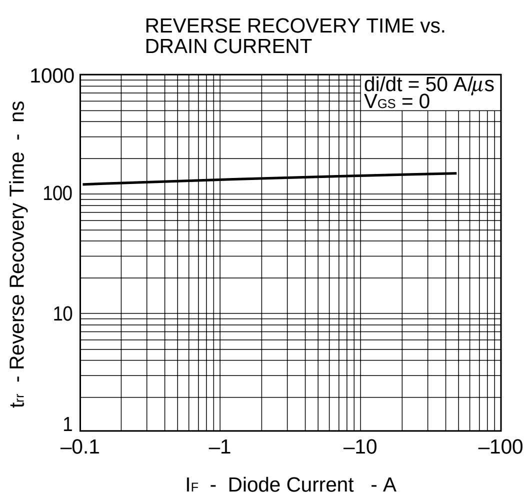


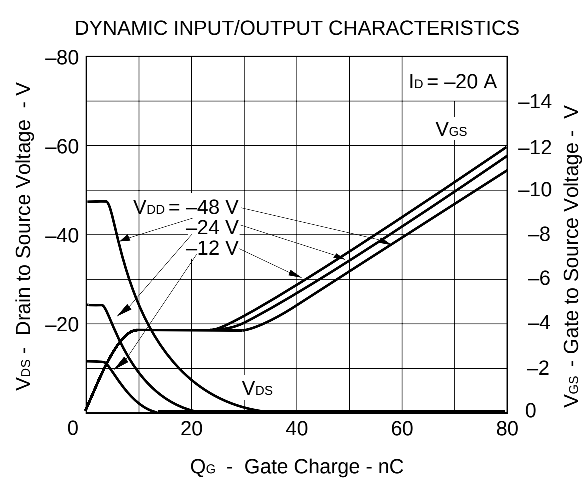

DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE
RDS(on) - Drain to Source On-State Resistance - mΩ
VGS = –4 V
VGS = –10 V
ID = –10 A
Tch - Channel Temperature - ˚C


SOURCE TO DRAIN DIODE
FORWARD VOLTAGE
Pulsed
ISD - Diode Forward Current - A
VGS = –4 V
VGS = 0
VSD - Source to Drain Voltage - V


CAPACITANCE vs. DRAIN TO
SOURCE VOLTAGE
VGS = 0
f = 1 MHz
Ciss
Coss
Crss
Ciss, Coss, Crss - Capacitance - pF
VDS - Drain to Source Voltage - V


SWITCHING CHARACTERISTICS
td(off)
tf
tr
td(on)
VDD = –30 V
VGS = –10 V
RG = 10 Ω
td(on), tr, td(off), tf - Switching Time - ns
ID - Drain Current - A


REVERSE RECOVERY TIME vs.
DRAIN CURRENT
di/dt = 50 A/μs
VGS = 0
trr - Reverse Recovery Time - ns
IF - Diode Current - A


DYNAMIC INPUT/OUTPUT CHARACTERISTICS
ID = –20 A
VGS
VDD = –48 V
–24 V
–12 V
VDS
VDS - Drain to Source Voltage - V
VGS - Gate to Source Voltage - V
QG - Gate Charge - nC

Document Name	Document No.
NEC semiconductor device reliability/quality control system	C11745E
Power MOS FET features and application to switching power supply	D12971E
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037
Guide to prevent damage for semiconductor devices by electrostatic discharge (EDS)	C11892E

[MEMO]