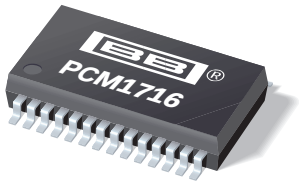
Not Recommended For New Design
捷多邦，您值得信赖的PCB打样专家！

BURR - BROWN®



PCM1716

SoundPLUS™ 24-Bit, 96kHz Sampling CMOS Delta-Sigma Stereo Audio DIGITAL-TO-ANALOG CONVERTER

FEATURES

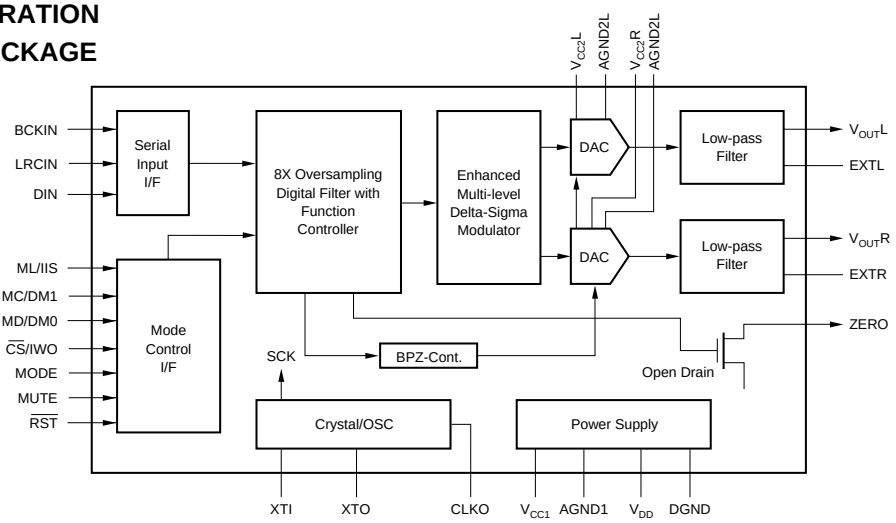
- ENHANCED MULTI-LEVEL DELTA-SIGMA DAC
- SAMPLING FREQUENCY (f_S): 16kHz - 96kHz
- INPUT AUDIO DATA WORD:
  16-, 20-, 24-Bit
- HIGH PERFORMANCE:
  THD+N: –96dB
  Dynamic Range: 106dB
  SNR: 106dB
  Analog Output Range: 0.62 x V_{CC} (Vp-p)
- 8x OVERSAMPLING DIGITAL FILTER:
  Stop Band Attenuation: –82dB
  Passband Ripple: ±0.002dB
  Slow Roll Off
- MULTI FUNCTIONS:
  Digital De-emphasis
  L/R Independent Digital Attenuation
  Soft Mute
  Zero Detect Mute
  Zero Flag
  Chip Select
  Reversible Output Phase
- +5V SINGLE SUPPLY OPERATION
- SMALL 28-LEAD SSOP PACKAGE

DESCRIPTION

The PCM1716 is designed for Mid to High grade Digital Audio applications which achieve 96kHz sampling rates with 24-bit audio data. PCM1716 uses a newly developed, enhanced multi-level delta-sigma modulator architecture that improves audio dynamic performance and reduces jitter sensitivity in actual applications.

The internal digital filter operates at 8x over sampling at a 96kHz sampling rate, with two kinds of roll-off performances that can be selected: sharp roll-off, or slow roll-off, as required for specific applications.

PCM1716 is suitable for Mid to High grade audio applications such as CD, DVD-Audio, and Music Instruments, since the device has superior audio dynamic performance, 24-bit resolution and 96kHz sampling.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

© 1997 Burr-Brown Corporation
PDS-1415C
Printed in U.S.A. August, 1998
SBAS080

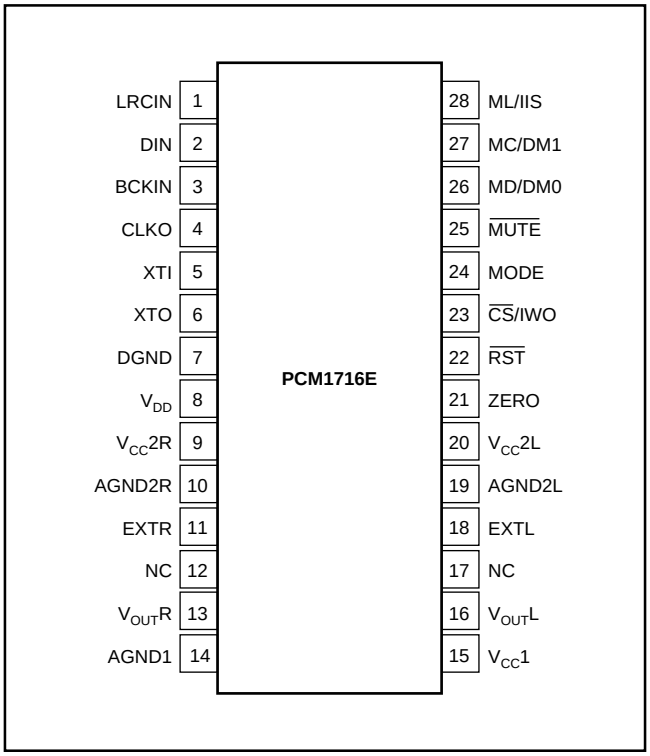
SPECIFICATIONS

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, and 24-bit input data, SYSCLK = 384f_S, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1716 MIN	PCM1716 TYP	PCM1716 MAX	UNITS
RESOLUTION			24		Bits
DATA FORMAT					
Audio Data Interface Format			Standard/I²S		
Data Bit Length			16/20/24 Selectable		
Audio Data Format			MSB First, 2's Comp		
Sampling Frequency (f_S)		16		96	kHz
System Clock Frequency(1)			256/384/512/768f_S		
DIGITAL INPUT/OUTPUT LOGIC LEVEL					
Input Logic Level V_{IH}		2.0			V
V_{IL}				0.8	V
Output Logic Level (CLKO) V_{OH}	I_{OH} = 2mA	4.5			V
V_{OL}	I_{OL} = 4mA			0.5	V
CLKO PERFORMANCE(2)					
Output Rise Time	20 ~ 80% V_{DD}, 10pF		5.5		ns
Output Fall Time	80 ~ 20% V_{DD}, 10pF		4		ns
Output Duty Cycle	10pF Load		37		%
DYNAMIC PERFORMANCE(3) (24-Bit Data)					
THD+N V_O = 0dB	f_S = 44.1kHz		–97	–90	dB
	f_S = 96kHz		–94		dB
V_O = –60dB	f_S = 44.1kHz		–42		dB
Dynamic Range	f_S =44.1kHz EIAJ A-weighted	98	106		dB
	f_S = 96kHz A-weighted		103		dB
Signal-to-Noise Ratio(4)	f_S =44.1kHz EIAJ A-weighted	98	106		dB
	f_S = 96kHz A-weighted		103		dB
Channel Separation	f_S = 44.1kHz	96	102		dB
	f_S = 96kHz		101		dB
DYNAMIC PERFORMANCE(3) (16-Bit Data)					
THD+N V_O = 0dB	f_S = 44.1kHz		–94		dB
	f_S = 96kHz		–92		dB
Dynamic Range	f_S = 44.1kHz EIAJ A-weighted		98		dB
	f_S = 96kHz A-weighted		97		dB
DC ACCURACY					
Gain Error			±1.0	±3.0	% of FSR
Gain Mismatch: Channel-to-Channel			±1.0	±3.0	% of FSR
Bipolar Zero Error	V_O = 0.5V_{CC} at Bipolar Zero		±30	±60	mV
ANALOG OUTPUT					
Output Voltage	Full Scale (0dB)		0.62 V_{CC}		Vp-p
Center Voltage			0.5 V_{CC}		V
Load Impedance	AC Load	5			kΩ
DIGITAL FILTER PERFORMANCE					
Filter Characteristics 1					
(Sharp Roll-Off)					
Passband	±0.002dB			0.454f_S	
	–3dB			0.490f_S	
Stopband		0.546f_S			
Passband Ripple				±0.002	dB
Stopband Attenuation	Stop Band = 0.546f_S	–75			dB
	Stop Band = 0.567f_S	–82			dB
Filter Characteristics 2					
(Slow Roll-Off)					
Passband	±0.002dB			0.274f_S	
	–3dB			0.454f_S	
Stopband		0.732f_S			
Passband Ripple				±0.002	dB
Stopband Attenuation	Stopband = 0.732f_S	–82			dB
Delay Time			30/f_S		sec
De-emphasis Error				±0.1	dB
INTERNAL ANALOG FILTER					
–3dB Bandwidth			100		kHz
Passband Response	f = 20kHz		–0.16		dB
POWER SUPPLY REQUIREMENTS					
Voltage Range	V_{DD}, V_{CC}	4.5	5	5.5	VDC
Supply Current: I_{CC} +I_{DD}	f_S = 44.1kHz		32	45	mA
	f_S = 96kHz		45		mA
Power Dissipation	f_S = 44.1kHz		160	225	mW
	f_S = 96kHz		225		mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+100	°C

NOTES: (1) Refer section of system clock. (2) External buffer is recommended. (3) Dynamic performance specs are tested with 20kHz low pass filter and THD+N specs are tested with 30kHz LPF, 400Hz HPF, Average Mode. (4) SNR is tested at internally infinity zero detection off.

PIN CONFIGURATION



PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM1716E	28-Pin SSOP	324

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	+6.5V
$+V_{CC}$ to $+V_{DD}$ Difference	±0.1V
Input Logic Voltage	–0.3V to (V_{DD} + 0.3V)
Input Current (except power supply)	±10mA
Power Dissipation	400mW
Operating Temperature Range	–25°C to +85°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 5s)	+260°C

PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	LRCIN	IN	Left and Right Clock Input. This clock is equal to the sampling rate - f_S.(1)
2	DIN	IN	Serial Audio Data Input(1)
3	BCKIN	IN	Bit Clock Input for Serial Audio Data.(1)
4	CLKO	OUT	Buffered Output of Oscillator. Equivalent to System Clock.
5	XTI	IN	Oscillator Input (External Clock Input)
6	XTO	OUT	Oscillator Output
7	DGND	—	Digital Ground
8	V_{DD}	—	Digital Power +5V
9	$V_{CC}2R$	—	Analog Power +5V
10	AGND2R	—	Analog Ground
11	EXTR	OUT	Rch, Common Pin of Analog Output Amp
12	NC	—	No Connection
13	$V_{OUT}R$	OUT	Rch, Analog Voltage Output of Audio Signal
14	AGND1	—	Analog Ground
15	$V_{CC}1$	—	Analog Power +5V
16	$V_{OUT}L$	OUT	Lch, Analog Voltage Output of Audio Signal
17	NC	—	No Connection
18	EXTL	OUT	Lch, Common Pin of Analog Output Amp
19	AGND2L	—	Analog Ground
20	$V_{CC}2L$	—	Analog Power +5V
21	ZERO	OUT	Zero Data Flag
22	$\overline{RST}$	IN	Reset. When this pin is low, the DF and modulators are held in reset.(2)
23	$\overline{CS}$/IWO	IN	Chip Select/Input Format Selection. When this pin is low, the Mode Control is effective.(3)
24	MODE	IN	Mode Control Select. (H: Software, L: Hardware)(2)
25	$\overline{MUTE}$	IN	Mute Control
26	MD/DM0	IN	Mode Control, DATA/De-emphasis Selection 1(2)
27	MC/DM1	IN	Mode Control, BCK/De-emphasis Selection 2(2)
28	ML/I²S	IN	Mode Control, WDCK/Input Format Selection(2)

NOTES: (1) Pins 1, 2, 3; Schmitt Trigger input. (2) Pins 22, 24, 25, 26, 27, 28; Schmitt Trigger input with pull-up resister. (3) Pin 23; Schmitt Trigger input with pull-down resister.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

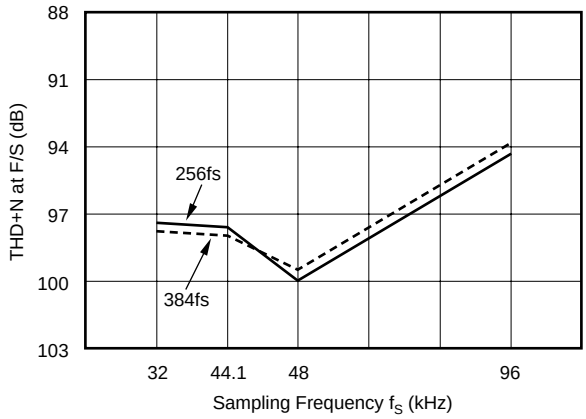
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

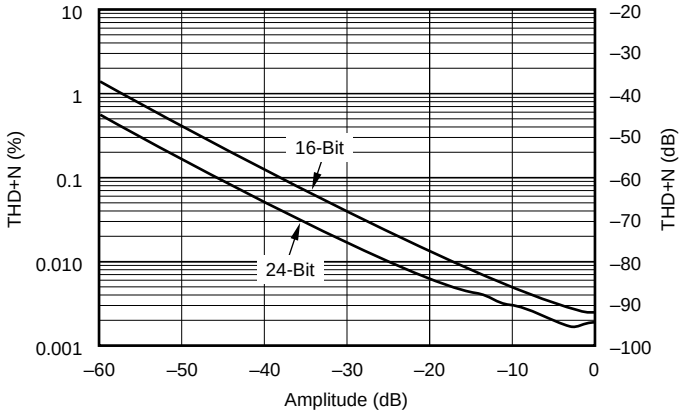
TYPICAL PERFORMANCE CURVES

All specifications at +25°C, $+V_{CC}$ = $+V_{DD}$ = +5V, f_S = 44.1kHz, and 24-bit input data, SYSCLK = 384f_S, unless otherwise noted.

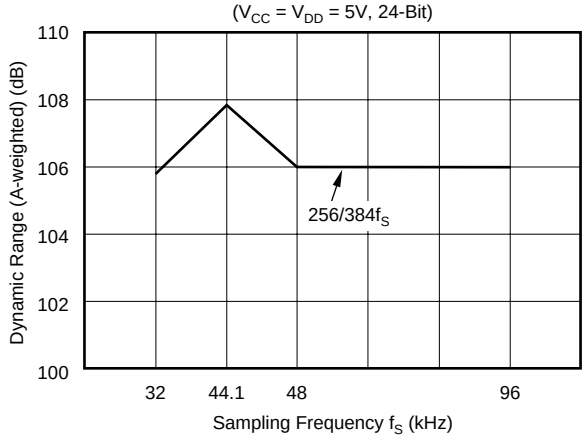
THD+N vs SAMPLING FREQUENCY
(V_{CC} = V_{DD} = 5V, 24-Bit)



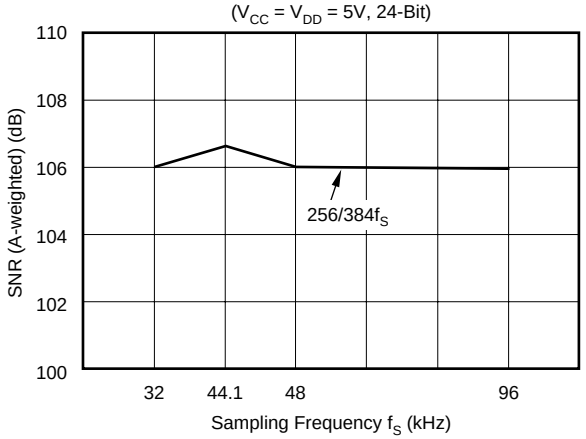
THD+N vs LEVEL
(f_S = 44.1kHz)



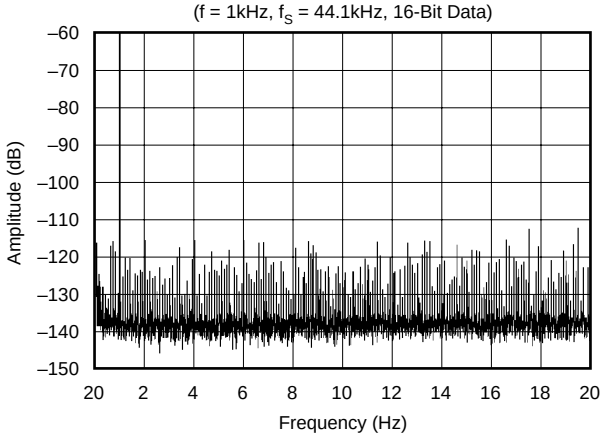
DYNAMIC RANGE vs SAMPLING FREQUENCY
(V_{CC} = V_{DD} = 5V, 24-Bit)



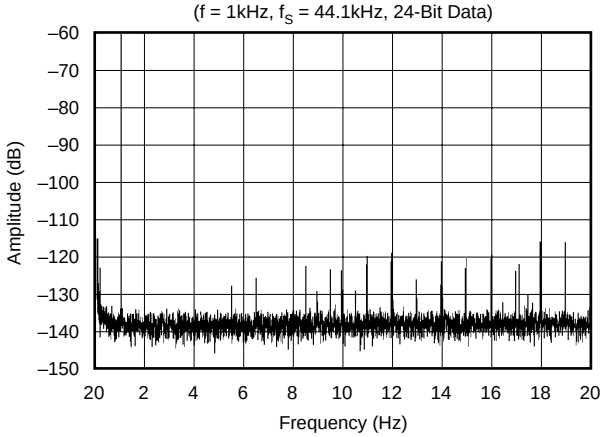
SNR vs SAMPLING FREQUENCY
(V_{CC} = V_{DD} = 5V, 24-Bit)



–60dB OUTPUT SPECTRUM
(f = 1kHz, f_S = 44.1kHz, 16-Bit Data)

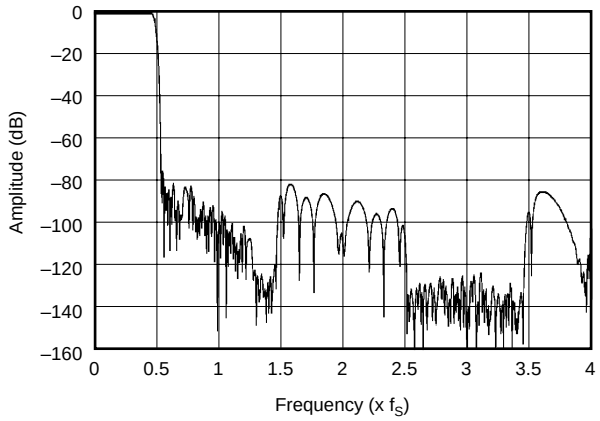


–60dB OUTPUT SPECTRUM
(f = 1kHz, f_S = 44.1kHz, 24-Bit Data)

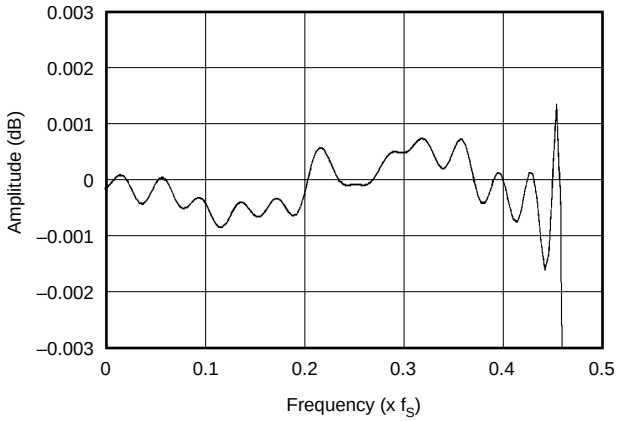


TYPICAL PERFORMANCE CURVES (CONT)

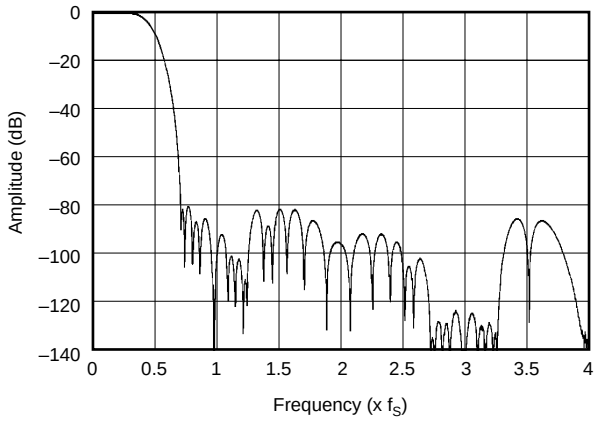
OVERALL FREQUENCY CHARACTERISTIC
(Sharp Roll-Off)



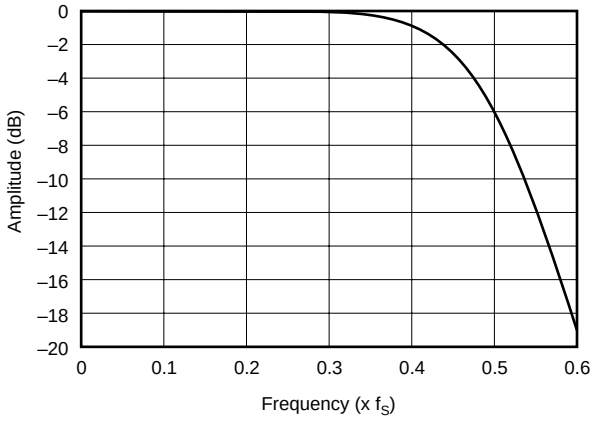
PASSBAND RIPPLE CHARACTERISTIC
(Sharp Roll-Off)



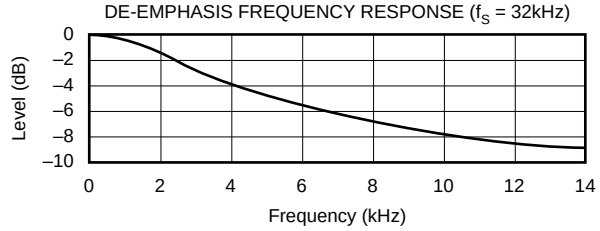
OVERALL FREQUENCY CHARACTERISTIC
(Slow Roll-Off)



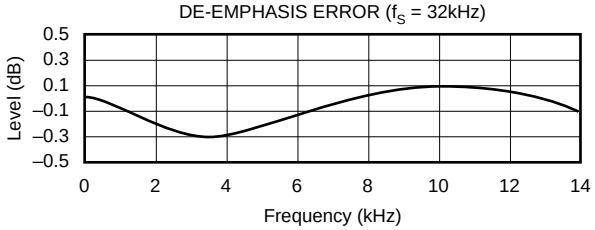
FREQUENCY CHARACTERISTIC
(Slow Roll-Off)



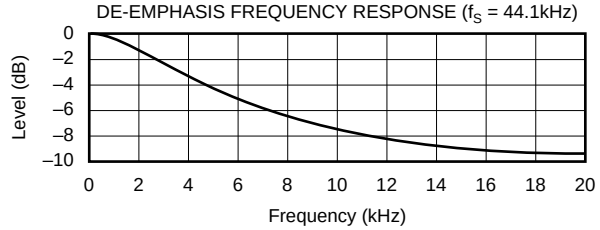
DE-EMPHASIS FREQUENCY RESPONSE (f_S = 32kHz)



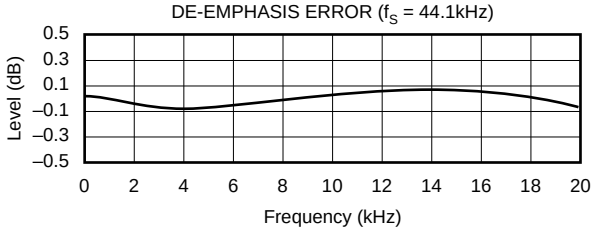
DE-EMPHASIS ERROR (f_S = 32kHz)



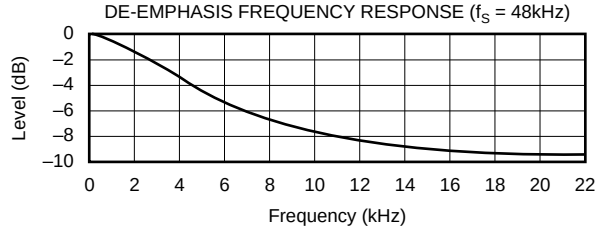
DE-EMPHASIS FREQUENCY RESPONSE (f_S = 44.1kHz)



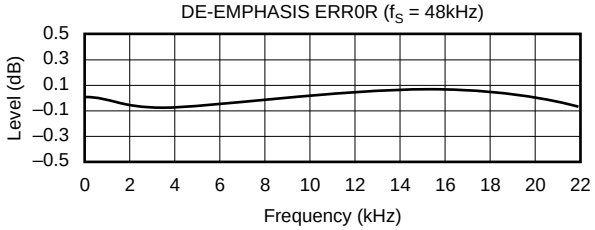
DE-EMPHASIS ERROR (f_S = 44.1kHz)



DE-EMPHASIS FREQUENCY RESPONSE (f_S = 48kHz)



DE-EMPHASIS ERR0R (f_S = 48kHz)



SYSTEM CLOCK

The system clock for PCM1716 must be either $256f_S$, $384f_S$, $512f_S$ or $768f_S$, where f_S is the audio sampling frequency (typically 32kHz, 44.1kHz, 48kHz, or 96kHz). But $768f_S$ at 96kHz is not accepted.

The system clock can be either a crystal oscillator placed between XTI (pin 5) and XTO (pin 6), or an external clock input to XTI. If an external system clock is used, XTO is open (floating). Figure 1 illustrates the typical system clock connections.

PCM1716 has a system clock detection circuit which automatically senses if the system clock is operating at $256f_S$ ~ $768f_S$. The system clock should be synchronized with LRCIN (pin 1) clock. LRCIN (left-right clock) operates at the sampling frequency f_S. In the event these clocks are not synchronized, PCM1716 can compensate for the phase difference internally. If the phase difference between left-right and system clocks is greater than 6-bit clocks (BCKIN), the synchronization is performed internally. While the synchronization is processing, the analog output is forced to a DC level at bipolar zero. The synchronization typically occurs in less than 1 cycle of LRCIN.

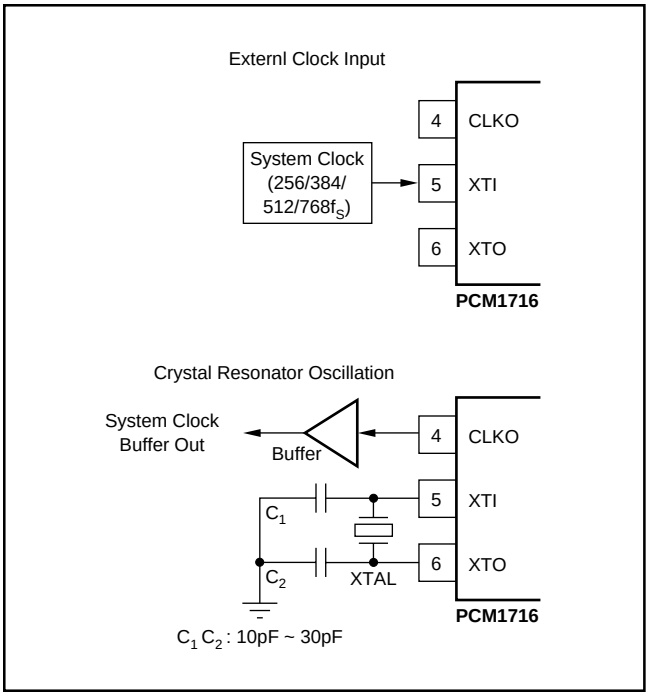


FIGURE 1. System Clock Connection.

Typical input system clock frequencies to the PCM1716 are shown in Table I, also, external input clock timing requirements are shown in Figure 2.

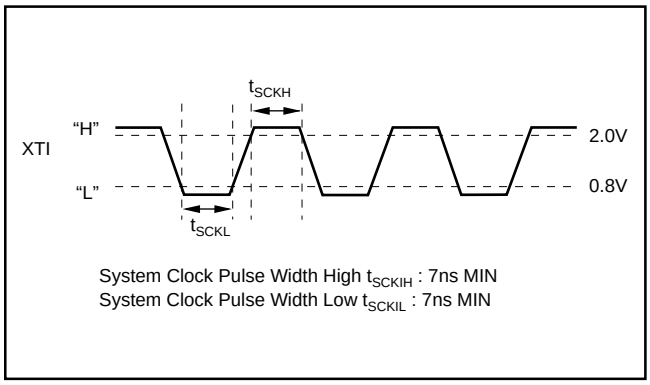


FIGURE 2. XTI Clock Timing.

DATA INTERFACE FORMATS

Digital audio data is interfaced to PCM1716 on pins 1, 2, and 3, LRCIN (left-right clock), DIN (data input) and BCKIN (bit clock). PCM1716 can accept both standard, I^2S, and left justified data formats.

Figure 3 illustrates acceptable input data formats. Figure 4 shows required timing specification for digital audio data.

Reset

PCM1716 has both internal power-on reset circuit and the $\overline{RST}$ pin (pin 22) which accepts an external forced reset by $\overline{RST}$ = LOW. For internal power on reset, initialize (reset) is done automatically at power on V_{DD} >2.2V (typ). During internal reset = LOW, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$. Figure 5 illustrates the timing of the internal power on reset.

PCM1716 accepts an external forced reset when $\overline{RST}$ = L. When $\overline{RST}$ = L, the output of the DAC is invalid and the analog outputs are forced to $V_{CC}/2$ after internal initialization (1024 system clocks count after $\overline{RST}$ = H.) Figure 6 illustrates the timing of the $\overline{RST}$ pin.

Zero Out (pin 21)

If the input data is continuously zero for 65536 cycles of BCK, an internal FET is switched to "ON". The drain of the internal FET is the zero-pin, it will enable "wired-or" with external circuit. This zero detect function is available in both software mode and hardware mode.

SAMPLING RATE FREQUENCY (f_S) - LRCIN	SYSTEM CLOCK FREQUENCY - MHz			
	$256f_S$	$384f_S$	$512f_S$	$768f_S$
32kHz	8.1920	12.2880	16.3840	24.5760
44.1kHz	11.2896	16.9340	22.5792	33.8688(1)
48kHz	12.2880	18.4320	24.5760	36.8640(1)
96kHz	24.5760	36.8640(1)	49.1520(1)	—

NOTE: (1) The Internal Crystal oscillator frequency cannot be larger than 24.576MHz.

TABLE I. Typical System Clock Frequency.

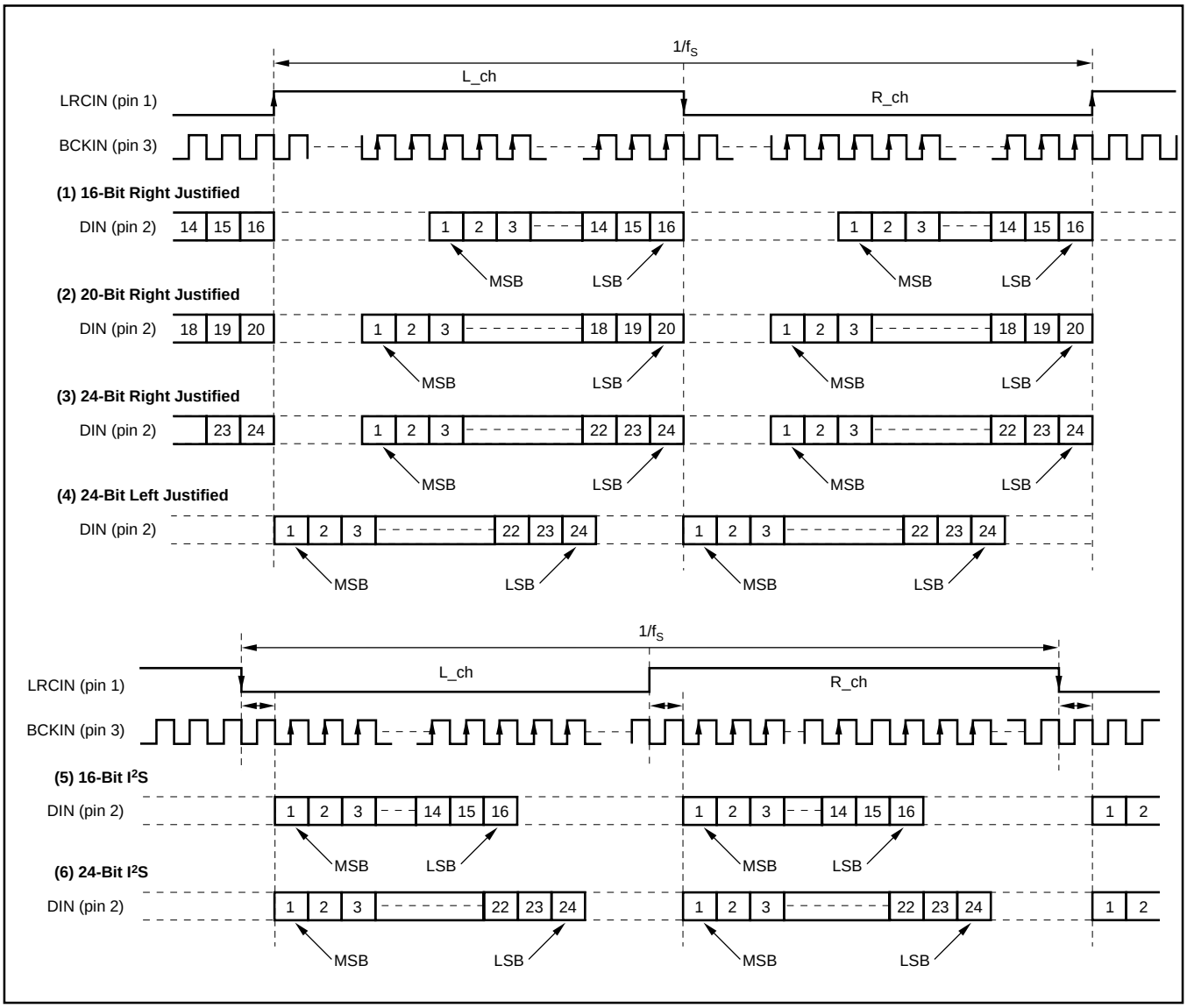
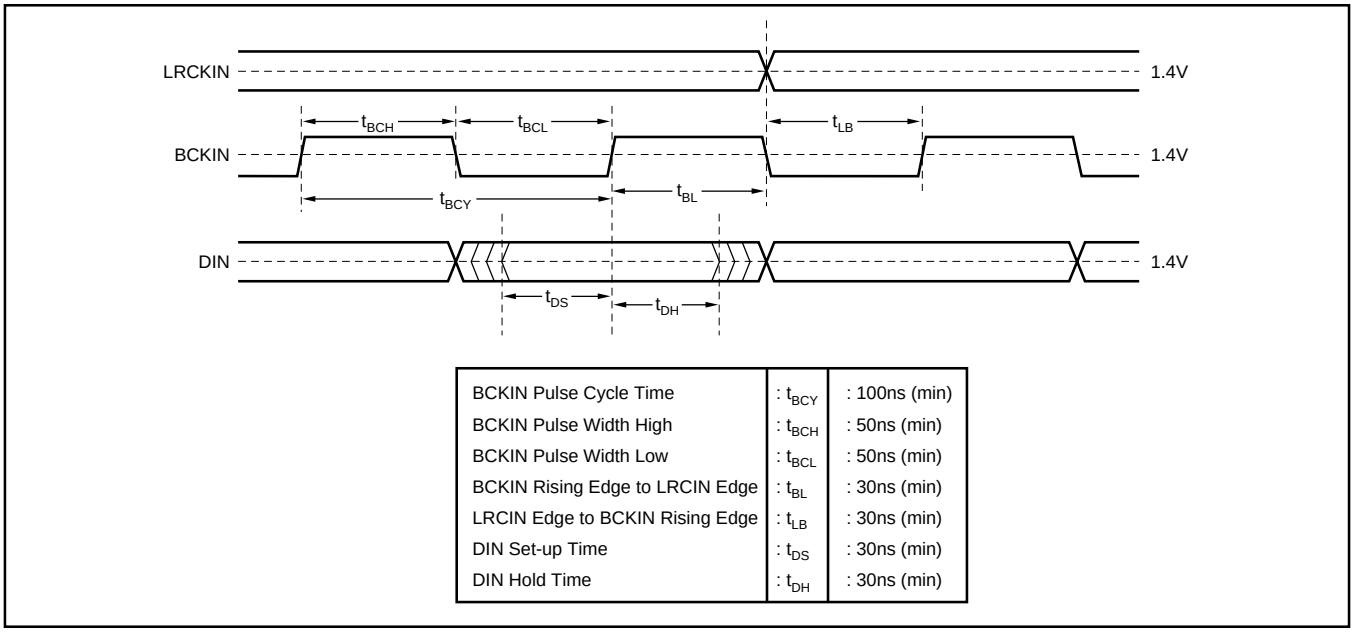


FIGURE 3. Audio Data Input Formats.



BCKIN Pulse Cycle Time	: t_{BCY}	: 100ns (min)
BCKIN Pulse Width High	: t_{BCH}	: 50ns (min)
BCKIN Pulse Width Low	: t_{BCL}	: 50ns (min)
BCKIN Rising Edge to LRCIN Edge	: t_{BL}	: 30ns (min)
LRCIN Edge to BCKIN Rising Edge	: t_{LB}	: 30ns (min)
DIN Set-up Time	: t_{DS}	: 30ns (min)
DIN Hold Time	: t_{DH}	: 30ns (min)

FIGURE 4. Audio Data Input Timing Specification.

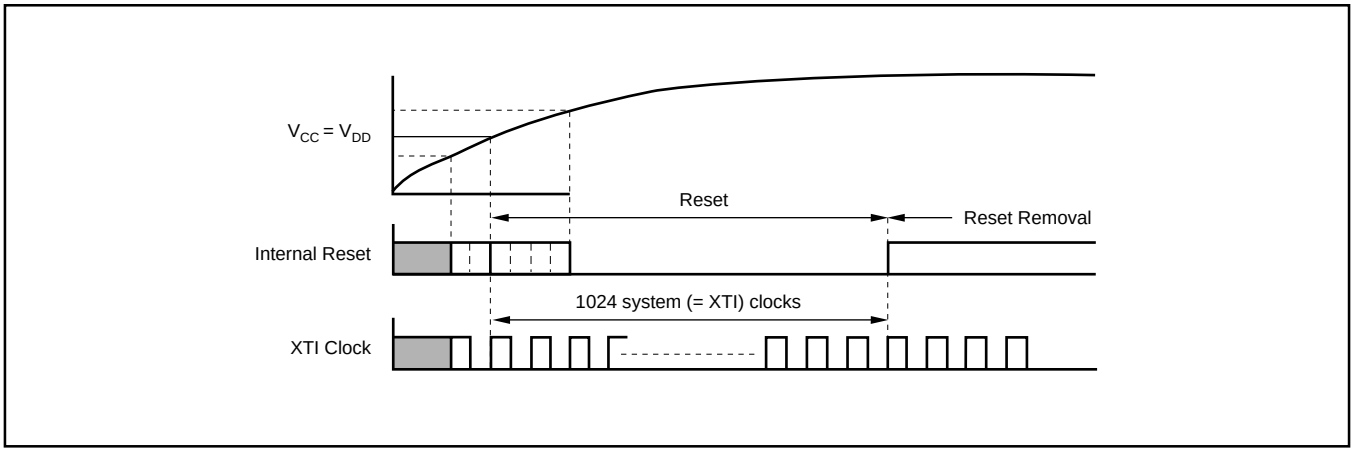


FIGURE 5. Internal Power-On Reset Timing.

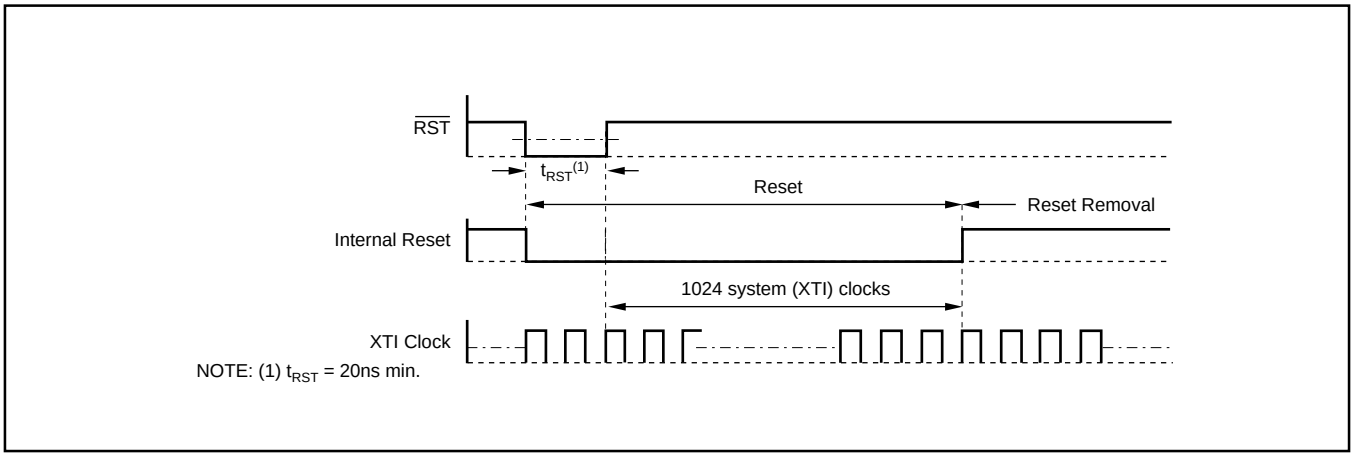


FIGURE 6. External Forced Reset Timing.

FUNCTIONAL DESCRIPTION

PCM1716 has several built-in functions including digital attenuation, digital de-emphasis, input data format selection, and others. These functions are software controlled. PCM1716 can be operated in two different modes, software mode or hardware mode. Software mode is a three-wire interface using pin 28 (ML), 27 (MC), and 26 (MD).

PCM1716 can also be operated in hardware mode, where static control signals are used on pin 28 (115, pin 27 (DM1), pin 26 (DM0) and pin 23 (IWO).

This basic operation mode as software or hardware can be selected by pin 24 (MODE) as shown in Table II.

MODE (pin 24) = H	Software Mode
MODE (pin 24) = L	Hardware Mode

TABLE II. Mode Control.

Table III indicates which functions are selectable within the users chosen mode. All of the functions shown are selectable within the software mode, but only de-emphasis control, soft mute and input data format may be selected when using PCM1716 in the hardware mode.

FUNCTION	SOFTWARE (Mode = H)	HARDWARE (Mode = L)
Input Data Format Selection	O	O
Input Data Bit Selection	O	O
Input LRCIN Polarity Selection	O	X
De-emphasis Control	O	O
Mute	O	O
Attenuation	O	X
Infinity Zero Mute Control	O	X
DAC Operation Control	O	X
Slow Roll-Off Selection	O	X
Output Phase Selection	O	X
CLKO Output Selection	O	X

NOTE: O = Selectable, X: Not Selectable.

TABLE III. Mode Control, Selectable Functions.

HARDWARE MODE (MODE = L)

In hardware mode, the following function can be selected.

De-emphasis control

De-emphasis control can be selected by DM1 (pin 27) and DM0 (pin 26)

DM1 (Pin 27)	DM0 (Pin 26)	DE-EMPHASIS
L	L	OFF
L	H	48kHz
H	L	44.1kHz
H	H	32kHz

TABLE IV. De-emphasis Control.

Input Audio Data Format

Input data format can be selected by I^2S (pin 28) and IWO (pin 23)

I²S (Pin 28)	IWO (Pin 23)	DATA FORMAT
L	L	16-Bit Data Word, Normal, Right Justified
L	H	20-Bit Data Word, Normal, Right Justified
H	L	16-Bit Data Word, I²S Format
H	H	24-Bit Data Word, I²S Format

TABLE V. Data Format Control.

SOFT MUTE

Soft Mute function can be controlled by $\overline{\text{MUTE}}$ (pin 25)

$\overline{\text{MUTE}}$ (Pin 25)	SOFT MUTE
L	Mute ON
H	Mute OFF (Normal Operation)

SOFTWARE MODE (MODE = H)

PCM1716's special functions at software mode is shown in Table VI. These functions are controlled using a ML, MC, MD serial control signal.

FUNCTION	DEFAULT MODE
Input Audio Data Format Selection Standard Format Left Justified I²S Format	Standard Format
Input Audio Data Bit Selection 16-Bit 20-Bit 24-Bit	16-Bit
Input LRCIN Polarity Selection Lch/Rch = High/Low Lch/Rch = Low/High	Lch/Rch = High/Low
De-emphasis Control	OFF
Soft Mute Control	OFF
Attenuation Control Lch, Rch Individually Lch, Rch Common	0dB, Individual
Infinite Zero Mute Control	Not Operated
DAC Operation Control	Operated
Sampling Rate Selection for De-emphasis Standard Frequency 44.1kHz 48kHz 32kHz	44.1kHz
Slow Roll-Off Selection	Not Selected (Sharp Roll-Off)
Output Phase Selection	Not Inverted
CLK0 Output Selection	Input Frequency

TABLE VI. Selectable Functions and Default.

PROGRAM REGISTER BIT MAPPING

PCM1716's special functions are controlled using four program registers which are 16 bits long. These registers are all loaded using MD. After the 16 data bits are clocked in, ML is used to latch in the data to the appropriate register. Table VII shows the complete mapping of the four registers and Figure 7 illustrates the serial interface timing.

MAPPING OF PROGRAM REGISTERS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
MODE0	res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
MODE1	res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
MODE2	res	res	res	res	res	A1	A0	res	res	res	res	IW1	IW0	OPE	DEM	MUT
MODE3	res	res	res	res	res	A1	A0	IZD	SF1	SF0	CK0	REV	SR0	ATC	LRP	I²S

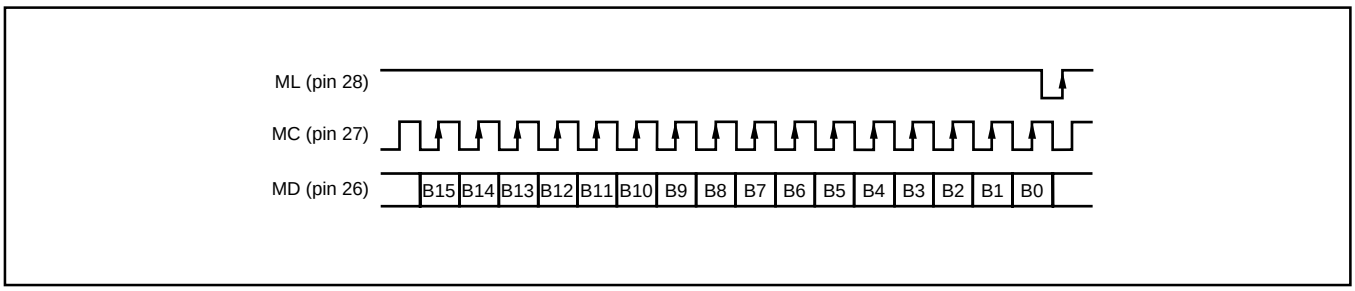


FIGURE 7. Three-Wire Serial Interface.

REGISTER NAME	BIT NAME	DESCRIPTION
Register 0	AL (7:0) LDL A (1:0) res	DAC Attenuation Data for Lch Attenuation Data Load Control for Lch Register Address Reserved, should be “L”
Register 1	AR (7:0) LDR A (1:0) res	DAC Attenuation Data for Rch Attenuation Data Load Control for Rch Register Address Reserved, should be “L”
Register 2	MUT DEM OPE IW (1:0) res A (1:0) res	Left and Right DACs Soft Mute Control De-emphasis Control Left and Right DACs Operation Control Input Audio Data Bit and Format Select Reserved Register Address Reserved, should be “L”
Register 3	I^2S LRP ATC SRO REV CKO SF (1:0) IZD A (1:0) res	Audio Data Format Select Polarity of LRCIN Select Attenuator Control Slow Roll-Off Select Output Phase Select CLKO Output Select Sampling Rate Select Internal Zero Detection Circuit Control Register Address Reserved, should be “L”

TABLE VII. Register Functions

REGISTER 0 (A1 = 0, A0 = 0)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0

Register 0 is used to control left channel attenuation. Bits 0 - 7 (AL0 - AL7) are used to determine the attenuation level. The level of attenuation is given by:

ATT = 0.5 x (data-255) (dB)
FFh = –0dB
FEh = –0.5dB
:
:
01h = –127.5dB
00h = – ∞ (= Mute)

ATTENUATION DATA LOAD CONTROL

Bit 8 (LDL) is used to control the loading of attenuation data in B0:B7. When LDL is set to 0, attenuation data will be loaded into AL0:AL7, but it will not affect the attenuation level until LDL is set to 1. LDR in Register 1 has the same function for right channel attenuation.

REGISTER 1 (A1 = 0, A0 = 1)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0

Register 1 is used to control right channel attenuation. As in Register 1, bits 0 - 7 (AR0 - AR7) control the level of attenuation.

REGISTER 2 (A1 = 1, A0 = 0)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	res	res	res	res	IW1	IWO	OPE	DEM	MUTE

Register 2 is used to control soft mute, de-emphasis, operation enable, input resolution, and input audio data bit and format.

MUT (B0)	
MUT = L	Soft Mute OFF
MUT = H	Soft Mute ON

DEM (B1)	
DEM = L	De-emphasis OFF
DEM = H	De-emphasis ON

OPE (B2)	
OPE = L	Normal Operation
OPE = H	DAC Operation OFF

when OPE (B2) is “HIGH”, the output of the DAC will be forced to bipolar zero, irrespective of any input data.

IWO (B3), IW1 (B4) and I^2S (B0) of Register 3

These resisters, IWO, IW1, I^2S determine the input data word and input data format as shown below.

IW1	IW0	I^2S	Audio Interface
0	0	0	16-Bit Standard (Right-Justified)
0	1	0	20-Bit Standard (Right-Justified)
1	0	0	24-Bit Standard (Right-Justified)
1	1	0	24-Bit Left-Justified (MSB First)
0	0	1	16-Bit I^2S
0	1	1	24-Bit I^2S
1	0	1	Reserved
1	1	1	Reserved

REGISTER 3 (A1 = 1, A0 = 1)

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
res	res	res	res	res	A1	A0	IZD	SF1	SF0	CKO	REV	SRO	ATC	LRP	I^2S

REGISTER 3 (A1 = 1, A0 = 1)

Register 3 is used to control input data format and polarity, attenuation channel control, system clock frequency, sampling frequency, infinite zero detection, output phase, CLKO output, and slow roll-off.

Bit 8 is used to control the infinite zero detection function (IZD).

When IZD is “LOW”, the zero detect circuit is off. Under this condition, no automatic muting will occur if the input is continuously zero. When IZD is “HIGH”, the zero detect feature is enabled. If the input data is continuously zero for 65, 536 cycles of BCKIN, the output will be immediately

forced to a bipolar zero state ($V_{CC}/2$). The zero detection feature is used to avoid noise which may occur when the input is DC. When the output is forced to bipolar zero, there may be an audible click. PCM1716 allows the zero detect feature to be disabled so the user can implement an external muting circuit.

IZD (B8)	
B8 = L	Zero Detect Mute OFF
B8 = H	Zero Detect Mute ON

Bits 6 (SF0) and 7 (SF1) are used to select the sampling frequency for De-emphasis.

SF1	SF0	Sampling Rate
0	0	Reserved
0	1	48kHz
1	0	44.1kHz
1	1	32kHz

CKO (B5) is output frequency control at CLKO pin, can be selected as Buffer (1/1) or half rate of input frequency (1/2).

CKO = L	Buffer Out of XTi Clock
CKO = H	Half (1/2) Frequency Out of XTi Clock

REF (B4) is output analog signal phase control.

REV = L	Normal Output
REV = H	Inverted Output

SRO (B3) is roll-off performance of digital filter selection.

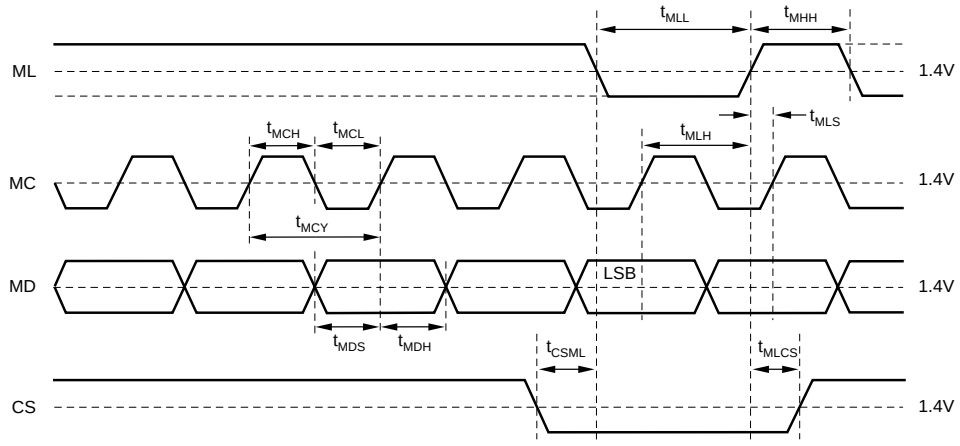
SRO = L	Sharp Roll-Off
SRO = H	Slow Roll-Off

ATC (B2) is used as an attenuation control. When bit 3 is set HIGH, the attenuation data on Register 0 is used for both channels, and the data in Register 1 is ignored. When bit 3 is LOW, each channel has separate attenuation data.

ATC = L	Ch Individual ATT Control
ATC = H	Common ATT Control

Bits 0 (I^2S) and 1 (LRP) are used to control the input data format. A “LOW” on bit 0 sets the format to (MSB-first, right-justified Japanese format) and a “HIGH” sets the format to I^2S (Philips serial data protocol). Bit 1 (LRP) is used to select the polarity of LRCIN (sample rate clock). When bit 1 is “LOW”, left channel data is assumed when LRCIN is in a “HIGH” phase and right channel data is assumed when LRCIN is in a “LOW” phase. When bit 1 is “HIGH”, the polarity assumption is reversed.

LRP = L	L R	H/Lch
LRP = H	L R	L/Lch



MC Pulse Cycle Time	: t_{MCY}	: 100ns (min)
MC Pulse Width LOW	: t_{MCL}	: 40ns (min)
MC Pulse Width HIGH	: t_{MCH}	: 40ns (min)
MD Hold Time	: t_{MDH}	: 40ns (min)
MD Set-up Time	: t_{MDS}	: 40ns (min)
ML Low Level Time	: t_{MLL}	: 40ns (min) + 1SYSCLK(1) (min)
ML High Level Time	: t_{MHH}	: 40ns (min) + 1SYSCLK(1) (min)
ML Hold Time	: t_{MLH}	: 40ns (min)
ML Set-up Time	: t_{MLS}	: 40ns (min)
$\overline{CS}$ Low to ML Low Time(2)	: t_{CSML}	: 10ns (min)
ML High to $\overline{CS}$ High Time(2)	: t_{MLCS}	: 10ns (min)

NOTE: (1) System Clock Cycle. (2) $\overline{CS}$ Should be changed during ML = H.

FIGURE 8. Program Register Input Timing.

THEORY OF OPERATION

The delta-sigma section of PCM1716 is based on a 8-level amplitude quantizer and a 4th-order noise shaper. This section converts the oversampled input data to 8-level delta-sigma format.

This newly developed, "Enhanced Multi-level Delta-Sigma" architecture achieves high-grade audio dynamic performance and sound quality.

A block diagram of the 8-level delta-sigma modulator is shown in Figure 9. This 8-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8-times interpolation filter is $64f_S$ for all system clock ratios ($256/384/512/768f_S$).

The theoretical quantization noise performance of the 8-level delta-sigma modulator is shown in Figure 10. This enhanced multi-level delta-sigma architecture also has advantages for input clock jitter sensitivity due to the multi-level quantizer, simulated jitter sensitivity is shown in Figure 11.

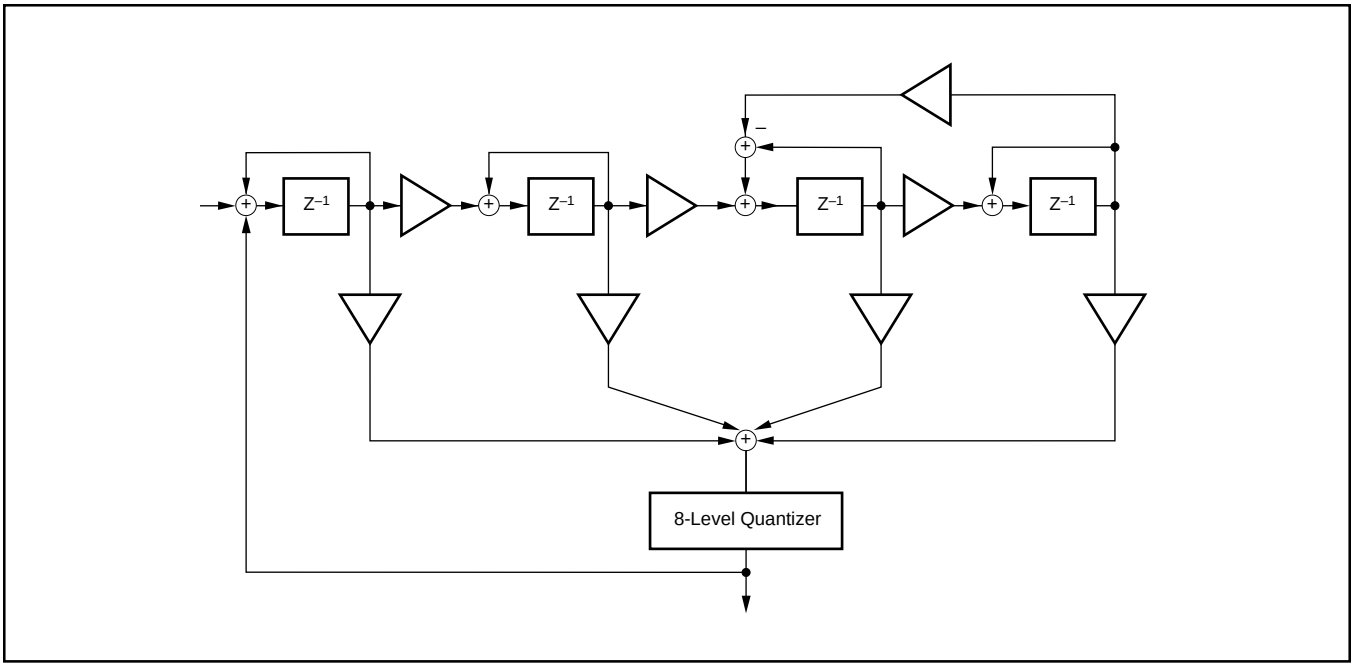


FIGURE 9. 8-Level Delta-Sigma Modulator.

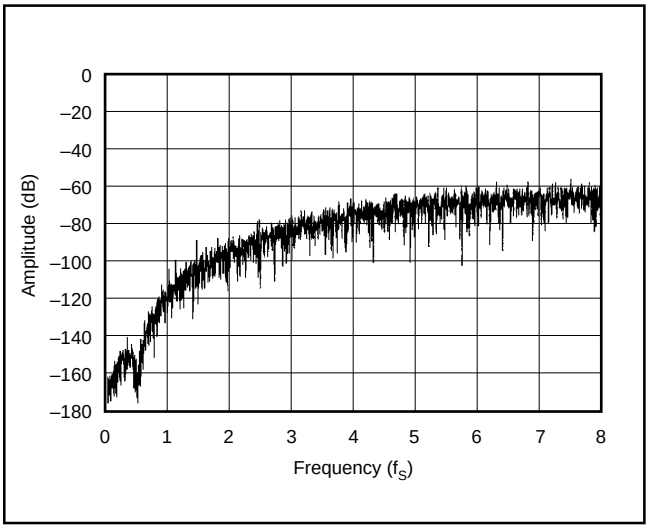


FIGURE 10. Quantization Noise Spectrum.

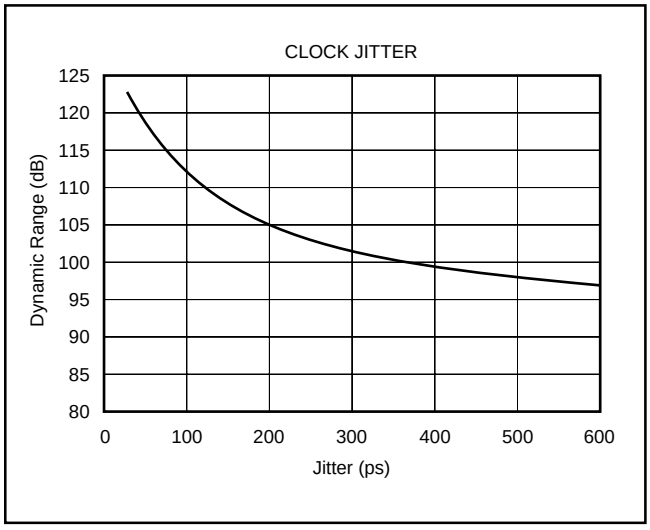


FIGURE 11. Jitter Sensitivity.

APPLICATION CONSIDERATIONS

DELAY TIME

There is a finite delay time in delta-sigma converters. In A/D converters, this is commonly referred to as latency. For a delta-sigma D/A converter, delay time is determined by the order number of the FIR filter stage, and the chosen sampling rate. The following equation expresses the delay time of PCM1716:

$$T_D = 30 \times 1/f_S$$

For f_S = 44.1kHz, T_D = 30/44.1kHz = 680µs

Applications using data from a disc or tape source, such as CD audio, DVD audio, Video CD, DAT, Minidisc, etc., generally are not affected by delay time. For some professional applications such as broadcast audio for studios, it is important for total delay time to be less than 2ms.

OUTPUT FILTERING

For testing purposes all dynamic tests are done on the PCM1716 using a 20kHz low pass filter. This filter limits the measured bandwidth for THD+N, etc. to 20kHz. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the specifications. The low pass filter removes out of band noise. Although it is not audible, it may affect dynamic specification numbers.

The performance of the internal low pass filter from DC to 40kHz is shown in Figure 12. The higher frequency roll-off of the filter is shown in Figure 13. If the user's application has the PCM1716 driving a wideband amplifier, it is recommended to use an external low pass filter.

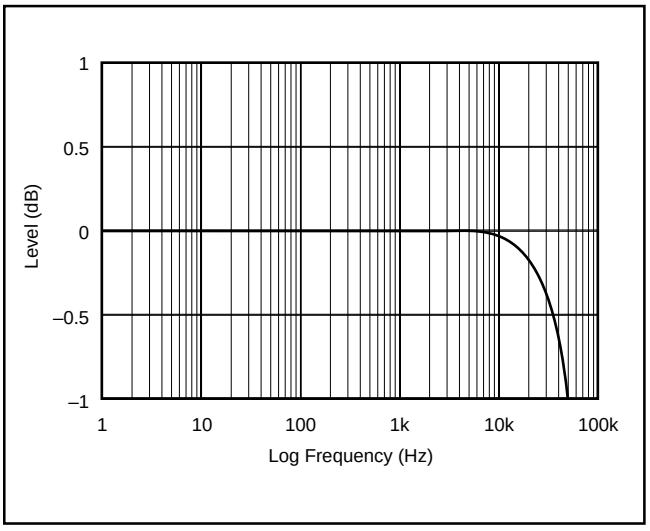


FIGURE 12. Low Pass Filter Response.

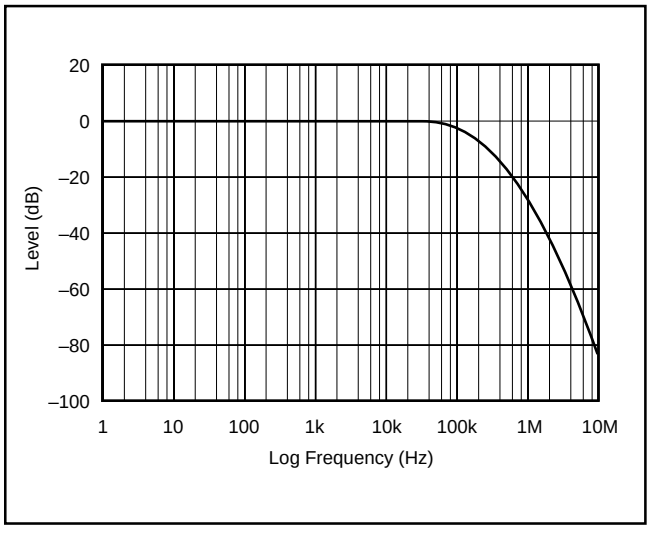


FIGURE 13. Low Pass Filter Response.

BYPASSING POWER SUPPLIES

The power supplies should be bypassed as close as possible to the unit. Refer to Figure 15 for optimal values of bypass capacitors.

POWER SUPPLY CONNECTIONS

PCM1716 has three power supply connections: digital (V_{DD}), and analog (V_{CC}). Each connection also has a separate ground. If the power supplies turn on at different times, there is a possibility of a latch-up condition. To avoid this condition, it is recommended to have a common connection between the digital and analog power supplies. If separate supplies are used without a common connection, the delta between the two supplies during ramp-up time must be less than 0.1V.

An application circuit to avoid a latch-up condition is shown in Figure 14.

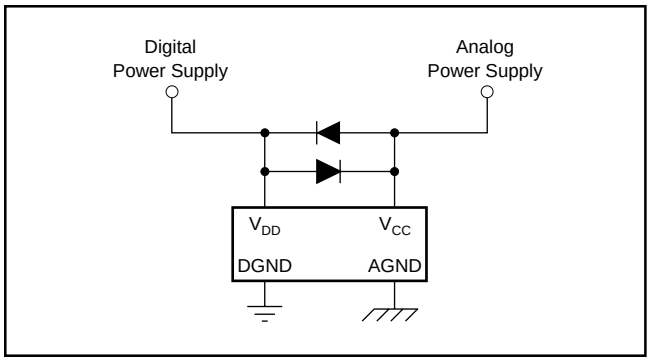


FIGURE 14. Latch-Up Prevention Circuit.

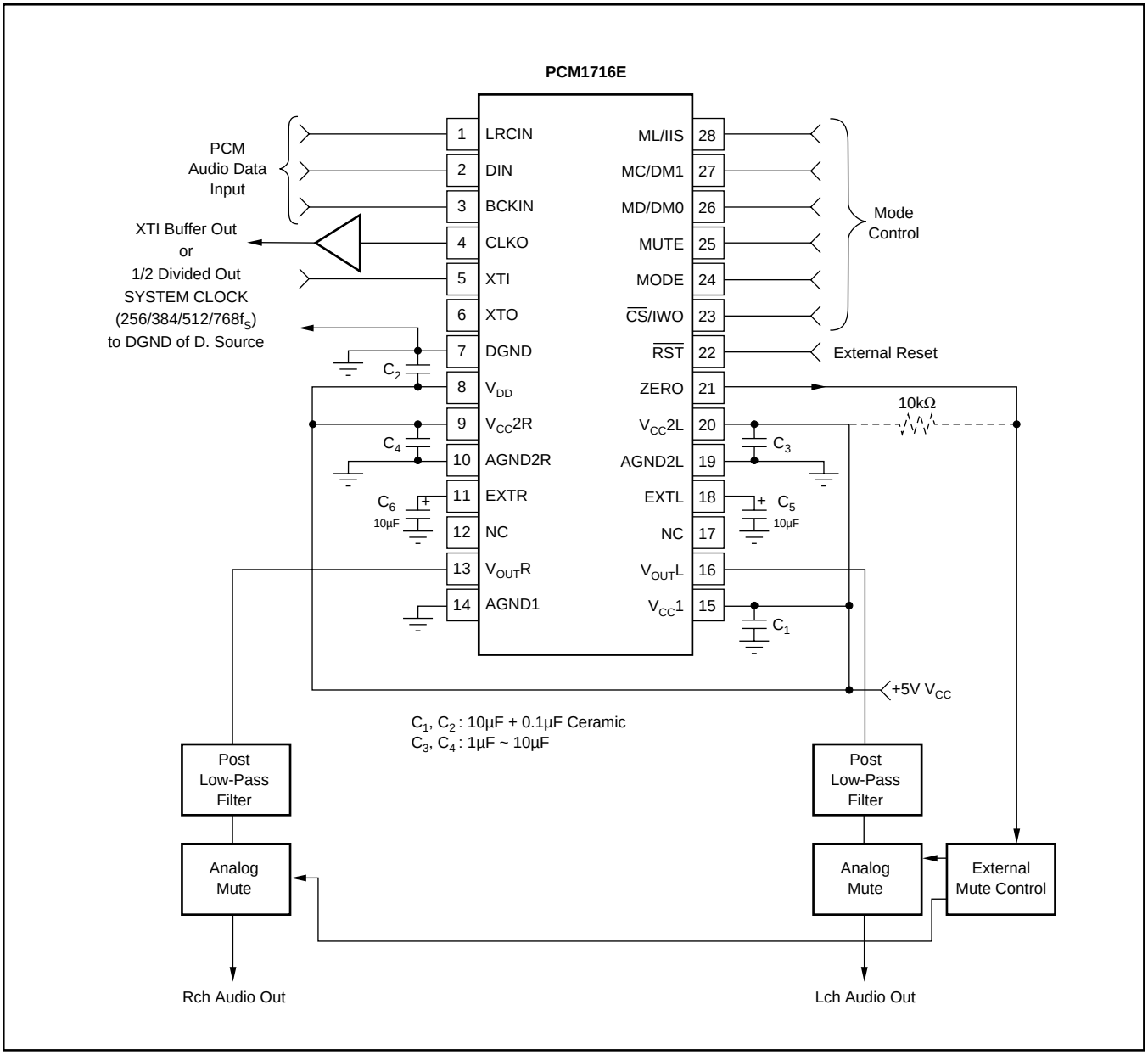


FIGURE 15. Typical Circuit Connection Diagram.

www.ti.com

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
PCM1716E	NRND	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
PCM1716E/2K	NRND	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
PCM1716E/2KG4	NRND	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260
PCM1716EG4	NRND	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

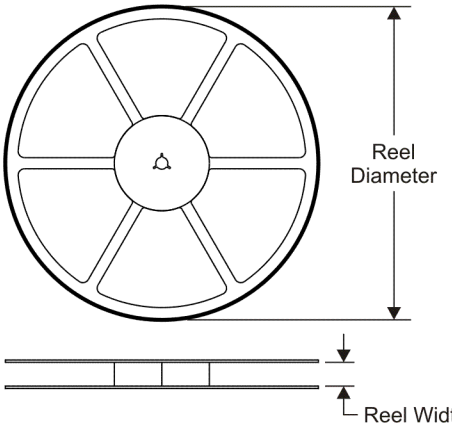
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI
provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate inf
continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical an
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for releas

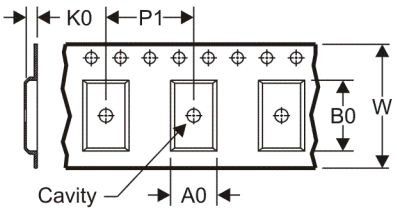
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Cu

TAPE AND REEL INFORMATION

REEL DIMENSIONS

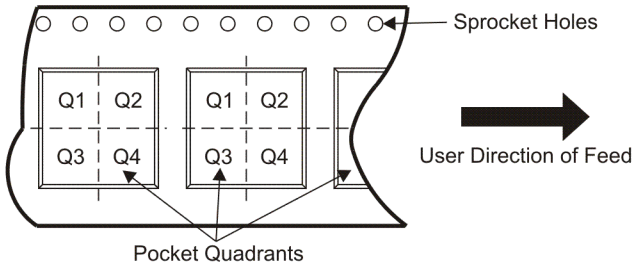


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

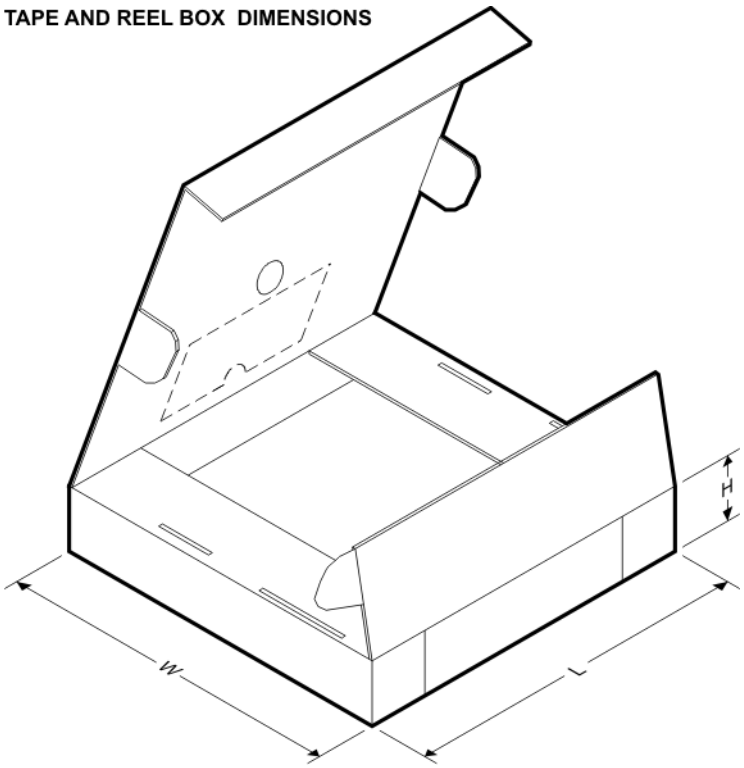
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1716E/2K	SSOP	DB	28	2000	330.0	17.4	8.5	10.8	2.4	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1716E/2K	SSOP	DB	28	2000	336.6	336.6	28.6

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connctivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated