DATA SHEET

AR1019 Single Chip FM Radio

Single Chip FM Radio

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Airoha Technology Corp.

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Revision History

Version	Change Summary	Date	Author
0.10	Created	27-Aug-2010	Adrian. Wu

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1 Features

- Worldwide FM band support: 64MHz~108MHz
- Highest integration level with minimized external BOM cost
- Frequency synthesizer with integrated VCO and Automatic Frequency Control (AFC)
- Integrated XO with external reference clock input (32.768KHz, 32KHz, 4.5MHz, 12MHz, 13MHz, 19.2MHz, 24MHz, 26Mhz, 27MHz, 38.4MHz) or external 32.768KHz crystal
- Automatic Gain Control (AGC) on LNA/VGA amplifiers
- Signal strength measurement
- Programmable de-emphasis time constant (50/75us)
- Adaptive noise suppression
- Analog output with volume control and Line-level outputs
- Serial control interface for 2-wire mode
- Embedded Seek tuning function
- Integrated LDO regulators support 2.2V to 3.6 V supply voltage
- Support 32Ω output load resistance
- MSOP 3x4.9x1mm 10-pin package

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2 Description

AR1019 is a highly integrated single chip stereo FM radio receiver for all kinds of applications. AR1019 supports worldwide FM bands from 64MHz to 108MHz. It integrates LNA, Mixer, Oscillator and LDO regulator to minimize the external BOM cost. The built-in FM signal processing unit with noise reduction mechanism provides optimum sound quality. A simple 2-wire interface allows easy control from the host.

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3 Pin Assignment

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1.1 Pin Name Description

PIN	SIGANL	TYPE	DESCRIPTION
1	DATAIO	Input/Output, Digital	Serial Interface
2	VCC	VCC Supply	Supply Voltage
3	LOUT	Output, Analog	Left Audio Output
4	ROUT	Output, Analog	Right Audio Output
5	GNDA	GND	Analog Ground
6	NC	NC	Not Connected/The pin must be floating
7	GNDRF	GND	RF Ground
8	RFIN	Input, Analog	RF Input
9	CLOCK	Input, Digital Control	Serial Interface
10	XTAL	Analog	XTAL Input/External REFCLK input

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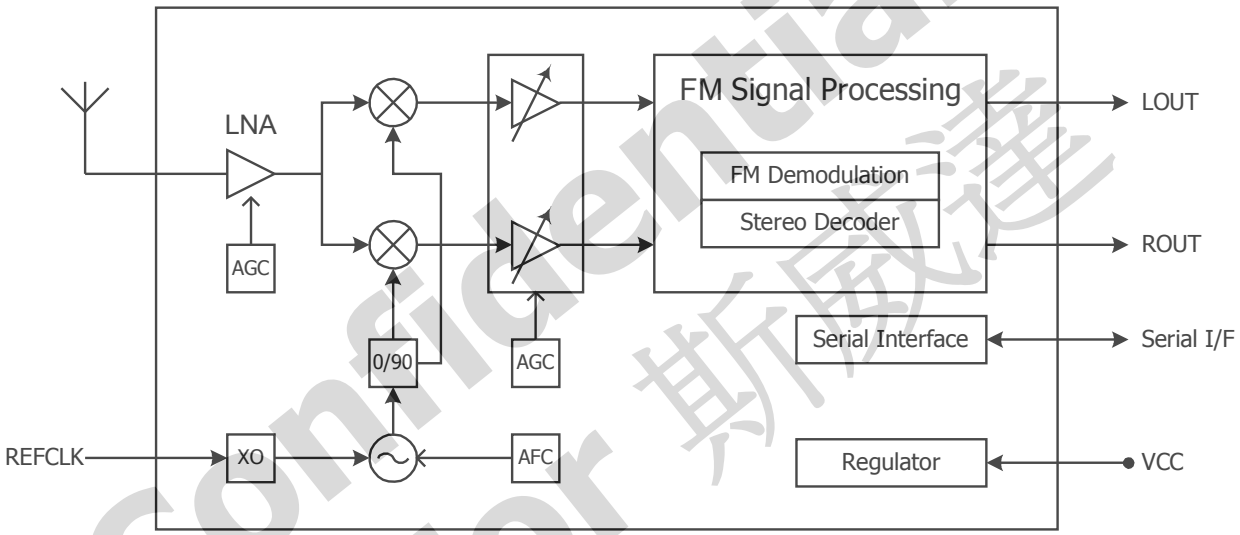
4 Block Diagram and Description

1.2 General Description



AR1019 is a single chip FM radio receiver IC, which supports full 64MHz to 108MHz band. AR1019 integrates on-chip LNA, Mixer, VGA, XO, FM signal processing unit, serial digital I/O interfaces and regulator. The highest integration level minimizes external BOM cost and provides optimum sound quality.

1.3 Radio Receiver

The Radio Receiver part comprises a LNA, a Low-IF mixer and a VGA. The front-end gain of the LNA could be adjusted automatically and thus optimize the received signal-to-noise ratio. The RF signal is then converted to Low-IF band and amplified by the VGA, which is also automatically adjusted. After then the received signal is fed into the FM signal processing unit.

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An internal reference oscillator is integrated, so only an external 32.768KHz crystal or a REFCLK signal is required. (32.768KHz, 32KHz, 4.5MHz, 12MHz, 13MHz, 19.2MHz, 24MHz, 26Mhz, 27MHz, 38.4MHz)

1.4 FM signal processing Unit

The main function of the FM signal processing unit includes FM Demodulation and Stereo Decoding . The received FM signal at VGA output is first demodulated into stereo multiplexed signals (Left+Right and Left–Right) and then decoded into Left and Right signals individually by the stereo decoder. Two time constants (50μs or 75μs) of de-emphasis are provided and programmable through the serial interface.

The decoded stereo signals are output to the LOUT and ROUT pins. The output volume could be adjusted or mute through the serial interface. The stereo output could be blocked and only mono signal is output under weak signals.

1.5 Serial 2-Wire Interface

Serial 2-wire interfaces are provided to read and write the control registers.

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SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
	CLOCK Frequency	0		400	KHz
T_{S1}	CLOCK Input to DATA N-edge Setup time (START)	600			ns
T_{H1}	CLOCK Input to DATA N-edge Hold time (START)	600			ns
T_{S2}	DATA Input to CLOCK P-edge Setup time	100			ns
T_{H2}	DATA Input to CLOCK N-edge Hold time	0		900	ns
T_{S3}	CLOCK Input to DATA P-edge Setup time (STOP)	600			ns
T_{BUF}	STOP to START time	1300			ns
T_{OF}	DATA Output Fall time	20		250	ns
T_{IR}	DATA Input & CLOCK Rise time	20		300	ns
T_{IF}	DATA Input & CLOCK Fall time	20		300	ns
T_{HIGH}	CLOCK HIGH duration	600			ns
T_{LOW}	CLOCK LOW duration	1300			ns
T_{PS}	Input Filter Pulse Suppression			50	ns

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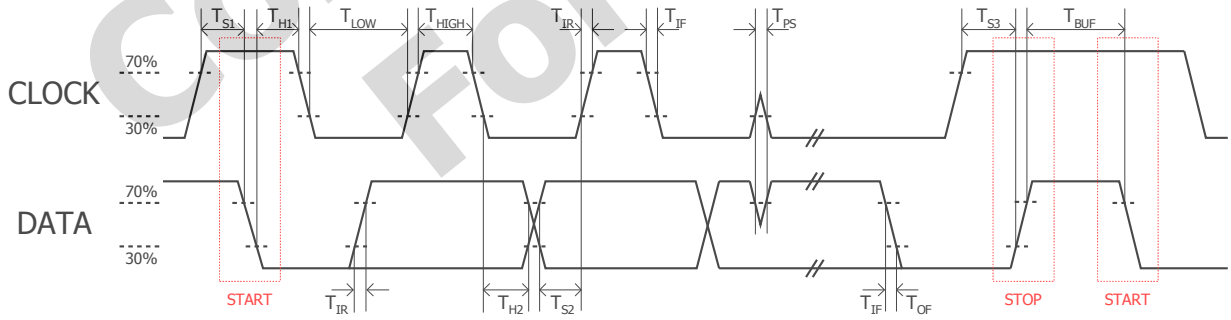
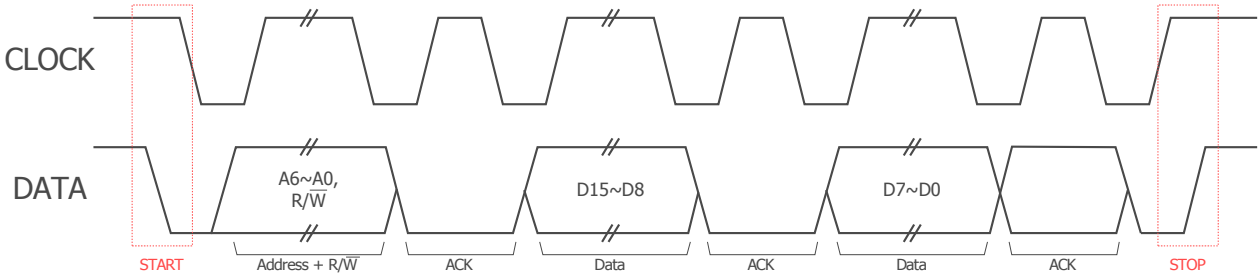
2-Wire Interface Read and Write Timing Parameters



2-Wire Interface Read and Write Procedure



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5 Electrical Characteristics

1.6 Absolute Maximum Ratings

AR1019 could be damaged by any stress in excess of the absolute maximum ratings listed below.

ITEM	MIN.	MAX.
Power supply voltage (VCC)	- 0.3V	3.6V
Pin voltage	- 0.3V	HOST_IO_VCC + 0.3V
Maximum power dissipation	-	1W
Operating temperature	- 40°C	+85°C
Storage temperature	- 65°C	+150°C
LNA input level	-	+10 dBm

1.7 DC Electrical Specifications

Recommended operating ambient temperature range T_A = -20 to 85°C

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
VCC Supply Voltage	VCC		2.2		3.6	V
VCC Supply Current	I_{VCC}	ENABLE=1		15.5		mA
Power Down Current	I_{VCC}	ENABLE=0		7	20	μA
Digital Input Voltage – High Level	V_{IH}		0.7*VCC		VCC+0.3	V
Digital Input Voltage – Low Level	V_{IL}		- 0.3		0.3*VCC	V
Digital Input Current – High Level	I_{IH}	V_{IN}=VCC=3.6V	-10		10	μA
Digital Input Current – Low Level	I_{IL}	V_{IN}=0V, VCC=3.6V	-10		10	μA
Interface Output Voltage – High Level	V_{OH}	I_{OUT} = 500μA	0.8*VCC			V
Interface Output Voltage – Low Level	V_{OL}	I_{OUT} = - 500μA			0.2*VCC	V

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1.8 AC Electrical Specification

Typical values are tested under VCC=3.3V, Ta=25°C unless otherwise specified

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input Frequency		64		108	MHz
Sensitivity	(S+N)/N=26dB, FD=22.5KHz		1.8	3.5	μVemf
LNA Input Resistance			126		Ω
LNA Input Capacitance			3.6		pF
IIP3			86		dBμV
AM Suppression	m=0.3		70		dB
Adjacent Channel Selectivity	Low-side, -200KHz		38		dB
	Low-side, +200KHz		55		dB
	Low-side, -400KHz		>60		dB
	Low-side, +400KHz		>60		dB
Spurious Response Rejection	In-band		38		dB
Crystal REFCLK Frequency			32.768		KHz
External REFCLK Frequency		32K		38.4M	Hz
REFCLK Frequency Tolerance	25°C	-20		+20	ppm
	-20°C ~ +85°C	-150		+150	ppm
Audio Output Voltage *1,	FD=22.5KHz, at max. vol.	90	95	110	mV_{RMS}
Audio Output L/R Imbalance *1	FD=75KHz	-0.5		0.5	dB
Audio Stereo Separation *1	FD=75KHz including 9% pilot		40		dB
Audio S/N *1	FD=22.5KHz		56		dB
Audio THD *1,	FD=75KHz		0.1		%
De-emphasis Time Constant			75		μs
			50		μs
Audio Common-mode Voltage			0.9		V
Audio Output Load Resistance	Single-end	32			Ω

note *1 : VRF=60dBuV

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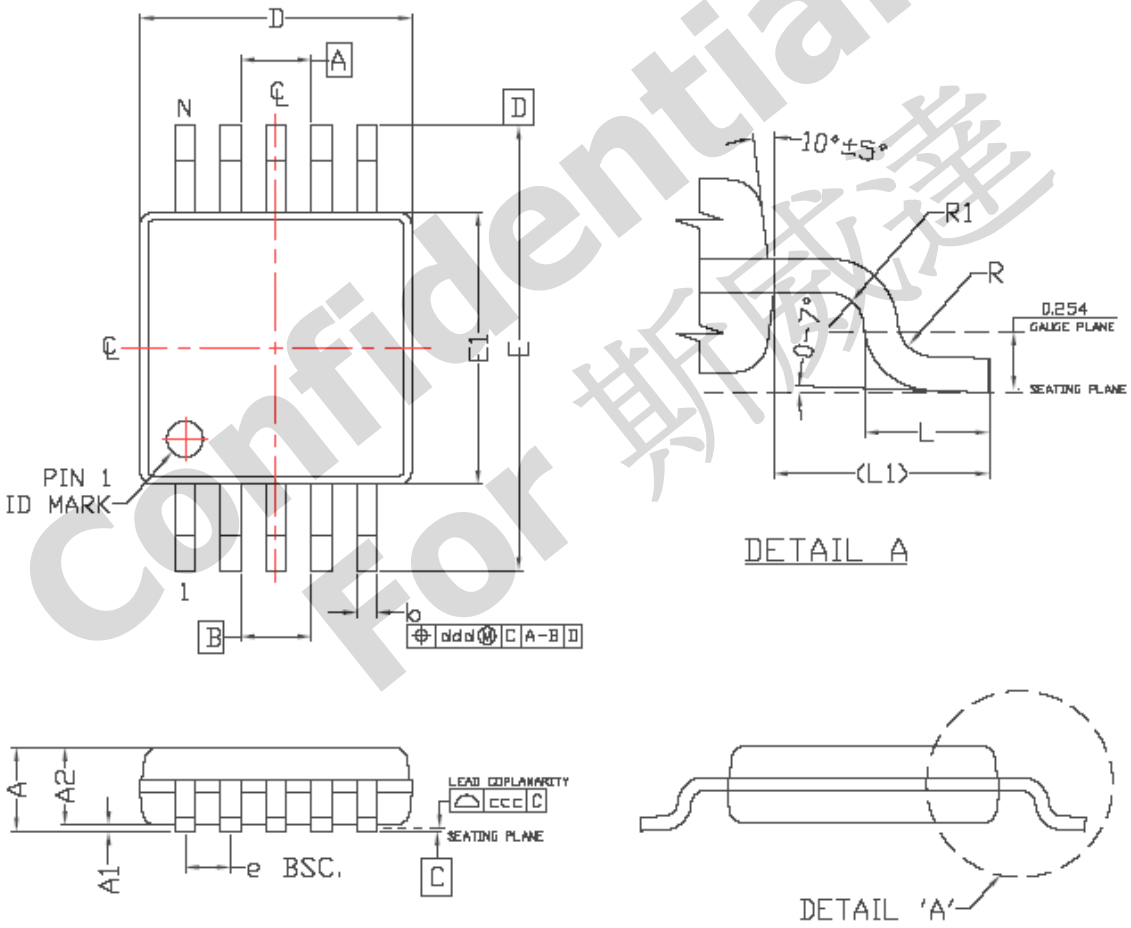
6 Package Dimension

Package:MSOP-10pin/3x4.9x1mm/0.5 pitch,



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SYMBOL	10L MSOP		
	MIN	NOM.	MAX.
A	--	--	1.10
A1	0.00	--	0.15
A2	0.75	0.85	0.95
b	0.17	--	0.33
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
R	0.07	--	--
R1	0.07	--	--
L	0.40	0.55	0.70
L1	0.95 REF		
e	0.50 BSC		
ddd	0.08		
ccc	0.10		
N	10		

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Notes:

1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH ,PROTRUSIONS OR GATE BURRS.
4. DIMENSION 'E1' DOES NOT INCLUDE INTERNAL FLASH OR PROTRUSION.
5. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION.
6. FOOT LENGTH "L" IS MEASURED AT GAGE PLANE,AT 0.254 ABOVE THE SEATING PLANE.

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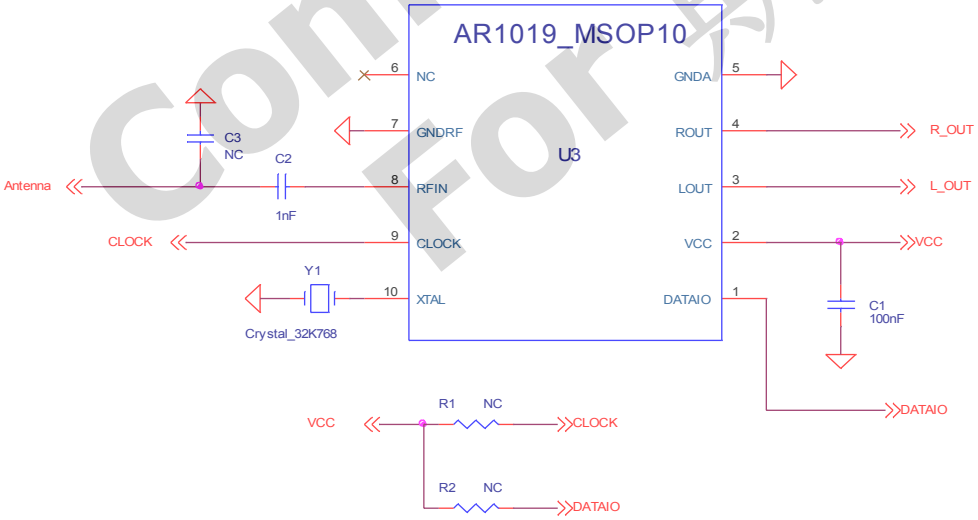
7 Schematic

1.9 Crystal solution



Note1: The pull-high resistors must be added on 2-wire CLOCK(pin9) & DATAIO(pin1) respectively.The 2.2K ohm is recommended for the pull-high resistors .
Note2: C1(100nF) must be as close to VCC(pin2) as possible.
Note3: The pin6 (NC) must be floating.
Note4: Please reserve C3 for fine tune.
Note5: Y1 must be as close to XTAL(pin10) as possible.

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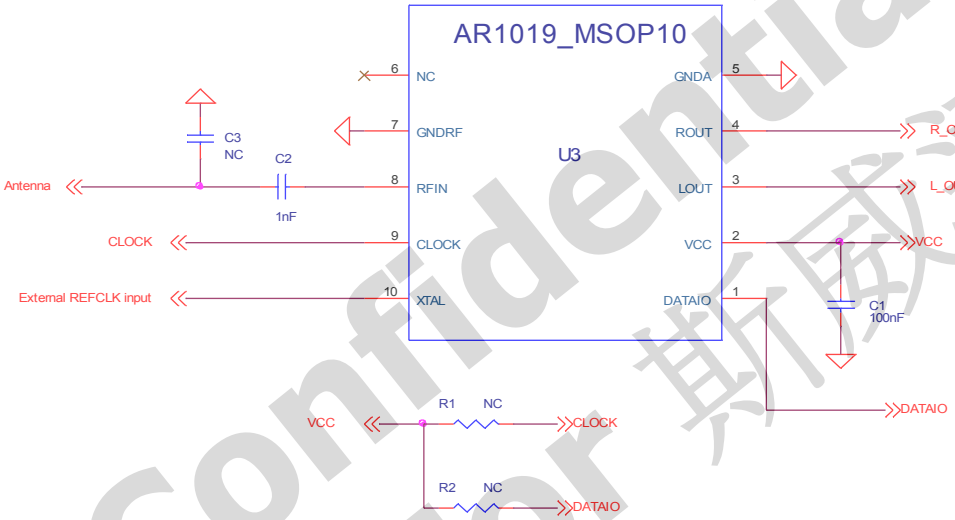
1.10 External REFCLK solution



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Note3: The pin6 (NC) must be floating.
Note4: Please reserve C3 for fine tune.

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