1. General Description

This 8-bit Micro-controller uses a fully static CMOS technology to achieve high speed, small size, low power and high noise immunity.

On chip memory includes 1 K words of Flash ROM, and 128 bytes of EEPROM, and 64 bytes of static RAM.

2. Features

- Fully CMOS static design
- 8-bit data bus
- On chip flash ROM size :
  MDT10F630 -- 1 K words
- Internal RAM size :
  MDT10F630 -- 64 bytes
  (64 general purpose registers)
- 128 bytes of EEPROM
- 37 single word instructions
- 14-bit instructions
- 8-level stacks
- Operating voltage : 2.3V ~ 5.5 V
- Watchdog timer with on-chip RC oscillator
- Interrupt capability
- Timer0 : 8-bit timer with 3-bit prescaler
- Timer1 : 16-bit timer with 2-bit prescaler
- One analog comparator module
- Sleep mode for power saving
- PA with port change wake-up interrupt
- Power-on Reset
- 12 I/O pins with their own independent direction control
- System input clock select at 4M or 8MHz

3. Applications

The application areas of this MDT10F630 range from appliance motor control and high speed automotive to low power remote transmitters/receivers, pointing devices, and telecommunications processors, such as Remote controller, small instruments, chargers, toy, automobile and PC peripheral … etc.

4. Pin Assignment

MDT10F630P11 (DIP)

MDT10F630S11 (SOP)

Vdd	1	14	Vss
OSC1/PA5	2	13	PA0/CIN+
OSC2/PA4	3	12	PA1/CIN-
PA3	4	11	PA2/INT
PC5	5	10	PC0
PC4	6	9	PC1
PC3	7	8	PC2

MDT10F630P13 (DIP)

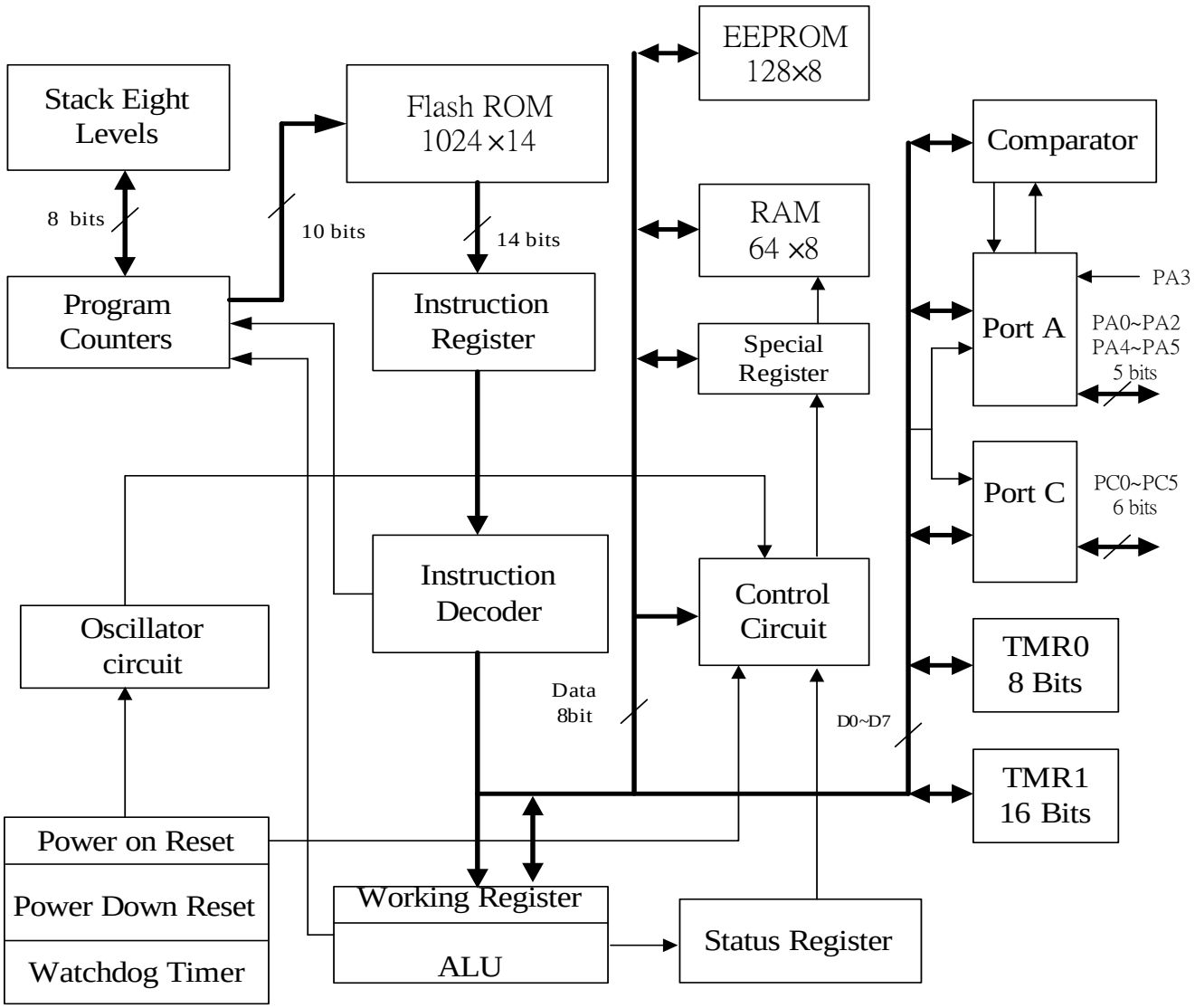
MDT10F630S13 (SOP)

Vdd	1	14	Vss
OSC1/PA5	2	13	PA0/CIN+
OSC2/PA4	3	12	PA1/CIN-
/MCLR	4	11	PA2/INT
PC5	5	10	PC0
PC4	6	9	PC1
PC3	7	8	PC2

5. Order Information

Device	ROM (Words)	RAM (Bytes)	EEPROM (Bytes)	I/O	Comparators	Timer (8/16 bit)	Package	Remark
MDT10F630P11	1.0K	64	128	12	1	1/1	14-DIP	Pin 4 is PA3 function
MDT10F630P13	1.0K	64	128	11	1	1/1	14-DIP	Pin 4 is /MCLR external reset function
MDT10F630S11	1.0K	64	128	12	1	1/1	14-SOP	Pin 4 is PA3 function
MDT10F630S13	1.0K	64	128	11	1	1/1	14-SOP	Pin 4 is /MCLR external reset function

6. Block Diagram

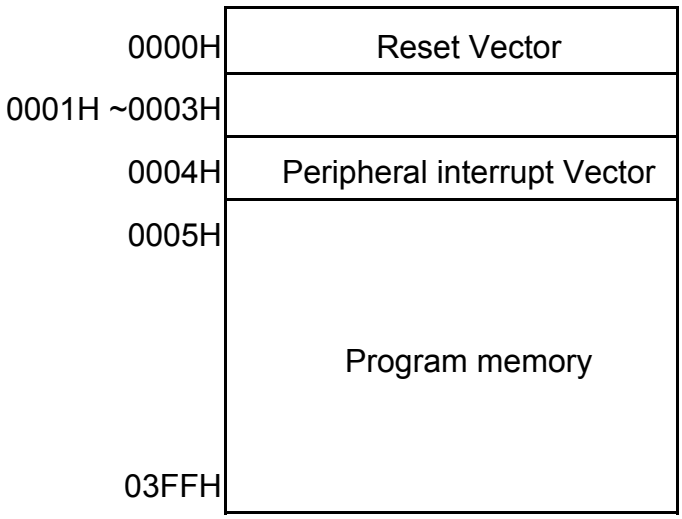


7. Pin Function Description

Pin Name	I/O	Function Description
PA0/CIN+	I/O	Port A, TTL input level, with program pull_hi and interrupt on pin change. Comparator input.
PA1/CIN-	I/O	Port A, TTL input level, with program pull_hi and interrupt on pin change. Comparator input.
PA2/T0CK/INT/COUT	I/O	Port A, ST input level, with program pull_hi and interrupt on pin change. Timer0 clock input. External interrupt. Comparator output.
PA3/$\overline{\text{MCLR}}$	I	Port A, TTL input level, with program interrupt on pin change. Master clear. Schmitt Trigger (ST) input level.
PA4/OSC2/T1G	I/O	Port A, TTL input level, with program pull_hi and interrupt on pin change. Oscillator crystal output, in RC mode clock output Fosc/4 frequency. Timer1 gate.
PA5/OSC1/T1CKI	I/O	Port A, TTL input level, with program pull_hi and interrupt on pin change. Oscillator crystal input/external clock source input. Timer1 clock input.
PC0 ~ 5	I/O	Port C, TTL input level.
Vdd		Power supply
Vss		Ground

8. Memory Map

8.1 Program memory :



8.2 Register file map :

Address	Description		Address
BANK 0			BANK 1
00	IAR	IAR	80
01	RTCC	TMR	81
02	PCL	PCL	82
03	STATUS	STATUS	83
04	MSR	MSR	84
05	PORT A	CPIO A	85
06			86
07	PORT C	CPIO C	87
08~09			88~89
0A	PCHLAT	PCHLAT	8A
0B	INTS	INTS	8B
0C	PIFB1	PIEB1	8C
0D			8D
0E	TMR1L	PSTA	8E
0F	TMR1H		8F
10	T1STA	INOSCR	90
11~14			91~94
15		PAPHR	95
16		PAINTR	96
17~18			97~98
19	CMSTA	VRSTA	99
1A		EEDATA	9A
1B		EEADR	9B
1C		EECON1	9C
1D		EECON2	9D
1E~1F			9E~9F
20~5F	64 General Register	Mapped in Bank 0	A0~DF
60~7F			E0~FF

Unimplemented memory location.

(1). 00H or 80H : IAR (Indirect Address Register)

Use contents of MSR to address data memory (not a physical register)

(2). 01H : RTCC (Timer0 Counter).

8-bit real time clock/counter

(3). 02H or 82H : PCL (Program Counter Low Byte)

Low order 8 bits of the Program Counter (PC)

(4). 03H or 83H : STATUS (Status register).

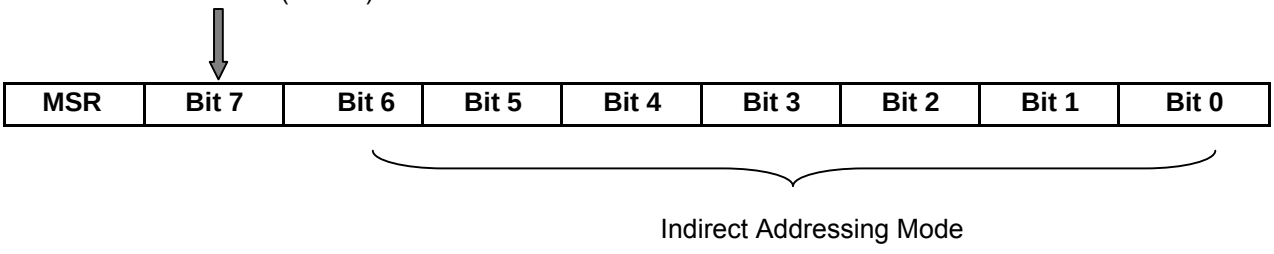
Bit	Symbol	Function
0	C	Carry bit
1	HC	Half Carry bit
2	Z	Zero bit
3	/PF	Power loss Flag bit
4	/TF	WDT time-out Flag bit
5	page	Register page select bit : 0 : 00H --- 7FH 1 : 80H --- FFH
6—7	——	General purpose bit

(5). 04H or 84H : MSR (Memory Select Register)

Memory Bank Select Register :

0 : 00~7F (Bank0)

1 : 80~FF (Bank1)



(6). 05H : Port A data output register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port A	**-**	**-**	**PA5**	**PA4**	**PA3**	**PA2**	**PA1**	**PA0**

Bit 7-6 : Unimplemented

Bit 5-0 : PA5~PA0, I/O Register

(7). 06H : Unimplemented Register.

(8). 07H : Port C data output register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port C	**-**	**-**	**PC5**	**PC4**	**PC3**	**PC2**	**PC1**	**PC0**

(9). 08 ~ 09H : Unimplemented Register.

(10). 0AH or 8AH : Program counter high byte.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCHLAT	**-**	**-**	**-**	**PCH4**	**PCH3**	**PCH2**	**PCH1**	**PCH0**

(11). 0BH or 8BH : Interrupt control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTS	**GIS**	**PEIE**	**TIS**	**INTS**	**PAIE**	**TIF**	**INTF**	**PAIF**

GIS : Global Interrupt Enable Bit.
0 = Disable all interrupts
1 = Enable all un-masked interrupts

PEIE : Peripheral Interrupt Enable Bit.
0 = Disable all peripheral interrupts
1 = Enable all peripheral interrupts

TIS : TMR0 Overflow Interrupt Enable Bit.
0 = Disable the Timer0 interrupt
1 = Enable the Timer0 interrupt

INTS : PA2/INT Interrupt Enable Bit.
0 = Disable the PA2/INT interrupt
1 = Enable the PA2/INT interrupt

PAIE : PA Port Change Interrupt Enable Bit.
0 = Disable the PA port change interrupt
1 = Enable the PA port change interrupt

TIF : TMR0 Overflow Interrupt Flag Bit.
0 = Timer0 did not overflowed
1 = Timer0 has overflowed (must be cleared in software)

INTF : PA2/INT Interrupt Flag Bit.
0 = The PA2/INT interrupt did not occur
1 = The PA2/INT interrupt occurred

PAIF : PA Port Change Interrupt Flag Bit.
0 = None of the PA5~0 pins have changed state
1 = When at least one of the PA5~0 pins changed state (must be cleared in software)

(12). 0CH : Peripheral interrupt register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIFB1	**EEIF**	**-**	**-**	**-**	**CMIF**	**-**	**-**	**TMR1IF**

EEIF : EEPROM Write Operation Interrupt Flag Bit.
0 = The EEPROM write operation is not completed or has not been start
1 = The EEPROM write operation completed (must be cleared in software)

CMIF : Comparator Interrupt Flag Bit.
0 = Comparator input has not changed
1 = Comparator input has changed (must be cleared in software)

TMR1IF : TMR1 Overflow Interrupt Flag Bit.
0 = Timer1 register did not overflow
1 = Timer1 register overflowed (must be cleared in software)

(13). 0DH : Unimplemented register.

(14). 0EH : TMR1L (The timer1 LSB register)
The LSB of the 16-bit TMR1.

(15). 0FH : TMR1H (The timer1 MSB register)
The MSB of the 16-bit TMR1.

(16). 10H : Timer1 control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1STA	**-**	**TMR1GE**	**T1CKPS1**	**T1CKPS1**	**T1OSCEN**	**/T1SYNC**	**TMR1CLK**	**TMR1ON**

TMR1GE : Timer1 Gate Enable Bit.
If TMR1ON = 0 this bit is ignored
If TMR1ON = 1
0 = Timer1 is on
1 = Timer1 is on if /T1G pin is low

T1CKPS1 & T1CKPS0: Timer1 Input Clock Prescale Select bits.
0 0 = 1 : 1 Prescale value
0 1 = 1 : 2 Prescale value
1 0 = 1 : 4 Prescale value
1 1 = 1 : 8 Prescale value

T1OSCEN : LF Oscillator Enable Bit.
If INTOSC without CLKOUT oscillator is active :
0 = LP oscillator is off
1 = LP oscillator is enabled for Timer1 clock

/T1SYNC : Timer1 External Clock Input Synchronization Control Bit.
If TMR1CLK = 0 this bit is ignored
Timer1 use internal clock
If TMR1CLK = 1

0 = Synchronize external clock input
1 = Do not synchronize external clock input

TMR1CLK : Timer1 Clock Source Select Bit.
0 = Select internal clock Fosc/4
1 = Select External clock from T1CKI pin (on rising edge)

TMR1ON : TMR1 On Bit.
0 = Stop Timer1
1 = Enable Timer1

(17). 11 ~ 18H : Unimplemented register.

(18). 19H : Comparator control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMSTA	**-**	**CMOUT**	**-**	**CMOINV**	**CMIS**	**CMP2**	**CMP1**	**CMP0**

CMOUT : Comparator Output Bit.
When CMOINV = 0
1 = Vin+ > Vin- ; 0 = Vin+ < Vin-
When CMOINV = 1
1 = Vin+< Vin- ; 0 = Vin+ > Vin-

CMOINV: Comparator Output Inversion Bit.
0 = Output not inverted
1 = Output inverted

CMIS: Comparator Input Switch Bit.
When CMP2 ~ 0 = 110 or 101 :
0 = Vin- connects to CIN-
1 = Vin- connects to CIN+

CMP2 ~ 0: Comparator Mode Bits.
0 0 0 = Comparator reset (POR default value – low power)
0 0 1 = Comparator with output
0 1 0 = Comparator without output
0 1 1 = Comparator with output and internal reference (Cvref in 99H register)
1 0 0 = Comparator without output and with internal reference (Cvref in 99H register)
1 0 1 = Comparator multiplexed input with internal reference (Cvref in 99H register) and output
1 1 0 = Comparator multiplexed input with internal reference (Cvref in 99H register)
1 1 1 = Comparator off (lowest power)

(19). 1A ~ 1FH : Unimplemented register.

(20). 81H : Option control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR	**/PAPH**	**IES**	**TCS**	**TCE**	**PSC**	**PS2**	**PS1**	**PS0**

Bit	Symbol	Function		
		Prescaler Value	TMR0 rate	WDT rate
2—0	PS2—0	0 0 0	1 : 2	1 : 1
		0 0 1	1 : 4	1 : 2
		0 1 0	1 : 8	1 : 4
		0 1 1	1 : 16	1 : 8
		1 0 0	1 : 32	1 : 16
		1 0 1	1 : 64	1 : 32
		1 1 0	1 : 128	1 : 64
		1 1 1	1 : 256	1 : 128
3	PSC	Prescaler assignment bit : 0 — TMR0 1 — Watchdog Timer		
4	TCE	TMR0 signal Edge : 0 — Increment on low-to-high transition on PA2 pin 1 — Increment on high-to-low transition on PA2 pin		
5	TCS	TMR0 signal set : 0 — Internal instruction cycle clock 1 — Transition on PA2/INT pin		
6	IES	PA2 interrupt edge select bit : 0 — Interrupt on falling edge of PA2/INT pin 1 — Interrupt on rising edge of PA2/INT pin		
7	/PAPH	Port A Pull-up Enable Bit : 0 — PA0~2 & PA4~5 pull-up all enable 1 — PA0~2 & PA4~5 pull-up all disable		

(21). 85H : Port A input/output control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPIO A	**-**	**-**	**CPIO PA5**	**CPIO PA4**	**CPIO PA3**	**CPIO PA2**	**CPIO PA1**	**CPIO PA0**

(22). 86H : Unimplemented register.

(23). 87H : Port A input/output control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPIO C	**-**	**-**	**CPIO PC5**	**CPIO PC4**	**CPIO PC3**	**CPIO PC2**	**CPIO PC1**	**CPIO PC0**

(24). 88 ~ 89H : Unimplemented register.

(25). 8CH : Peripheral interrupt enable register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIEB1	**EEIE**	**-**	**-**	**-**	**CMIE**	**-**	**-**	**TMR1IE**

EEIE : EEPROM Write Operation Interrupt Enable Bit.
0 = Disable the EEPROM write complete interrupt
1 = Enable the EEPROM write complete interrupt

CMIE : Comparator Interrupt Enable Bit.
0 = Disable the comparator interrupt
1 = Enable the comparator interrupt

TMR1IE : TMR1 Overflow Interrupt Enable Bit.
0 = Disable the TMR1 overflow interrupt
1 = Enable the TMR1 overflow interrupt

(26). 8DH : Unimplemented register.

(27). 8EH : Power control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSTA	-	-	-	-	-	-	PORB	PEDHB

PEDHB : Power Detect High Level Status Bit.
0 = A PED high level reset occurred (must be set in software after a power on reset occurs)
1 = No PED high level reset occurred

PORB : Power On Reset Status Bit.
0 = A power on reset occurred (must be set in software after a power on reset occurs)
1 = No power on reset occurred

(28). 8FH : Unimplemented register.

(29). 90H : MCU oscillator control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INOSCR	REG	OPRLC	OPRC	EN8M	ECKIN	OSO2E	OSC2O	/OSCIN

Bit 7 : Normal register bits.

OPRLC : OP RC Mode Lower Work Current Enable Bit.
0 = Disable
1 = Enable

OPRC : OP RC Mode Enable Bit.
0 = Disable
1 = Enable

EN8M : Internal 4MHz Oscillator Clock Double Enable Bit.
0 = System clock input is internal RC 4MHz
1 = System clock input is 8MHz (internal RC 4MHz frequency double)

ECKIN : External Clock Input Enable Bit.
0 = Disable oscillator external clock input
1 = Enable oscillator external clock input (must be set in external oscillator of RC mode)

OSO2E : Both of Internal and external oscillator Enable Bit.
0 = Only use internal oscillator or external oscillator
1 = Internal and external (LF mode only) oscillator enable both

OSC2O : OSC2/PA4 Oscillator Clock Output Enable Bit.
0 = Disable OSC2/PA4 oscillator clock output in internal or external of RC mode oscillator
1 = Enable OSC2/PA4 oscillator clock output in internal or external of RC mode oscillator

OSCIN : MCU Internal Or external oscillator Select Bit.
0 = Default the MCU clock based on internal 4MHz oscillator
1 = The MCU clock based on external oscillator (type from option select),
When internal 4MHz oscillator change to external oscillator must wait OST time 20ms.

(30). 91 ~ 94H : Unimplemented register.

(31). 95H : Port A pull_hi control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAPHR	-	-	PAH5	PHA4	-	PHA2	PHA1	PHA0

Bit 5-4 & Bit 2-0 : Port A Pull_hi Control Bits
0 = Pull_hi disable
1 = Pull_hi enable

(32). 96H : Port A interrupt-on-change control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAINTR	-	-	PINTA5	PINTA4	PINTA3	PINTA2	PINTA1	PINTA0

Bit 5-0 : Port A Interrupt-On-Change Control Bits
0 = Interrupt-on-change disable
1 = Interrupt-on-change enable

(33). 97 ~ 98H : Unimplemented register.

(34). 99H : Voltage reference control register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VRSTA	CVREN	-	CVRRS	-	CVR3	CVR2	CVR1	CVR0

Bit 7 : Comparator Voltage Reference Enable Bit
0 = Comparator voltage reference disable
1 = Comparator voltage reference enable

Bit 5 : Comparator Voltage Reference Range Select Bit
0 = High range ; CVref = Vdd/4 + (CVR3:CVR0/32)*Vdd
1 = Low range ; CVref = (CVR3:CVR0/24)*Vdd

Bit 3-0 : Comparator Voltage Reference Value Selection
When CVRRS = 0, CVref = Vdd/4 + (CVR3:CVR0/32)*Vdd
When CVRRS = 1, CVref = (CVR3:CVR0/24)*Vdd

(35). 9AH : EEPROM data register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEDATA	EED7	EED6	EED5	EED4	EED3	EED2	EED1	EED0

(36). 9BH : EEPROM address register.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEADR	-	EEAD6	EEAD5	EEAD4	EEAD3	EEAD2	EEAD1	EEAD0

(37). 9CH : EEPROM control register 1.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EECON1	-	-	-	-	WRERR	WREN	WR	RD

Bit 7~4 is unimplemented : Read as “0”

WRERR : EEPROM Write Error Flag Bit.
0 = The EEPROM write operation completed
1 = The EEPROM write operation is prematurely terminated
(any MCLR reset or any WDT reset during normal operation)

WREN : EEPROM Write Enable Bit.
0 = Inhibits write to the data EEPROM
1 = Allows write cycles

WR : Write Control Bit.
0 = Write cycle to the data EEPROM is complete
1 = Initiates a write cycle. (The bit is cleared by hardware once write is complete. The WR bit can only be set (not clear) in software.)

RD : Read Control Bit.
0 = Does not initiate an EEPROM read.
1 = Initiates an EEPROM read (read takes once cycle. RD is cleared in hardwave. The RD bit can only be set (not clear) in software.)

(38). 9DH : EEPROM control register 2.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EECON2	-	-	-	-	-	-	-	-

Write only ; Read as “0”

When write data to the EEPROM must write 55/H to EECON2, and writ AA/H to EECON2 then set WR bit; the EEPROM can write data inside for write each byte.

Example : Data EEPROM Write

```
BSR     STATUS, PAGE    ; Select bank1
BCR     INTS, GIS       ; Disable interrupt
BSR     EECON1, WREN    ; Enable write
LDWI    55H
STWR    EECON2          ; Write 55/H
LDWI    0AAH
STWR    EECON2          ; Write AA/H
BSR     EECON1, WR      ; Begin write
```

(39). 9E ~ 9FH : Unimplemented register.

9. Reset Condition for all Registers

Register	Address	Power-On Reset, Power range detector Reset	/MCLR or WDT Reset	Wake-up from SLEEP
IAR	00h(80h)	0000 0000	0000 0000	uuuu uuuu
RTCC	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h(82h)	0000 0000	0000 0000	0000 0100
STATUS	03h(83h)	0001 1xxx	000# #uuu	000# #uuu
MSR	04h(84h)	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORT A	05h	--xx xxxx	--uu uuuu	--uu uuuu
PORT C	07h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCHLAT	0Ah(8Ah)	---0 0000	---0 0000	---u uuuu
INTS	0Bh(8Bh)	0000 0000	0000 0000	uuuu uuuu
PIFB1	0Ch	0--- 0--0	0--- 0--0	u--- u--u
TMR1L	0Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	0Fh	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1STA	10h	-000 0000	-000 0000	-uuu uuuu
CMSTA	19h	-0-0 0000	-0-0 0000	-u-u uuuu
TMR	81h	1111 1111	1111 1111	uuuu uuuu
CPIO A	85h	--11 1111	--11 1111	--uu uuuu
CPIO C	87h	1111 1111	1111 1111	uuuu uuuu
PIEB1	8Ch	0--- 0--0	0--- 0--0	u--- u--u
PSTA	8Eh	---- --##	---- --uu	---- --uu
INOSCR	90h	-000 0000	-000 0000	-uuu uuuu
PAPHR	95h	--11 -111	--11 -111	--uu -uuu
PAINTR	96h	--00 0000	--00 0000	--uu uuuu
VRSTA	99h	0-0- 0000	0-0- 0000	u-u- uuuu
EEDATA	9Ah	0000 0000	0000 0000	uuuu uuuu
EEADR	9Bh	-000 0000	-000 0000	-uuu uuuu
EECON1	9Ch	---- x000	---- #000	---- #uuu
EECON2	9Dh	---- ----	---- ----	---- ----

Note : " x "＝unknown; " u "＝unchanged; " – "＝unimplemented, read as "0"; "# "＝value depends on condition

10. Instruction Set

Instruction Code	Mnemonic Operands	Function	Operation	Status
010000 00000000	NOP	No operation	None	
010000 00000001	CLRWT	Clear Watchdog timer	0→WT	/TF, /PF
010000 00000010	SLEEP	Sleep mode	0→WT, stop OSC	/TF, /PF
010000 00000011	TMODE	Load W to TMODE register	W→TMODE	None
010000 00000rrr	CPIO R	Control I/O port register	W→CPIO r	None
010001 1rrrrrrr	STWR R	Store W to register	W→R	None
011000 trrrrrrr	LDR R, t	Load register	R→t	Z
111010 iiiiiiii	LDWI I	Load immediate to W	I→W	None
010111 trrrrrrr	SWAPR R, t	Swap halves register	[R(0~3) ↔ R(4~7)]→t	None
011001 trrrrrrr	INCR R, t	Increment register	R + 1→t	Z
011010 trrrrrrr	INCRSZ R, t	Increment register, skip if zero	R + 1→t	None
011011 trrrrrrr	ADDWR R, t	Add W and register	W + R→t	C, HC, Z
011100 trrrrrrr	SUBWR R, t	Subtract W from register	R – W→t (R+/W+1→t)	C, HC, Z
011101 trrrrrrr	DECR R, t	Decrement register	R – 1→t	Z
011110 trrrrrrr	DECRSZ R, t	Decrement register, skip if zero	R – 1→t	None
010010 trrrrrrr	ANDWR R, t	AND W and register	R ∩ W→t	Z
110100 iiiiiiii	ANDWI I	AND W and immediate	I ∩ W→W	Z
010011 trrrrrrr	IORWR R, t	Inclu. OR W and register	R ∪ W→t	Z
110101 iiiiiiii	IORWI I	Inclu. OR W and immediate	I ∪ W→W	Z
010100 trrrrrrr	XORWR R, t	Exclu. OR W and register	R ⊕ W→t	Z
110110 iiiiiiii	XORWI I	Exclu. OR W and immediate	I ⊕ W→W	Z
011111 trrrrrrr	COMR R, t	Complement register	/R→t	Z
010110 trrrrrrr	RRR R, t	Rotate right register	R(n) →R(n-1), C→R(7), R(0)→C	C
010101 trrrrrrr	RLR R, t	Rotate left register	R(n)→r(n+1), C→R(0), R(7)→C	C

Instruction Code	Mnemonic Operands	Function	Operation	Status
010000 1xxxxxxx	CLRW	Clear working register	0→W	Z
010001 0rrrrrrr	CLRR R	Clear register	0→R	Z
0000bb brrrrrrr	BCR R, b	Bit clear	0→R(b)	None
0010bb brrrrrrr	BSR R, b	Bit set	1→R(b)	None
0001bb brrrrrrr	BTSC R, b	Bit Test, skip if clear	Skip if R(b)=0	None
0011bb brrrrrrr	BTSS R, b	Bit Test, skip if set	Skip if R(b)=1	None
100nnn nnnnnnnn	LCALL N	Long CALL subroutine	N→PC, PC+1→Stack	None
101nnn nnnnnnnn	LJUMP N	Long JUMP to address	N→PC	None
110001 iiiiiiii	RTIW I	Return, place immediate to W	Stack→PC, I→W	None
110111 iiiiiiii	ADDWI I	Add immediate to W	PC+1→PC, W+I→W	C,HC,Z
111000 iiiiiiii	SUBWI I	Subtract W from immediate	I-W→W	C,HC,Z
010000 00001001	RTFI	Return from interrupt	Stack→PC, 1→GIS	None
010000 00000100	RET	Return from subroutine	Stack→PC	None

Note :

W	:	Working register	b	:	Bit position
WT	:	Watchdog timer	t	:	Target
TMODE	:	TMODE mode register	0	:	Working register
CPIO	:	Control I/O port register	1	:	General register
/TF	:	Timer overflow flag	R	:	General register address
/PF	:	Power loss flag	C	:	Carry flag
PC	:	Program Counter	HC	:	Half carry
OSC	:	Oscillator	Z	:	Zero flag
Inclu.	:	Inclusive ‘∪’	/	:	Complement
Exclu.	:	Exclusive ‘⊕’	x	:	Don’t care
AND	:	Logic AND ‘∩’	I	:	Immediate data (8 bits)
			N	:	Immediate address