3/4-Cell Lithium-Ion/Polymer Protector

Features

- High Detection Accuracy
  - -Over-charge Detection: ±25mV
  - -Over-discharge Detection: ±80mV
  - -Discharge Over-current Detection: ±25mV
- Discharge Over-current Protection
- High Withstand Voltage
  - -Absolute maximum ratings: 40V (VDD – VSS)
- Low Supply Current
  - -Supply current: 9μA (Typ.)
  - -Standby current: 0.1μA (Max.) (Power Down Mode)
- Three Types of Current Protections
- Ultra Small Package
  - -TSSOP-16L

Description

The NT1775 protects lithium-ion/lithium-polymer rechargeable battery in the abnormal events of over-charge, over-discharge, discharging over-current and for a 3/4-cell lithium-ion/lithium polymer battery pack.

If any of above abnormal conditions occurred. NT1775 would turn off the MOSFETs to protect battery.

NT1775 would enter power down mode when over-discharge protection occurs to minimize the current consumption.

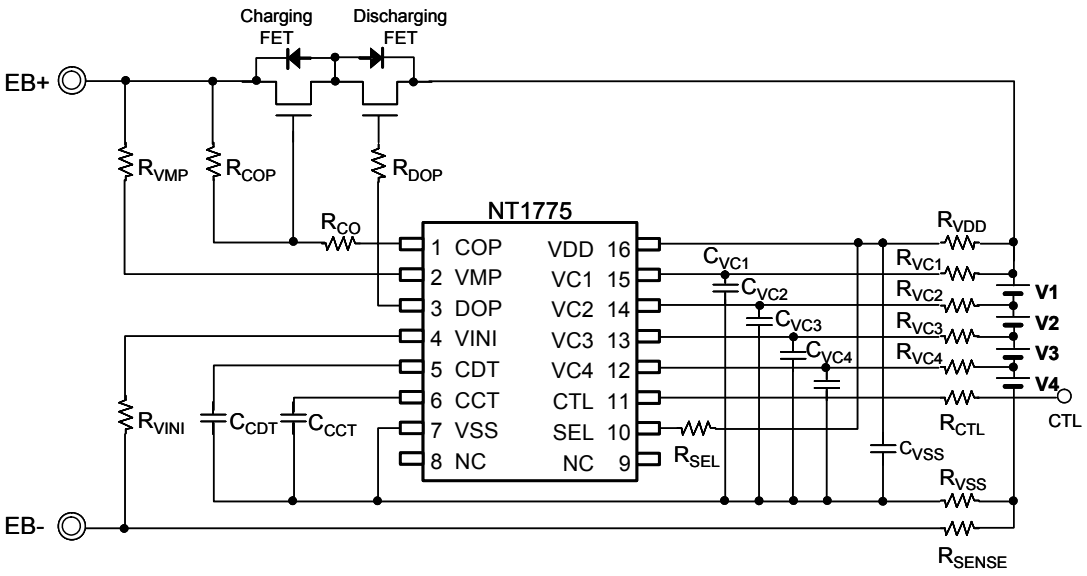
In general, NT1775 can be restored to normal mode after short-circuit or reversely charging is removed. To avoid hiccup reaction as protection is activated due to the serious short-circuit and reversely-charging conditions, NT1775 may enter power down mode sometimes. It can be awaked with charger reconnection.

The tiny package of 16 pin TSSOP is especially suitable for the battery packs in portable devices.

Applications

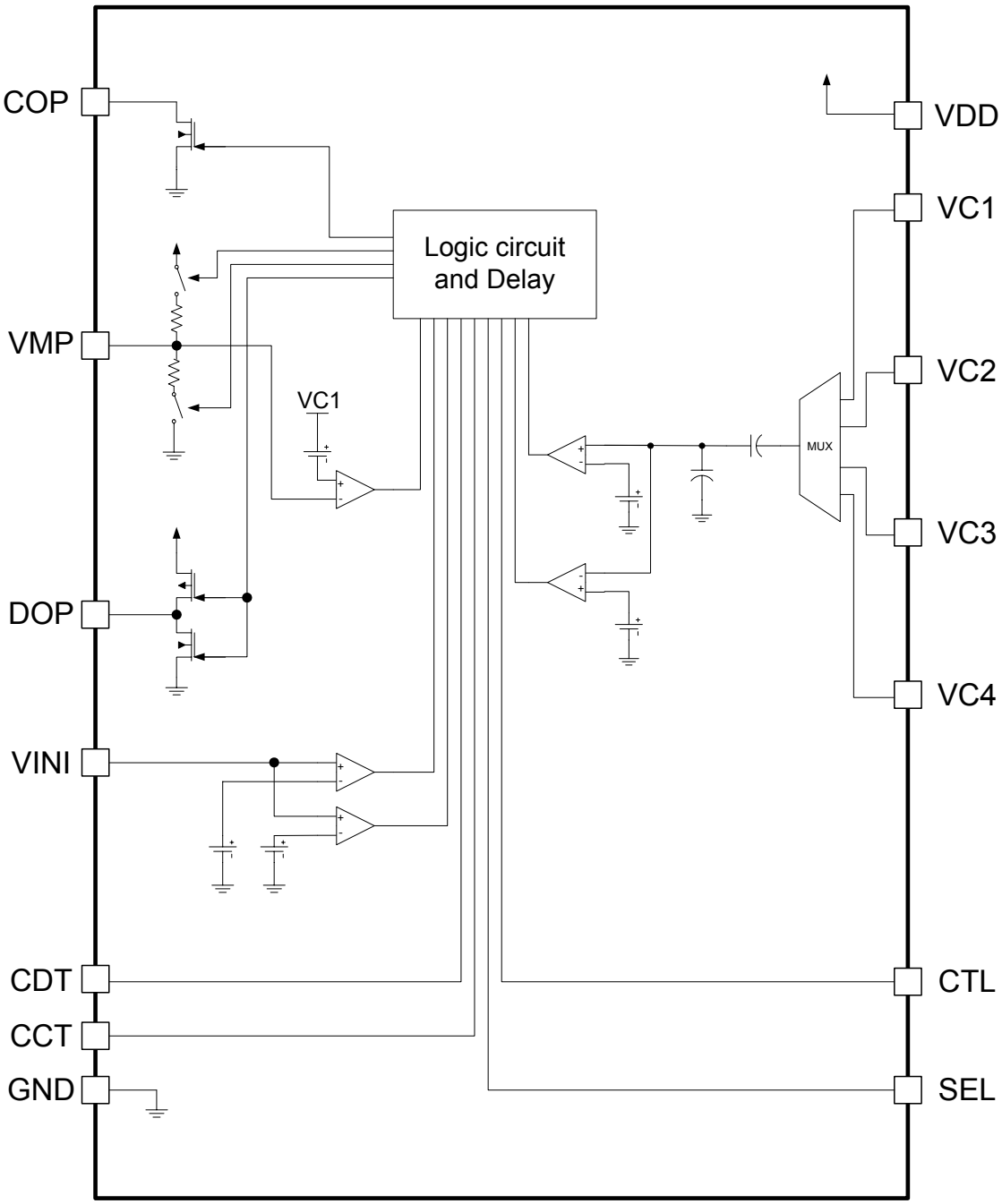
- Lithium-ion rechargeable battery packs
- Lithium-polymer rechargeable battery packs

Typical Application Circuit



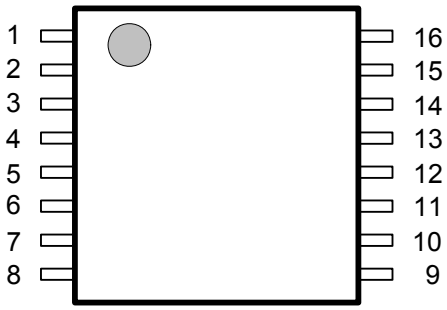
These devices have limited build-in ESD protection. The leads must be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Block Diagram



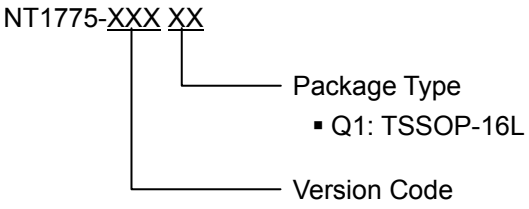
Package and Pin Configurations

16-Pin TSSOP
Top view



<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Pin description</th></tr>
<tr><td>1</td><td>COP</td><td>FET gate control pin for charging path (Nch open-drain output)</td></tr>
<tr><td>2</td><td>VMP</td><td>Voltage detction pin between VC1 and VMP (Short-circuit detection pin)</td></tr>
<tr><td>3</td><td>DOP</td><td>FET gate control pin for discharging path (CMOS output)</td></tr>
<tr><td>4</td><td>VINI</td><td>Voltage detction pin between VSS and VINI (Over-current 1,2 detection pin)</td></tr>
<tr><td>5</td><td>CDT</td><td>Capacitor connection for over-discharge detection, over-current detection 1 delay time</td></tr>
<tr><td>6</td><td>CCT</td><td>Capacitor connection for over-charge detection delay time</td></tr>
<tr><td>7</td><td>VSS</td><td>Negative power input pin</td></tr>
<tr><td>8</td><td>NC</td><td>No connection</td></tr>
<tr><td>9</td><td>NC</td><td>No connection</td></tr>
<tr><td>10</td><td>SEL</td><td>Pin for switching 3cell/4cell series
SEL pin=VSS: 3cell, SEL pin=VDD: 4cell</td></tr>
<tr><td>11</td><td>CTL</td><td>Control of charge FET and discharge FET
<table>
<tr><th>CTL Pin</th><th>COP Pin</th><th>DOP Pin</th></tr>
<tr><td>High</td><td>Hi-Z</td><td>VDD</td></tr>
<tr><td>Open</td><td>Hi-Z</td><td>VDD</td></tr>
<tr><td>Low</td><td>Normal status*</td><td>Normal status*</td></tr>
</table></td></tr>
<tr><td>12</td><td>VC4</td><td>Cell V4 positive voltage and cell 3 negative voltage input pin</td></tr>
<tr><td>13</td><td>VC3</td><td>Cell V3 positive voltage and cell 2 negative voltage input pin</td></tr>
<tr><td>14</td><td>VC2</td><td>Cell V2 positive voltage and cell 1 negative voltage input pin</td></tr>
<tr><td>15</td><td>VC1</td><td>Cell V1 positive voltage input pin</td></tr>
<tr><td>16</td><td>VDD</td><td>Power supply input pin</td></tr>
</table>

Ordering Information

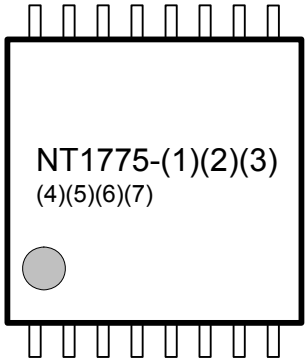


Product version code

Product Name	Version Code	Package Type	Over-charge Detection Voltage (V_{OV})	Over-charge Release Voltage (V_{REL1})	Over-discharge Detection Voltage (V_{OD})	Over-discharge Release Voltage (V_{REL2})	Discharge Over-current Detection Voltage 1 (V_{DOC1})	0V Battery Charge Function
NT1775	GNG	Q1	4.300V	4.150V	2.4V	3.0V	0.20V	Available

Marking Information

16-Pin TSSOP
Top view



(1)(2)(3) : Version Code

(4)(5)(6)(7) : Lot Number

Product name	Version code : (1)(2)(3)
NT1775-GNGQ1	GNG

Absolute Maximum Ratings

(Ta = 25°C unless otherwise specified)

Symbol	Descriptions	Rating	Unit
V_{DS}	Input voltage between VDD and VSS	VSS – 0.3 to VSS + 40	V
V_{IN}	Input voltage of (VC1-GND), (VC2-GND), (VC3-GND)	VSS – 0.3 to VDD + 0.3	V
	Input voltage of (VC1-VC2), (VC2-VC3), (VC3-VC4), (VC4-GND)	VSS – 0.3 to VSS + 8.0	V
	Input voltage range of CTL and SEL pin	VSS – 0.3 to VDD + 0.3	V
	Input voltage range of CCT, CDT and VINI pin	VSS – 0.3 to VSS + 8.0	V
V_{VMP}	Input voltage range of VMP pin	VSS – 0.3 to VSS + 40	V
V_{CO}	Output voltage range of COP pin	VSS – 0.3 to VSS + 40	V
V_{DO}	Output voltage range of DOP pin	VSS – 0.3 to VDD + 0.3	V
P_D	Power Dissipation	400	mV
T_{OPT}	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature range	-40 to 125	°C

Applying any over "Absolute Maximum Ratings" practice can permanently damage the device. These data are indicated the absolute maximum values only but not implied any operating performance.

Electrical Characteristics

(Ta = 25°C unless otherwise specified)

Symbol	Item	Conditions	MIN	TYP	MAX	Unit
Detection Voltage						
V_{OV}	Over-charge detection voltage	–	V_{OV} -0.025	V_{OV}	V_{OV} +0.025	V
V_{REL1}	Over-charge release voltage	–	V_{REL1} -0.050	V_{REL1}	V_{REL1} +0.050	V
V_{OD}	Over-discharge detection voltage	–	V_{OD} -0.080	V_{OD}	V_{OD} +0.080	V
V_{REL2}	Over-discharge release voltage	–	V_{REL2} -0.100	V_{REL2}	V_{REL2} +0.100	V
V_{DOC1}	Discharge over-current detection voltage 1	–	V_{DOC1} -0.025	V_{DOC1}	V_{DOC1} +0.025	V
V_{DOC2}	Discharge over-current detection voltage 2	–	0.4	0.5	0.6	V
V_{SHORT}	Short-circuit detection voltage	VC1 reference	-1.5	-1.2	-0.9	V
Delay Time						
t_{OV}	Output delay time of over-charge	CCT pin capacitance=0.1μF	0.5	1.0	1.5	s
t_{OD}	Output delay time of over-discharge	CDT pin capacitance=0.1μF	50	100	150	ms
t_{DOC1}	Output delay time of discharge over current 1	CDT pin capacitance=0.1μF	5	10	15	ms
t_{DOC2}	Output delay time of discharge over current 2	–	0.4	1.0	1.6	ms
t_{SHORT}	Output delay time of short-circuit detection	FET gate capacitance=2000pF	50	300	600	μs

Electrical Characteristics (continued)

(Ta = 25°C unless otherwise specified)

Symbol	Item	Conditions	MIN	TYP	MAX	Unit
Current Consumption						
I_{DD}	Supply current	V1=V2=V3=V4=3.5V	—	9	15	μA
I_{PDN}	Current consumption at power down	V1=V2=V3=V4=1.5V	—	—	0.1	μA
I_{VC1}	VC1 pin current	V1=V2=V3=V4=3.5V	-0.3	0.5	1	μA
I_{VC2}	VC2 pin current	V1=V2=V3=V4=3.5V	-0.3	0	0.3	μA
I_{VC3}	VC3 pin current	V1=V2=V3=V4=3.5V	-0.3	0	0.3	μA
I_{VC4}	VC4 pin current	V1=V2=V3=V4=3.5V	-0.3	0	0.3	μA
I_{CTLH}	CTL pin current “H”	V1=V2=V3=V4=3.5V, V_{CTL}=VDD	—	—	0.1	μA
I_{CTLL}	CTL pin current “L”	V1=V2=V3=V4=3.5V, V_{CTL}=VSS	-0.8	—	—	μA
I_{SELH}	SEL pin current “H”	V1=V2=V3=V4=3.5V, V_{SEL}=VDD	—	—	0.1	μA
I_{SELL}	SEL pin current “L”	V1=V2=V3=V4=3.5V, V_{SEL}=VSS	-0.1	—	—	μA
Input Voltage						
V_{DSOP}	Operating voltage between VDD and VSS	Output voltage of COP and DOP fixed	4.0	—	26.0	V
V_{CTLH}	CTL input voltage “H”	—	2.7	—	—	V
V_{CTLL}	CTL input voltage “L”	—	—	—	1.0	V
V_{SELH}	SEL input voltage “H”	—	VDD×0.8	—	—	V
V_{SELL}	SEL input voltage “L”	—	—	—	VDD×0.2	V
0V Battery Charging Function						
V_{0CHA}	0V battery charge starting charger voltage	0V battery charging available	—	1.6	2.0	V
Output Current						
I_{COH}	COP pin leakage current	V_{COP}=24V	—	—	0.1	μA
I_{COL}	COP pin sink current	V_{COP}=VSS+0.5V	10	—	—	μA
I_{DOH}	DOP pin source current	V_{DOP}=VDD-0.5V	10	—	—	μA
I_{DOL}	DOP pin sink current	V_{DOP}=VSS+0.5V	10	—	—	μA
VMP Internal Resistance						
R_{VMD}	Internal resistance between VMP and VDD	V1=V2=V3=V4=3.5V	0.5	1.0	1.5	MΩ
R_{VMS}	Internal resistance between VMP and V_{SS}	V1=V2=V3=V4=1.8V	450	900	1800	KΩ

Measurement Methods

(1) Power consumption (Measurement circuit 1)

1) Set V1=V2=V3=V4=3.5V, S1=ON and S2=OFF, enter normal condition.
2) The measured current at VSS pin is the supply current (I_{DD}).
3) Set V1=V2=V3=V4=1.5V, S1=OFF and S2=ON, enter power down mode.
4) The measured current at VSS pin is the current consumption at power down (I_{PDN}).

(2) Over-charge detection and release voltage (Measurement circuit 2)

1) Set V1=V2=V3=V4=3.5V, V_{VMP}=V_{SEL}=VDD, V_{VINI}=V_{CTL}=0V and S1=OFF, enter normal condition.
2) Initialize V1 voltage from 3.5V and increase gradually. The V1 voltage is the over-charge detection voltage (V_{OV}) when COP pin switches from low to high.
3) Decrease V1 gradually. The V1 voltage is the over-charge release detection voltage (V_{REL1}) when COP pin switches from high to low.
4) When the voltage of Vn (n=2 to 4) is changed. The over-charge detection/release voltage can be determined in the same way as when n=1.

(3) Over-discharge detection and release voltage (Measurement circuit 2)

1) Set V1=V2=V3=V4=3.5V, V_{VMP}=V_{SEL}=VDD, V_{VINI}=V_{CTL}=0V and S1=OFF, enter normal condition.
2) Decrease V1 voltage from 3.5V gradually. The V1 voltage is the over-discharge detection voltage (V_{OD}) when DOP pin switches from low to high.
3) Increase V1 gradually. When DOP pin switches from high to low, the V1 voltage is the over-discharge release detection voltage (V_{REL2}).
4) When the voltage of Vn (n=2 to 4) is changed. The over-discharge detection/release voltage can be determined in the same way as when n=1.

(4) Discharge over-current detection voltage 1 (Measurement circuit 2)

1) Set V1=V2=V3=V4=3.5V, V_{VMP}=V_{SEL}=VDD, V_{VINI}=V_{CTL}=0V and S1=OFF, enter normal condition.
2) Initialize V_{VINI} from 0V and increase gradually. When both COP and DOP pins switch from low to high, the V_{VINI} voltage is the discharge over-current detection voltage 1(V_{DOC1}).

(5) Discharge over-current detection voltage 2 (Measurement circuit 2)

1) Set V1=V2=V3=V4=3.5V, V_{VMP}=V_{SEL}=VDD, V_{VINI}=V_{CTL}=0V and S1=ON, enter normal condition.
2) Initialize V_{VINI} from 0V and increase gradually. When both COP and DOP pins switch from low to high, the V_{VINI} voltage is the discharge over-current detection voltage 2(V_{DOC2}).

(6) Short-circuit detection voltage (Measurement circuit 2)

1) Set V1=V2=V3=V4=3.5V, V_{VMP}=V_{SEL}=VDD, V_{VINI}=V_{CTL}=0V and S1=OFF, enter normal condition.
2) Initialize V_{VMP} from VDD and decrease gradually. When both COP and DOP pins switch from low to high, the voltage of (V_{VMP} -V_{VC1}) is the short-circuit detection voltage (V_{SHORT}).

(7) CTL input voltage "H" and "L" (Measurement circuit 2)

1) Set V1=V2=V3=V4=3.5V, V_{VMP}=V_{SEL}=VDD, V_{VINI}=V_{CTL}=0V and S1=OFF, enter normal condition.
2) Initialize V_{CTL} from 0V and increase gradually. When both COP and DOP pins switch from low to high, the V_{CTL} voltage is the CTL input voltage "H" (V_{CTLH}).
3) Decrease V_{CTL} from VDD gradually. When both COP and DOP pins switch from high to Low, the V_{CTL} is the CTL input voltage "L" (V_{CTLL}).

(8) SEL input voltage "H" and "L" (Measurement circuit 2)

1) Set V1=V2=V3=3.5V, V4=0V, V_{VMP}=V_{SEL}=VDD, V_{VINI}=V_{CTL}=0V, S1=OFF, enter normal condition.
2) Decrease V_{SEL} from VDD gradually. When DOP pin switches from high to Low, the V_{SEL} is the SEL input voltage "L" (V_{SELL}).
3) Initialize V_{SEL} from 0V and increase gradually. When DOP pin switches from low to high, the V_{SEL} voltage is the SEL input voltage "H" (V_{SELH}).

(9) Over-charge and over-discharge detection delay time (Measurement circuit 3)

1) Set V1=V2=V3=V4=3.5V, V_{VMP}=VDD, V_{VINI}=0V, enter normal condition.
2) Increase V1 from 3.5V to (V_{OV}+0.02V) immediately (within 10us). The over-charge detection delay time (t_{OV}) is the period from the time V1 gets to (V_{OV}+0.02V) till COP pin switches from low to high.
3) Set V1=V2=V3=V4=3.5V, V_{VMP}=VDD, V_{VINI}=0V, enter normal condition.
4) Decrease V1 from 3.5V to (V_{OD}-0.02V) immediately (within 10us). The over-discharge detection delay time (t_{OD}) is the period from the time V1 gets to (V_{OD}-0.02V) till DOP pin switches from low to high.

(10) Discharge over-current and short-circuit detection delay time (Measurement circuit 3)

1) Set V1=V2=V3=V4=3.5V, V_{VMP}=VDD, V_{VINI}=0V, enter normal condition.
2) Increase V_{VINI} from 0V to (V_{DOC1}+10mV) immediately (within 10us). The discharge over-current detection delay time 1 (t_{DOC1}) is the period from the time V_{VINI} gets to (V_{DOC1}+10mV) till COP and DOP pin switches from low to high.
3) Set V1=V2=V3=V4=3.5V, V_{VMP}=VDD, V_{VINI}=0V, enter normal condition.
4) Increase V_{VINI} from 0V to (V_{DOC2}+0.1V) immediately (within 10us). The discharge over-current detection delay time 2 (t_{DOC2}) is the period from the time V_{VINI} gets to (V_{DOC2}+0.1V) till COP and DOP pin switches from low to high.
5) Set V1=V2=V3=V4=3.5V, V_{VMP}=VDD, V_{VINI}=0V, enter normal condition.
6) Decrease V_{VMP} from VDD to (V_{SHORT} -0.2V) immediately (within 10us). The short detection delay time (t_{SHORT}) is the period from the time V_{VMP} gets to (V_{SHORT} -0.2V) till COP and DOP pin switches from low to high.

(11) Internal resistance (Measurement circuit 4)

1) Set V1=V2=V3=V4=3.5V, V_{VMP}=V_{SEL}=VDD, V_{CTL}=0V, COP and DOP pin left "open".
2) Decrease VMP voltage to 0V. VDD/I_{VMD} is the internal resistance between VDD and VMP (R_{VMD}).
3) Set V1=V2=V3=V4=3.5V, V_{VMP}=V_{SEL}=VDD, V_{CTL}=0V, COP and DOP pin left "open".
4) Decrease V1=V2=V3=V4=1.8V. VDD/I_{VMS} is the internal resistance between VSS and VMP (R_{VMS}).
   * Using the current value of the VMP pin.

(12) CTL pin "H", "L" current, SEL pin "H", "L" current (Measurement circuit 4)

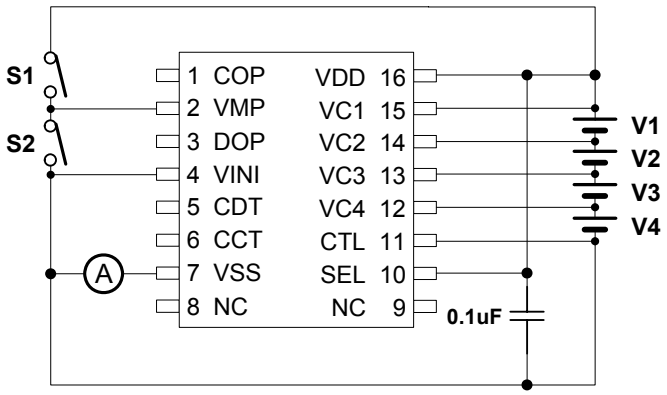
1) Set V1=V2=V3=V4=3.5V, V_{VMP}=V_{SEL}=VDD, V_{CTL}=0V, COP and DOP pin left "open". The current flowing through the CTL pin is the CTL pin current "L" (I_{CTLL}). Then, set V_{CTL}=VDD, the current flowing through the CTL pin is the CTL pin current "H" (I_{CTLH}).
2) Set V1=V2=V3=V4=3.5V, V_{VMP}=V_{SEL}=VDD, V_{CTL}=0V, COP and DOP pin left "open". The current flowing through the SEL pin is the SEL pin current "H" (I_{SELH}). Then, set V_{SEL}=0V, the current flowing through the SEL pin is the SEL pin current "L" (I_{SELL}).

(13) COP pin leakage and sink current, DOP pin source and sink current (Measurement circuit 4)

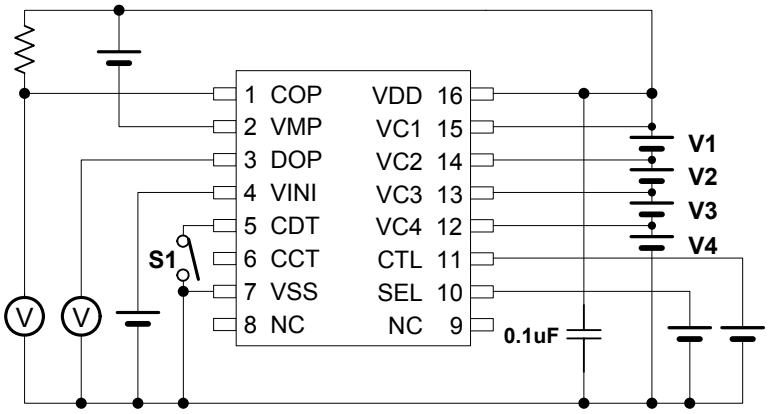
1) Set V1=V2=V3=V4=3.5V, V_{VMP}=V_{SEL}=VDD, V_{CTL}=0V, V_{COP}=0.5V, DOP pin left “open”. The current flowing through the COP pin is the COP pin sink current (I_{COL}).
2) Set V1=V2=V3=V4=6V, V_{VMP}=V_{SEL}=V_{COP}=VDD, V_{CTL}=0V, DOP pin left “open”. The current flowing through the COP pin is the COP pin leakage current (I_{COH}).
3) Set V1=V2=V3=V4=3.5V, V_{VMP}=V_{SEL}=VDD, V_{CTL}=0V, V_{DOP}=0.5V, COP pin left “open”. The current flowing through the DOP pin is the DOP pin sink current (I_{DOL}).
4) Set V1=V2=V3=V4=3.5V, V_{SEL}=VDD, V_{CTL}=0V, V_{VMP}=VDD-2V, V_{DOP}=VDD-0.5V, COP pin left “open”. The current flowing through the DOP pin is the DOP pin source current (I_{DOH}).

(14) 0V charge starting voltage (Measurement circuit 5)

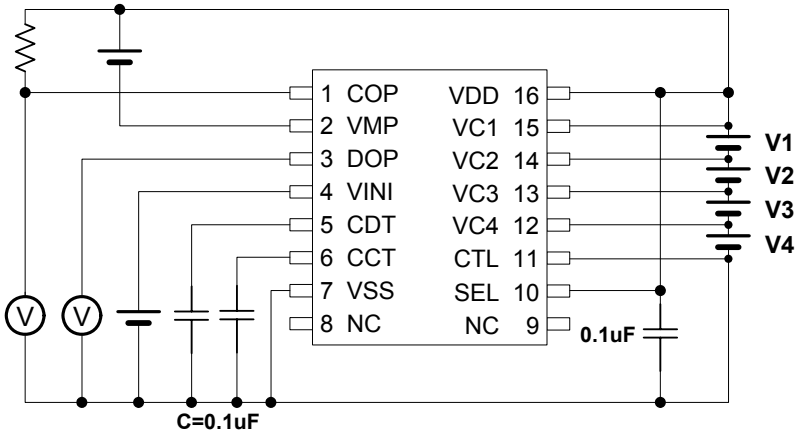
1) Set V1=V2=V3=V4=0V, increase V_{VMP} from 0V gradually. The V_{VMP} voltage is the 0V charge starting voltage (V_{0CHA}) when COP pin voltage is 1V lower than the V_{VMP} voltage.



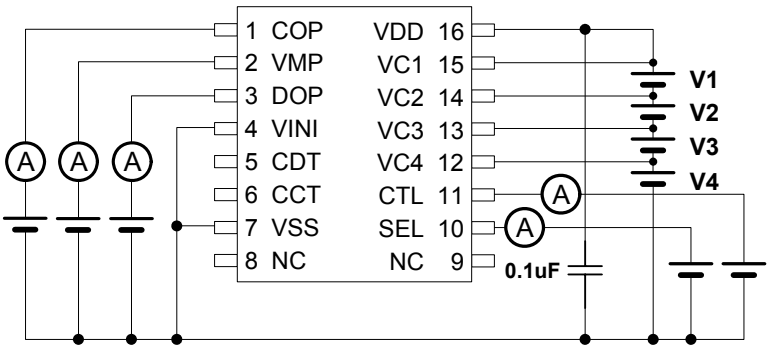
Measurement circuit 1



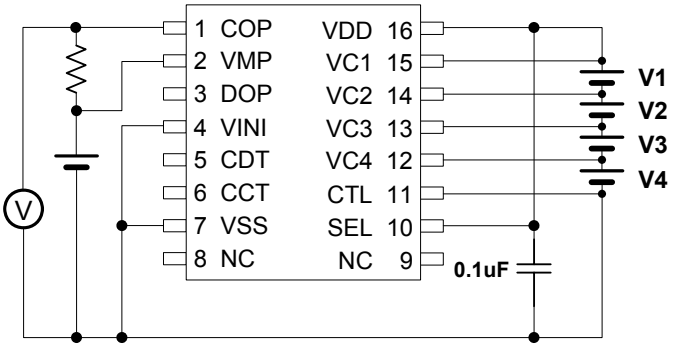
Measurement circuit 2



Measurement circuit 3



Measurement circuit 4



Measurement circuit 5

Operations

The NT1775 provides over-charge, over-discharge, discharge over-current, and short circuit protections for the 3/4-cell battery pack. When the battery pack is in charging stage, the current flow is from EB+ to EB- through the batteries. NT1775 continuously senses all the battery voltage by VC1~VC4 pins if the over-charge occurs. On the other hand, when the battery pack is in discharging stage, the current flow is from EB+ to EB- through the load. NT1775 also senses all battery voltages by VC1~VC4 pins if the over-discharge occurs. As discharging, there is a positive voltage between VSS and EB-, because the current passing through R_{SENSE}. NT1775 detects this positive voltage by VINI pin if the discharge over-current occurs as well. Further, NT1775 also provide a short protection by detecting the voltage drop between VDD and VMP pins.

(1) Over-charge Condition

1) Over-charge Protection

When any of the cells voltage is equal to or higher than the over-charge detection voltage (V_{OV}) for a certain delay time (t_{OV}), NT1775 would turn off the external Pch MOSFET by COP pin to protect the pack from being over-charged. In the meanwhile, COP pin turns to “H” from “L” level.

2) Over-charge Protection Release

The over-charge protection can be released by either of the following conditions,

(a) Removed charger and connect a load (100KΩ typically) when all battery voltages are lower than the detection voltage V_{OV}

(b) All battery voltages are lower than the over-charge release voltages V_{REL1}.

(2) Over-discharge Condition

1) Over-discharge Protection

When any of the cells is lower than the over-discharge detection voltage (V_{OD}) for a certain delay time (t_{OD}), NT1775 would turn off the external Pch MOSFET by DOP pin to protect the pack from being over-discharged.

2) Over-discharge Protection Release

The over-discharge protection can be released by connecting a charger when all battery voltages are equal to or higher than the over-discharge detection voltage (V_{OD}).

(3) Power Down Condition

1) Entering to Power Down Mode

NT1775 enters to the power down mode when over-discharge protection occurs. The VMP pin voltage would be pulled low through the R_{VMS} resister and the internal circuits would be turned off; therefore, the standby current consumption of NT1775 could be reduced to lower than 100nA (Max.).

2) Power Down Mode Release

The power down mode would be released when a charger is connected with the condition that the VMP pin voltage is around VDD/2 or higher.

(4) Discharge Over-current Condition

1) Discharge Over-current Protection

The NT1775 provides 3 levels of discharge over-current protection - discharge over-current 1, discharge over-current 2 and short circuit protection. When any of the discharge over-current conditions happens, the level of DOP and COP pin would become to “H” from “L” to turn off the MOSFET to cut off the discharge path.

a) Discharge over-current 1 protection happens when VINI pin voltage is in the condition of $V_{DOC1} \leqq V_{VINI} < V_{DOC2}$ and lasts for a delay time longer than the specified delay time (t_{DOC1}).

b) Discharge over-current 2 protection starts when VINI pin voltage is higher than V_{DOC2} and for lasts for a delay time longer than the specified delay time (t_{DOC2}).

c) Short-circuit protection occurs when VMP pin voltage is in the condition of $(V_{VMP} - V_{VC1}) \leqq V_{SHORT}$ and for lasts for a delay time longer than the specified delay time (t_{SHORT}).

In the discharge over-current state, the VMP pin voltage would be pulled up to the VDD level by the internal resister (R_{VMD}).

2) Discharge Over-current Protection Release

Any of the discharge over-current/short protections would be released to the normal mode when the load current reduces to the specified current (load resistance > 15MΩ) or the voltage drop between VMP and VC1 pins is higher than V_{SHORT}. For short-circuit protection, NT1775 may be released to normal or power down mode. It’s upon to short-circuit condition. However, it can be awaked from power-down mode as charger is plugged in correctly.

(5) 0V Battery Charge Function

NT1775 provides a 0 V battery charge function which the batteries can be charged when the charger voltage is higher than V_{0CHA}.

(6) Delay Time Setting

The over-charge delay time (t_{OV}) depend on the external capacitor’s capacitance value to the CCT pin. The over-discharge detection delay time (t_{OD}) and the discharge over-current delay time 1 (t_{DOC1}) depend on the external capacitor’s capacitance value to the CDT pin. The other delay times, discharge over-current delay time 2 (t_{DOC2}), and short detection delay time (t_{SHORT}) are internally fixed.

	Min.	Typ.	Max.	
t_{OV} [s]	= (5.00,	10.0,	15.0) x C_{CCT} [μF]	
t_{OD} [s]	= (0.50,	1.0,	1.50) x C_{CDT} [μF]	
t_{DOC1} [s]	= (0.05,	0.1,	0.15) x C_{CDT} [μF]	

Note: The capacitance deviation of the capacitors is not included in the equation above.

(7) CTL pin

NT1775 provides a CTL pin to control the DOP and COP status. This control function takes precedence over all of the protection functions.

Conditions set by CTL pin

CTL Pin	COP Pin	DOP Pin
High	Hi-Z	VDD
Open	Hi-Z	VDD
Low	Normal status*	Normal status*

* The all detection circuits take control of the normal status.

(8) SEL pin

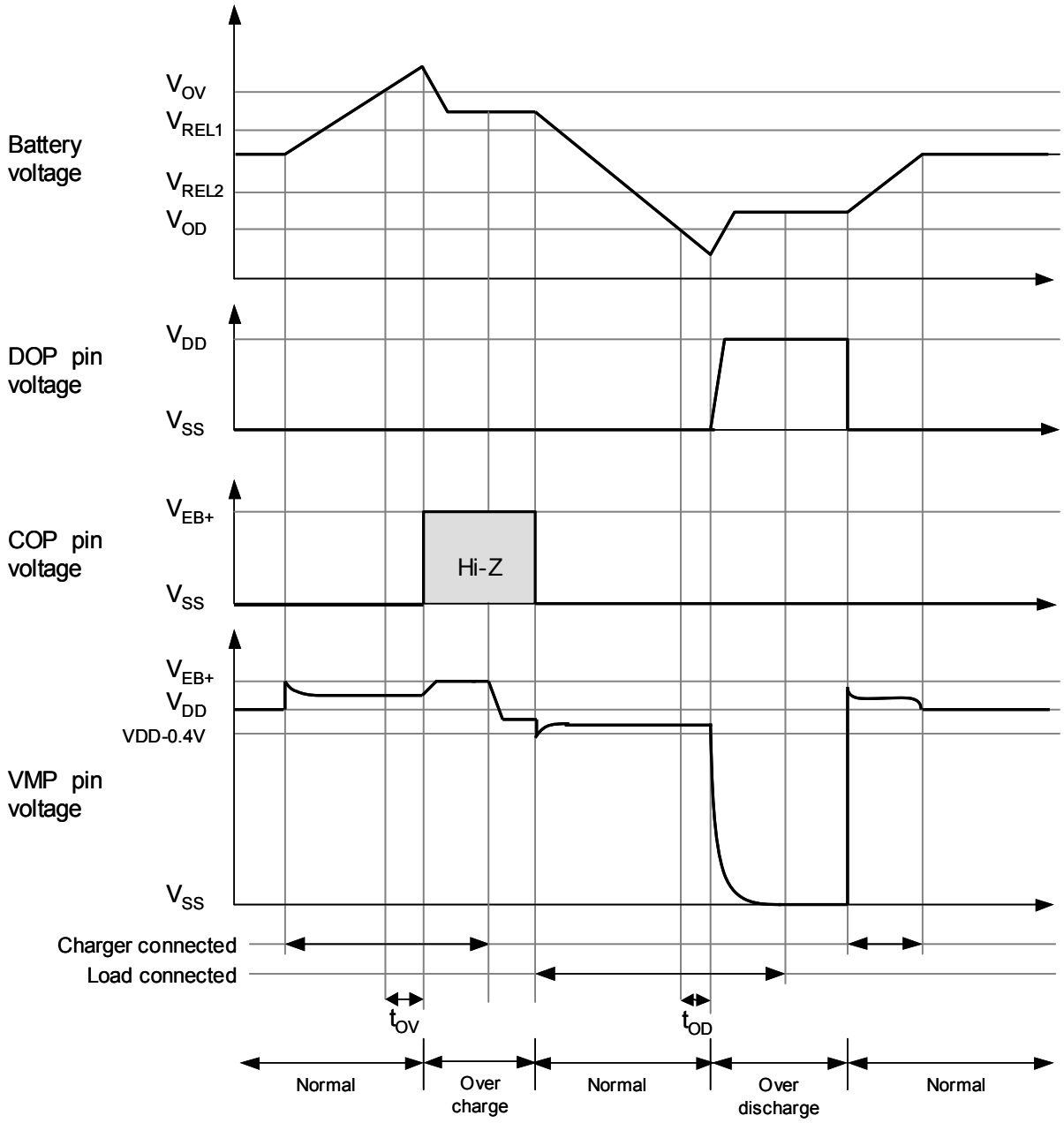
SEL pin is used to switch 4-cell application to the 3-cell. VC4 pin's detection function is prohibited when the SEL pin is connected to the VSS.

Conditions Set by SEL pin

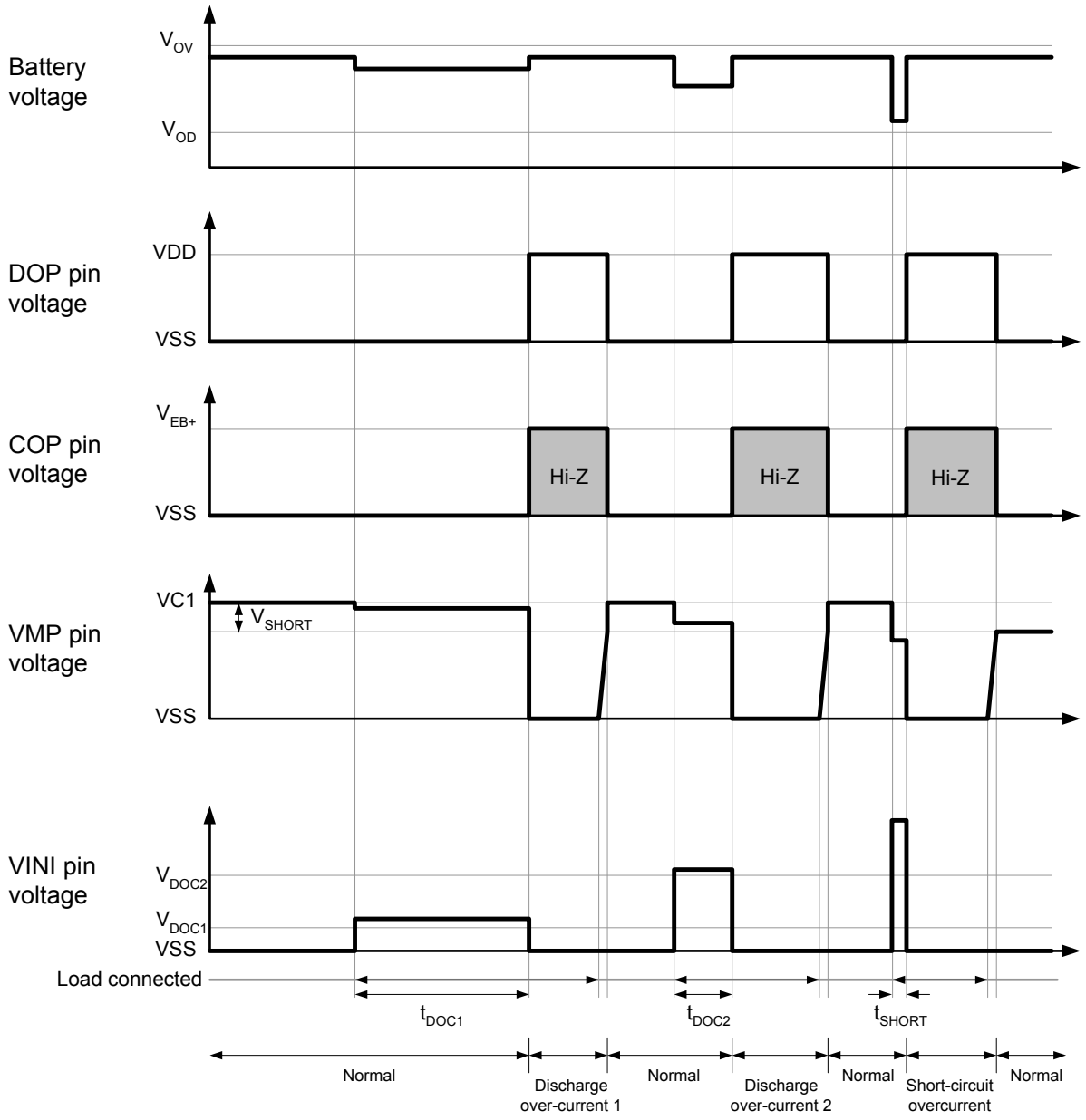
SEL Pin	Condition
High	4-cell protection
Open	Undefined
Low	3-cell protection

Timing Chart

(1) Over-charge Detection, Over-discharge Detection

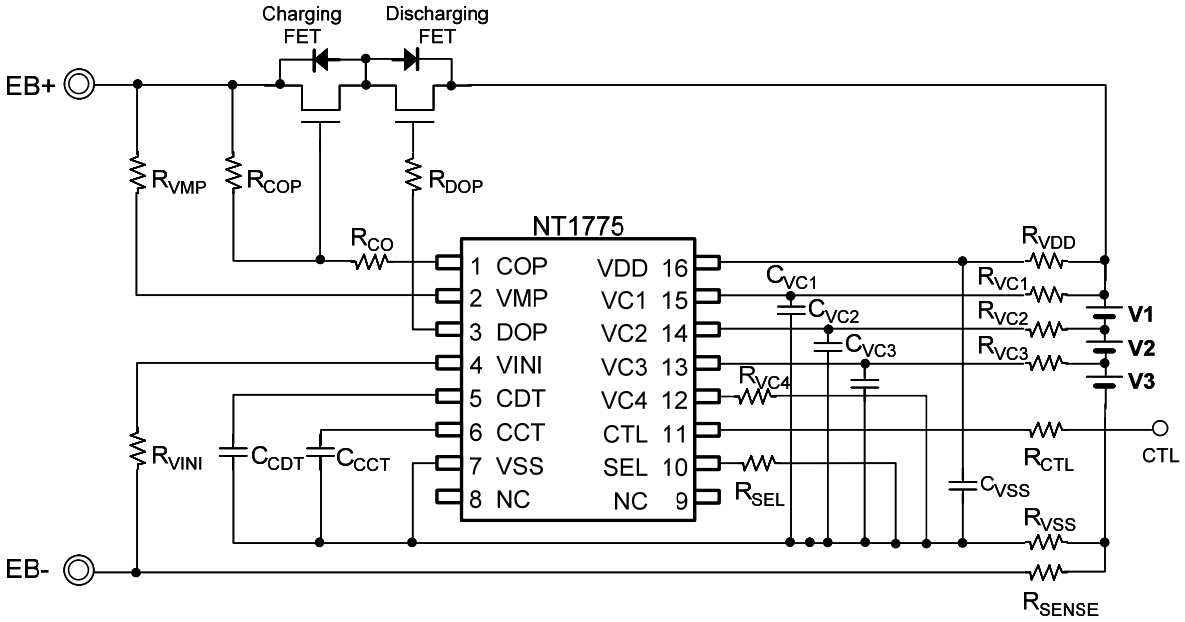


(2) Over-current Detection

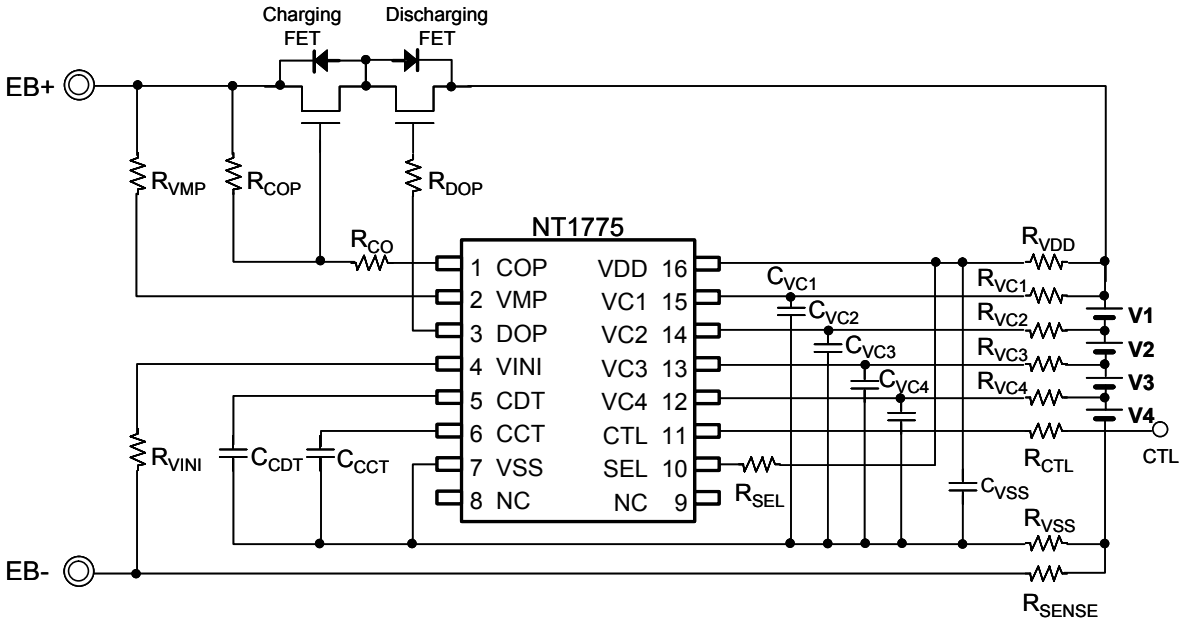


Recommended Application Circuit (Common VSS)

■ For 3-Cell Protection

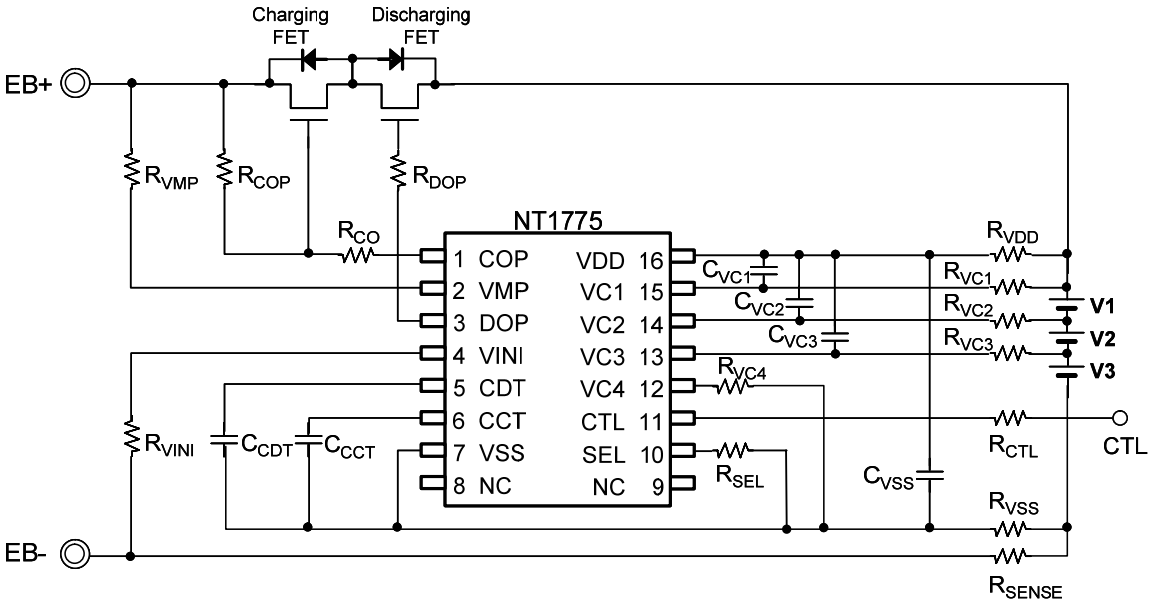


■ For 4-Cell Protection

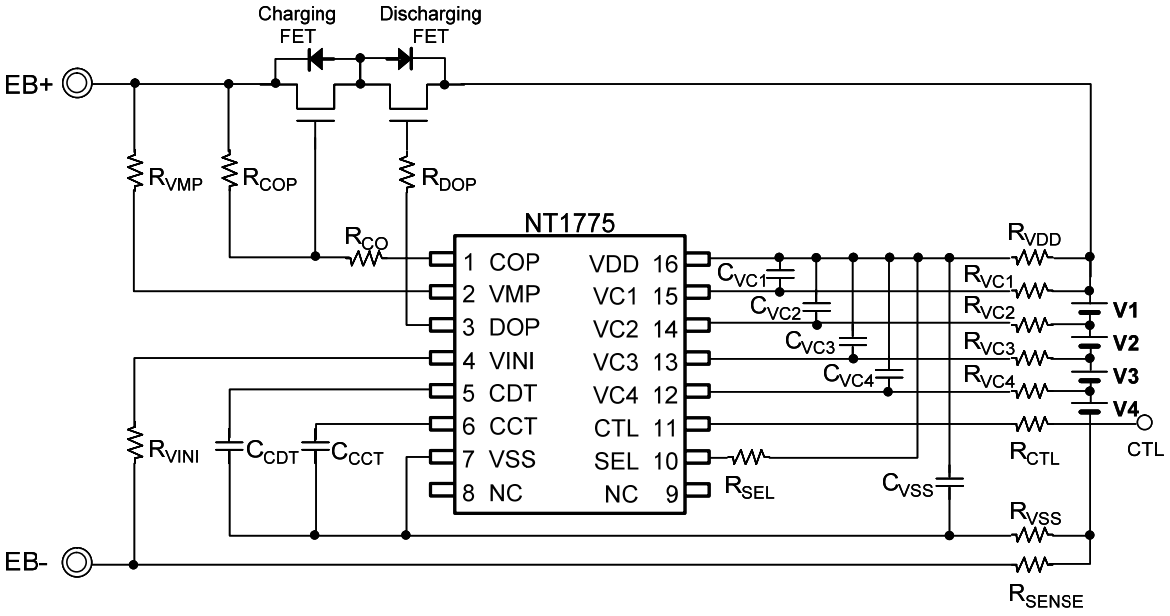


Recommended Application Circuit (Common VDD)

■ For 3-Cell Protection



■ For 4-Cell Protection



Constant for external components (Common VDD/VSS)

Table Constant for external components

Symbol	Parts	Recommended	Min.	Max.
Charging FET	P channel MOSFET	----	----	----
Discharging FET	P channel MOSFET	----	----	----
R_{VDD}	Resistor	**100Ω** *5	51Ω	510Ω
R_{VC1}	Resistor	**100Ω**	100Ω	1KΩ
R_{VC2}	Resistor	**100Ω**	100Ω	1KΩ
R_{VC3}	Resistor	**100Ω**	100Ω	1KΩ
R_{VC4}	Resistor	**100Ω**	100Ω	1KΩ
R_{CO}	Resistor	**5.1KΩ**	500Ω	10KΩ
R_{DOP}	Resistor	**5.1KΩ**	2KΩ	10KΩ
R_{COP}	Resistor	1MΩ	0.1MΩ	1.2MΩ
R_{VMP}	Resistor	**20KΩ**	5.1KΩ	120KΩ
R_{CTL}	Resistor	1KΩ	1KΩ	100KΩ
R_{VINI}	Resistor	1KΩ	1KΩ	100KΩ
R_{SEL}	Resistor	1KΩ	1KΩ	100KΩ
R_{SENSE}	Resistor	----	----	----
R_{VSS}	Resistor	**0Ω** *5	**----**	**----**
C_{VC1}	Capacitor	**0.1μF**	0.01μF	0.1μF
C_{VC2}	Capacitor	**0.1μF**	0.01μF	0.1μF
C_{VC3}	Capacitor	**0.1μF**	0.01μF	0.1μF
C_{VC4}	Capacitor	**0.1μF**	0.01μF	0.1μF
C_{CCT}	Capacitor	0.1μF	----	----
C_{CDT}	Capacitor	0.1μF	----	----
C_{VSS}	Capacitor	**2.2μF**	2.2μF	10μF

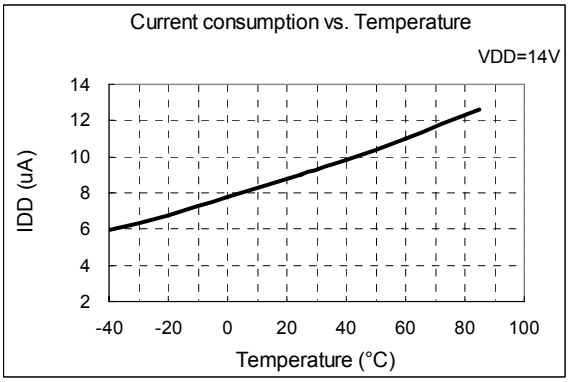
Note:

1) If the threshold voltage of an FET is lower than 0.4V, the FET may not stop the charging current.
   If the charger voltage is higher than the withstanding voltage between the gate and source, the FET may be damaged.
2) **For good noise immunity, C_{VC1}, C_{VC2}, C_{VC3}, C_{VC4} should be connected to ground.**
3) **For short-circuit protection, the R_{CO} should be placed for current limit.**
4) Using an over-spec R_{VC1}, R_{VC2}, R_{VC3}, R_{VC4}, may result in over-charge detection voltage and release voltage higher than the expectation.
   If R_{VC1} has a high resistance, the voltage between VDD and VSS may be higher than absolute maximum rating when a charger is connected reversely since the current flows from the charger to IC.
5) **The recommended values are 100Ω and 0Ω for R_{VDD} and R_{VSS}, respectively.**

Caution: The application circuit above is for reference only. To determine the correct constants, evaluation of actual application is required.

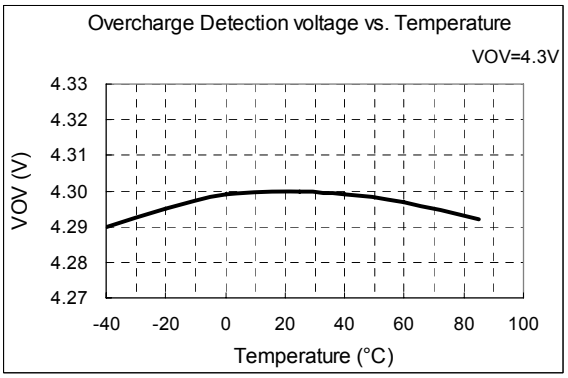
Characteristics (Typical Data)

1. Current consumption

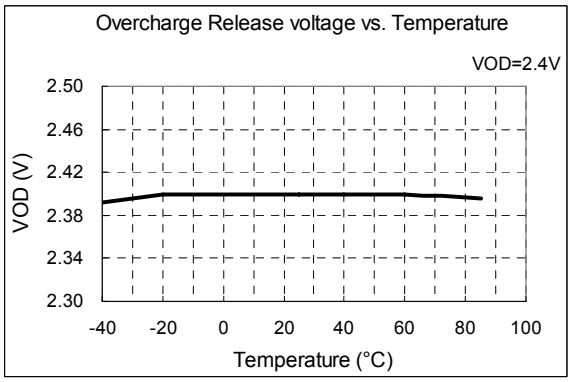


2. Detection Voltage

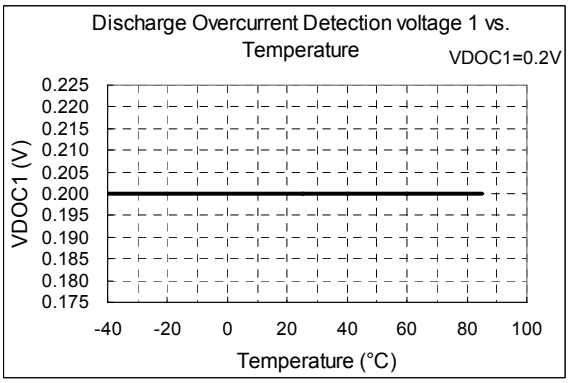
2.1 V_{OV} vs. Ta



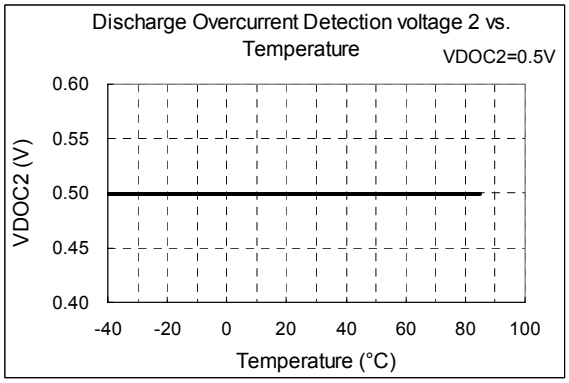
2.2 V_{OD} vs. Ta



2.3 V_{DOC1} vs. Ta

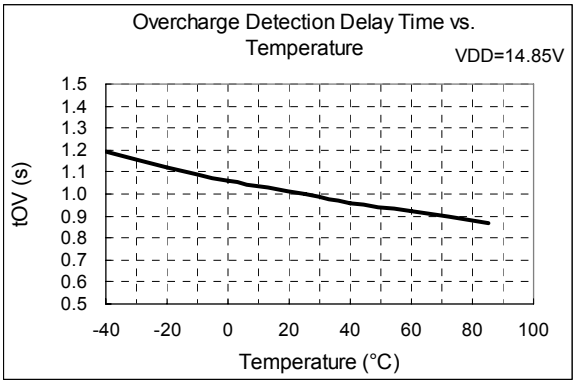


2.2 V_{DOC2} vs. Ta

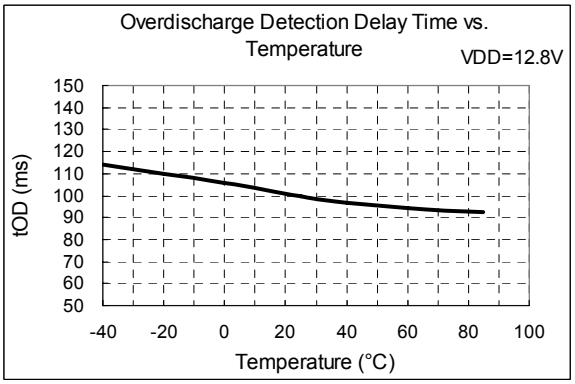


3. Detection Delay Time

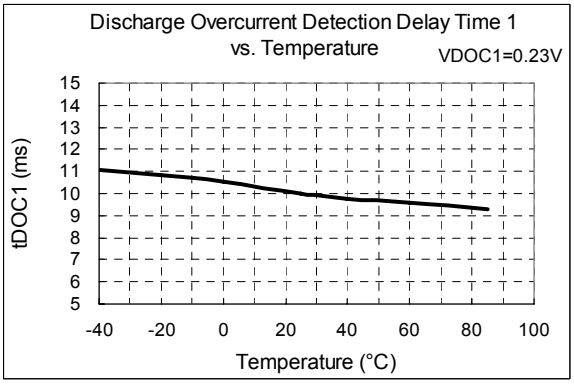
3.1 t_{OV} vs. Ta



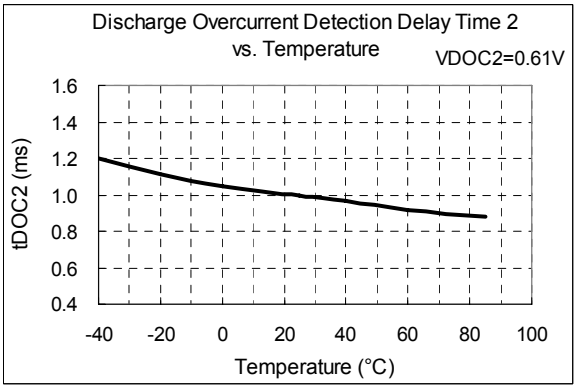
3.2 t_{OD} vs. Ta



3.3 t_{DOC1} vs. Ta

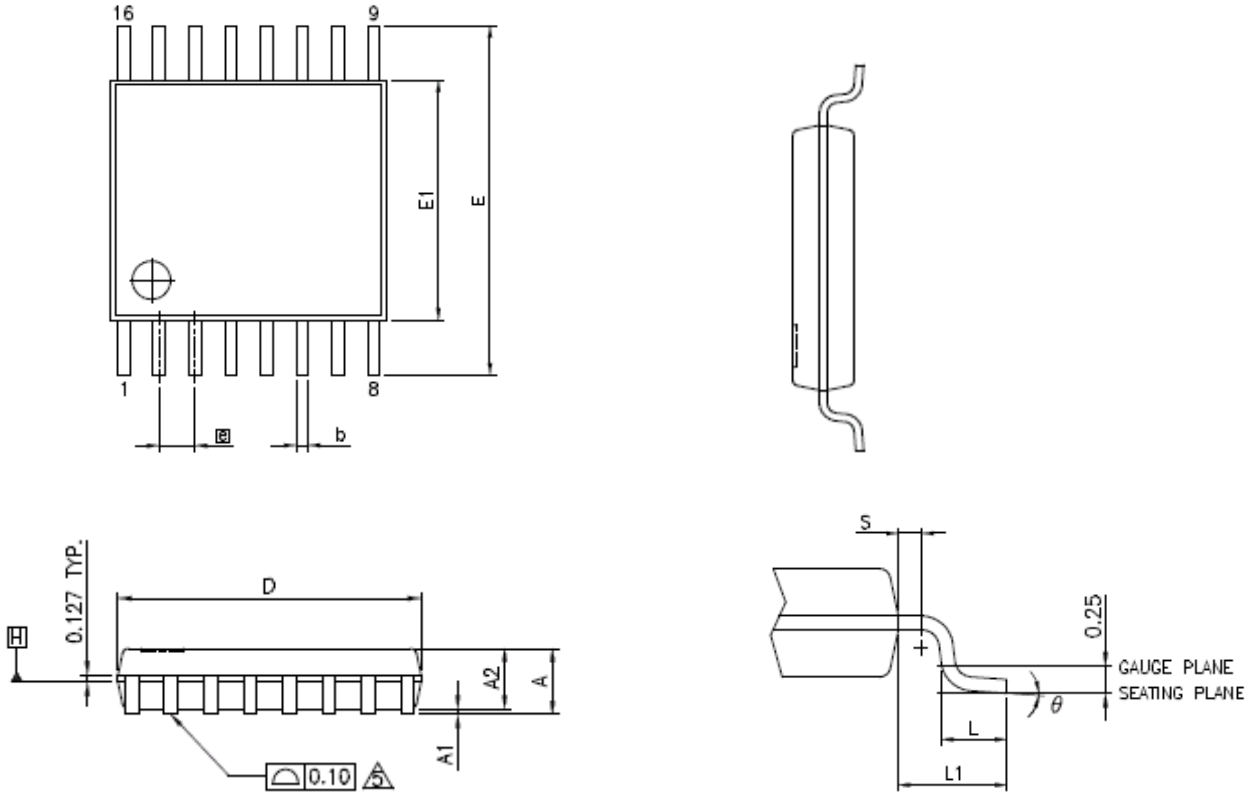


3.2 t_{DOC2} vs. Ta



Package Information

TSSOP-16L Dimension

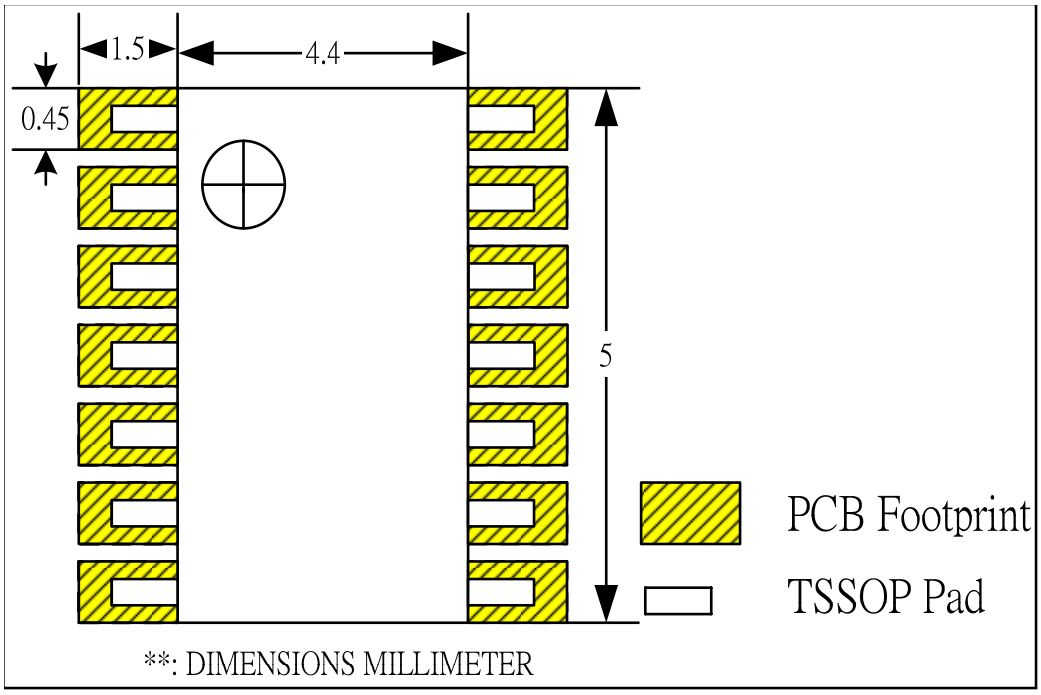


SYMBOLS	DIMENSIONS MILLIMETER		
	MIN.	NOM.	MAX.
A	—	—	1.2
A1	0.00	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 BSC		
L	0.45	0.60	0.75
S	0.20	—	—
θ	0°	—	8°

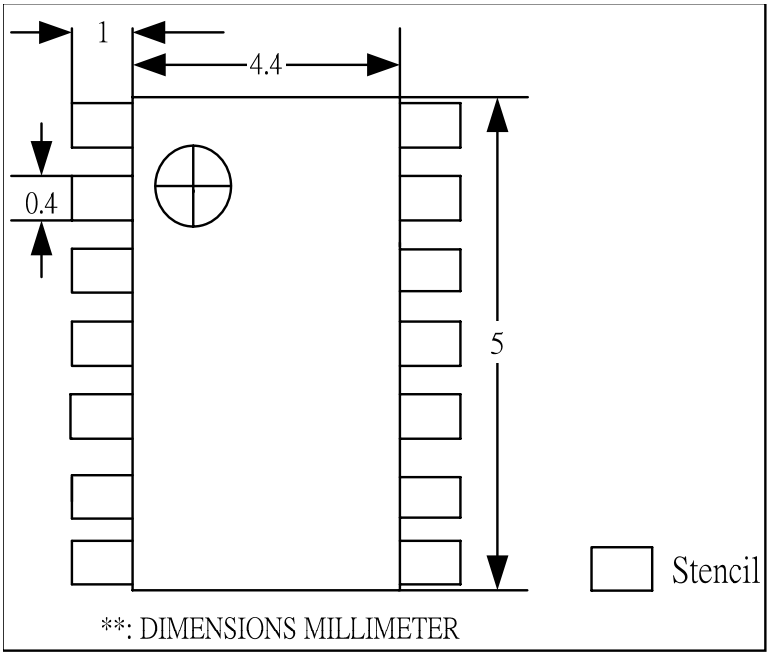
NOTES:
1. JEDEC OUTLINE :
   STANDARD : M0-153 ABT REV.F
   THERMALLY ENHANCED : M0-153 ABT REV.F
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FALSH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION 'b' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H.

Land Pattern Recommendation

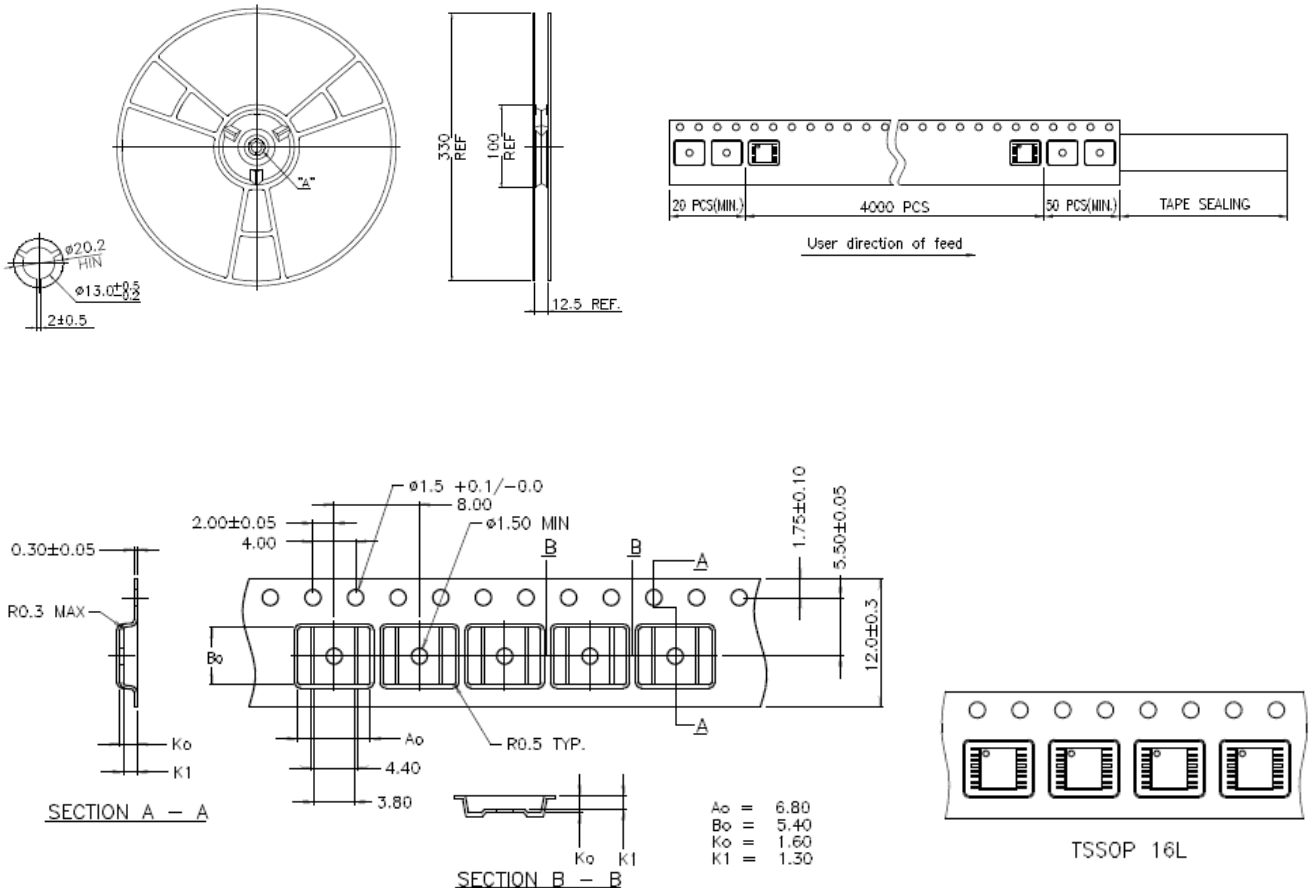
TSSOP-16L



Stencil Guideline



Tape and Reel Information



Notes:

1. 10 sprocket holes pitch cumulative tolerance ± 0.2mm.
2. Camber not to exceed 1mm in 100mm.
3. Material: Anti-Static Black Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket.
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Layout Guideline for PCB

1. For 4-layer PCB, the inter-layers are employed as VDD and VSS planes in general. So no matter for common-VDD or –VSS connection, the input filter capacitors can effectively screened out the noise to grand VDD or VSS planes.
2. For 2-layer PCB, input capacitors are supposed to be tied to noise-less plane or node. It's strongly recommended to keep VSS as a bulky and complete route as possible for common-VSS connection. Vice versa, a bulky and complete VDD plane or node is better for common-VDD connection. The bulk capacitor between VDD and VSS should be close beside IC.
3. Zener diodes are recommended for charging and discharging MOSFET to clamp the spike. An extra zener series-connected with resistor can help ESD and spike clamp for VDD pin.