

MegaChips Corporation

Product Specification

SPS-MA60000-EN

TITLE

frizz ES1 Product Specification

Product Number	MA60000
Product Name	frizz
Customer Name	general-purpose

Sub Group	Revision	Final Approved		
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Standard

frizz ES1 Product Specification

No.

SPS-MA60000-EN

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1. Overview

This specification is applied to frizz ES1.

frizz is DSP consisting of high-performance 32bit core processor and peripheral that are suitable for PDR (Pedestrian Dead reckoning) processing.

2. Specification

Table 2-1 frizz specifications

	Item	Spec	Notes
Power	Core	+1.2V +/-10%	
	IO	+1.8V +/-10% +2.5V +/-10% +2.8V +/-10% +3.0V +/-10% +3.3V +/-10%	
Package	Package shape	FBGA	
	Package size	3.5 x 3.5mm	
	Ball number	49	
	Ball pitch	0.4mm	
	Thickness	0.65mm	Max
System	Data RAM	256kbyte	
	Instruction RAM	256kbyte	
	Clock input method	External x1 Internal x2	
	External clock frequency	40MHz	Typ
	Internal clock frequency	• Slow:100kHz • Fast :40MHz	
	Clock setting	- selected external or internal by SELCLK pin - selected internal frequency(slow or fast) by register	
	DSP	paraForce (Xtensa LX4)	• 3way VLIW • Floating Point 4way SIMD
External interrupt	2ch	Alternative GPIO	
Host interface	SPI (Slave)	Alternative	
	I2C (Slave)		
Sensor interface	SPI (Master)	1ch(4 chip select)	Chip selects are alternaive GPIO
	I2C (Master)	1ch	
General interface	UART	1ch	
	GPIO	4ch	
	PWM	2ch(resolution:2^16)	Alternative GPIO
Others	Ambient Operating Temp.	-20-85 degrees C	

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3. Block Diagram

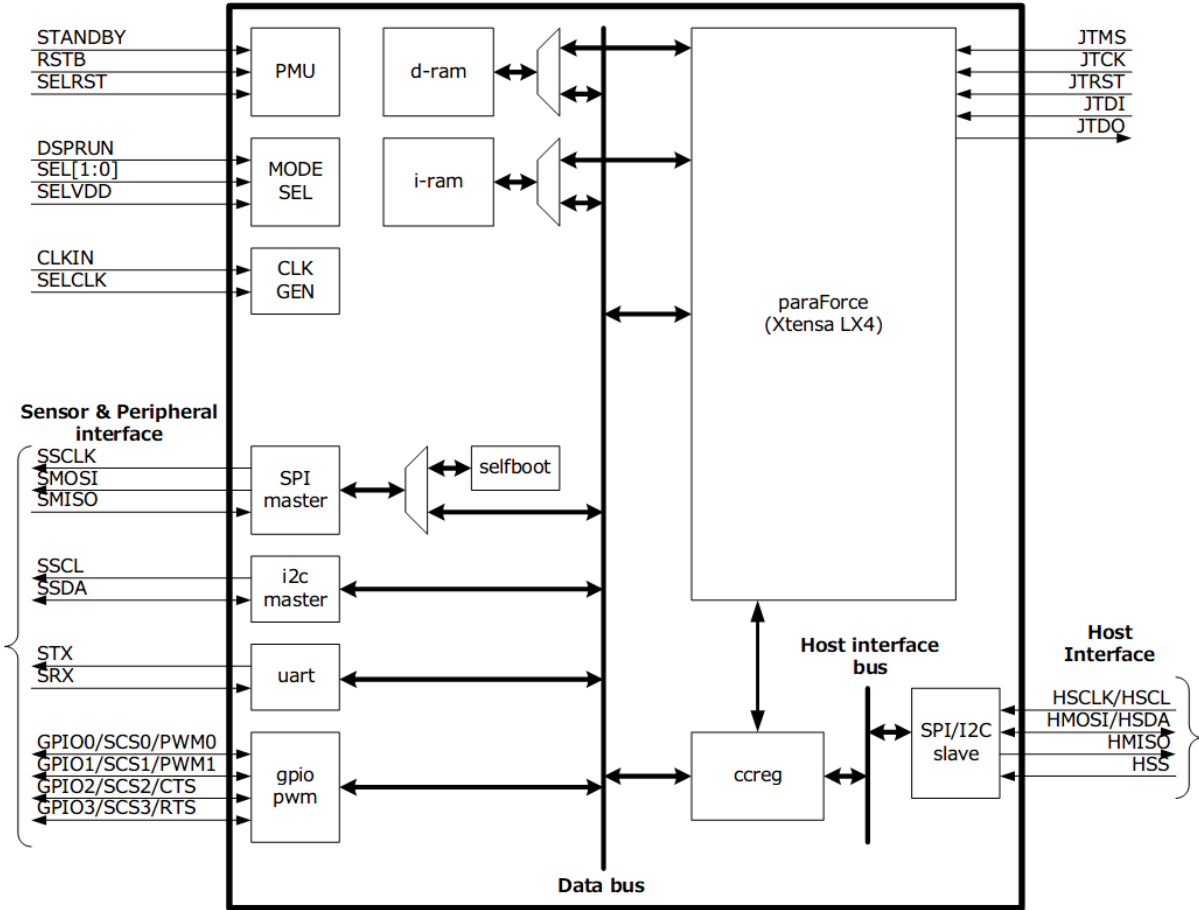


Figure 3-1 frizz block diagram

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4. External Terminal Specifications

Table 4-1 List of pinout

No	Area	Ball Name	Signal Name	Dir	Alt0 (Default)		Alt1		Alt2		Pin state@Reset	Power
					Function	Dir	Function	Dir	Function	Dir		
1	System	STANDBY	STANDBY	I	Standby mode set (0:Standby mode 1:Normal)	-	-	-	-	I	(Hi-Z)	1.8~ 3.3V
2		DSPRUN	DSPRUN	I	DSP Run mode set(0:Run 1:Stall)	-	-	-	-	I	(Hi-Z)	
3		CLKIN	CLKIN	I	External Clock Input	-	-	-	-	I	(Hi-Z)	
4		SELO	SELO	I	Mode setting 0	-	-	-	-	I	(Hi-Z)	
5		SEL1	SEL1	I	Mode setting 1	-	-	-	-	I	(Hi-Z)	
6		SELCLK	SELCLK	I	Ext/Int Clock switch (0: internal, 1: external)	-	-	-	-	I	(Hi-Z)	
7		SELVDD	SELVDD	I	IO voltage select (0V : IO voltage=3.3V 1.8V : IO voltage=1.8V)	-	-	-	-	I	(Hi-Z)	
8		RSTB	RSTB	I	External Reset (0:Reset 1:Normal)	-	-	-	-	I	Pull-up	
9		SELRST	SELRST	I	Reset Signal Select (0:POR 1:External Reset)	-	-	-	-	I	Pull-down	
10	Host IF	HSCLK	HSCLK/HSCL	I	Host IF SPI Clock Input	I	Host IF I2C SCL Input	-	-	I	(Hi-Z)	
11		HMOSI	HMOSI/HSDA	I	Host IF SPI Data Input	I/O	Host IF I2C SDA signal	-	-	I	(Hi-Z)	
12		HMISO	HMISO	O	Host IF SPI Data Output	-	-	-	-	I	(Hi-Z)	
13	Sensor IF	HSS	HSS	I	Host IF SPI Chip Select Input	-	-	-	-	I	(Hi-Z)	
14		SSCLK	SSCLK	O	Sensor IF SPI Clock Output	-	-	-	-	O	(Hi-Z)	
15		SMOSI	SMOSI	O	Sensor IF SPI Data Output	-	-	-	-	O	(Hi-Z)	
16		SMISO	SMISO	I	Sensor IF SPI Data Input	-	-	-	-	I	(Hi-Z)	
17		SSCL	SSCL	O	Sensor IF I2C SCL Output	-	-	-	-	I	(Hi-Z)	
18		SSDA	SSDA	I/O	Sensor IF I2C SDA Signal	-	-	-	-	I	(Hi-Z)	
19	UART	STX	STX	O	UART Data Output	-	-	-	-	O	(Hi-Z)	
20		SRX	SRX	I	UART Data Input	-	-	-	-	I	(Hi-Z)	
21	GPIO/PWM	GPIO0	GPIO0/SCS0/PWM0	I/O	GPIO0(SelfBoot CS)	O	Sensor IF SPI Chip Select Output 0	O	PWM0	I	(Hi-Z)	
22		GPIO1	GPIO1/SCS1/PWM1	I/O	GPIO1	O	Sensor IF SPI Chip Select Output 1	O	PWM1	I	(Hi-Z)	
23		GPIO2	GPIO2/SCS2/C TS	I/O	GPIO2(Ext INT Input. Level Only)	O	Sensor IF SPI Chip Select Output 2	I	UART Master Transmission ACK	I	(Hi-Z)	
24		GPIO3	GPIO3/SCS3/R TS	I/O	GPIO3(Ext INT Input. Level Only)	O	Sensor IF SPI Chip Select Output 3	O	UART Master Transmission Request	I	(Hi-Z)	
25	JTAG	JTMS	JTMS	I	JTAG TMS	-	-	-	-	I	Pull-up	
26		JTCK	JTCK	I	JTAG TCK	-	-	-	-	I	Pull-down	
27		JTRST	JTRST	I	JTAG RST	-	-	-	-	I	Pull-up	
28		JTDI	JTDI	I	JTAG Data Input	-	-	-	-	I	Pull-up	
29		JTDO	JTDO	O	JTAG Data Output	-	-	-	-	O	Pull-up	

5. System Specifications and settings

5.1. Mode Settings

The device carries out operation mode settings by SEL[1:0] pins. Self-boot performs a boot process from external serial flash ROM. Host download boot is from host device connected to host interface. Please refer to Table 5-1 for details.

Table 5-1 Setting of boot mode and host interface mode

Ball/Pad		Boot Modes
SELO	SEL1	
L	L	Host download boot SPI Mode0
L	H	Host download boot SPI Mode3
H	L	Host download boot I2C
H	H	Self-Boot

5.2. Low Power Modes

The device support low power modes in order to reduce power consumption when paraForce stop operating. Please refer to 5.7 Low Power Modes for details.

5.3. paraForce Initial Settings

DSPRUN pin can set paraForce initial settings after reset release. Generally, DSPRUN pin is set to "L" (Run). When debugging by JTAG, DSPRUN pin is set to "H" (Stall).

5.4. I/O Power Settings

The device I/O power can be selected 1.8V I/O or 3.3V I/O by SELVDD pin. I/O power settings can apply only one voltage, either 1.8V or 3.3V. When the device's I/O power is used 1.8V, SELVDD pin is applied 1.8V, and when it used 3.3V, SELVDD pin is applied 0V.

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5.5. Reset Specifications

frizz has function (POR : Power On Reset) to internally generate reset signal. Therefore, the external reset forming circuit is unnecessary when you use POR.

5.5.1 POR (Power On Reset)

POR output waveform and characteristics is below Figure 5-1 and Table 5-2.

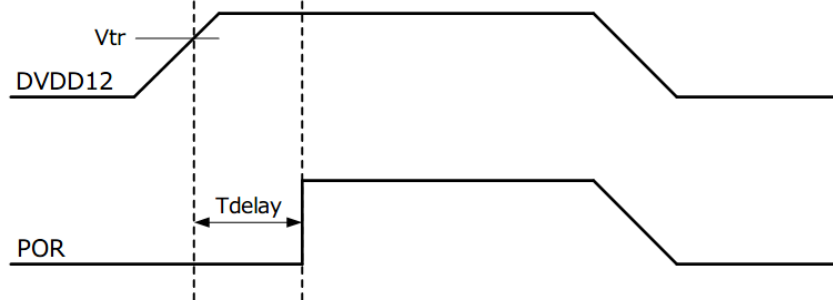


Figure 5-1 POR output waveform

Table 5-2 POR Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Condition
Reset Trigger Level	Vtr	0.4	0.6	1.0	V	1V/1s power up ratio
Reset Delay Time	Tdelay	20	40	1000	us	1V/1us power up ratio

- POR output: "L" is reset on, "H" is reset off.
- POR is available when DVDD12 ramp-up time is from 1V/us to 1V/s.
- If DVDD12 sets 1.2V -> 0V -> 1.2V, DVDD12 as 0V period has to keep over 200ms as below Figure 5-2.

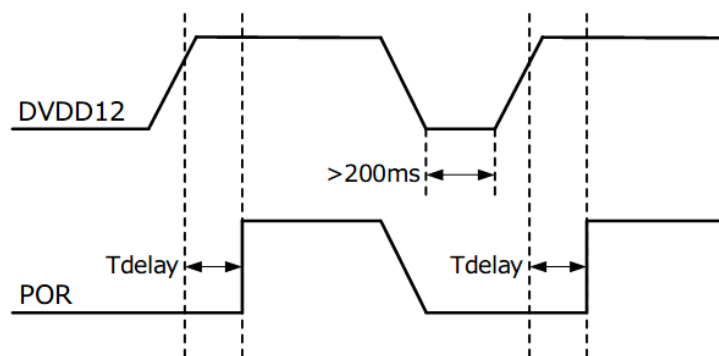


Figure 5-2 POR output waveform when DVDD12 sets OFF to ON

5.5.2 External Reset Input

It is possible to input the external reset input signal, and use for frizz reset control. When the external reset input, SELRST pin is set "H", and reset control signal inputs RSTB pin. In this case, RSTB pin logic is that "L" is reset on and "H" is reset off, in the same specification of POR.

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5.6. System Clock

The device has 3 clock sources. System clock can be selected by them. 3 clock sources specification is as below.

- External input clock (The clock which input at CLKIN pin)
- Internal slow clock (ROSC1 100kHz)
- Internal fast clock (ROSC2 40MHz)

Clock tree is below Figure 5-3.

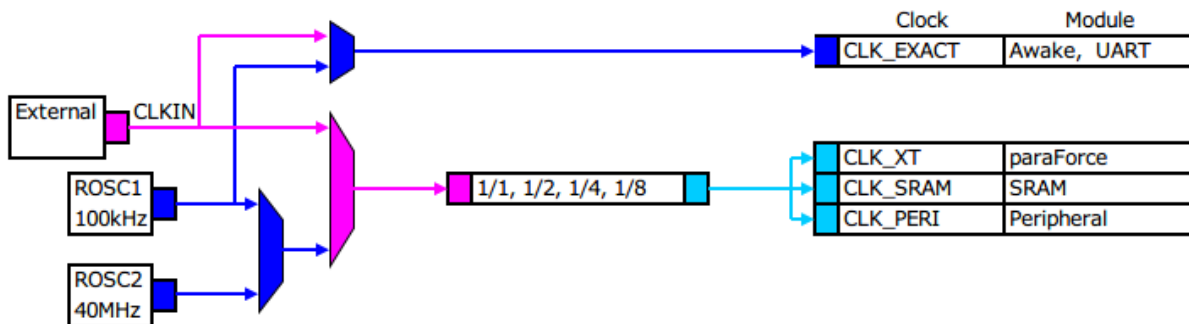


Figure 5-3 Clock tree

5.6.1 External Input Clock

This clock frequency is 40MHz (typ).

5.6.2 Internal Slow Clock (ROSC1)

ROSC1 Electrical Characteristics is below Table 5-3.

Table 5-3 ROSC1 Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Condition
Output frequency	F_{osc}	65	100	135	kHz	
Duty cycle	D	40	50	60	%	
Startup time when power on	T_{on1}		200		us	

ROSC1, 2 Startup waveform is below Figure 5-4. ROSC1 output is unstable during T_{on1} period, and this unstable oscillation is blocked to system clock source.

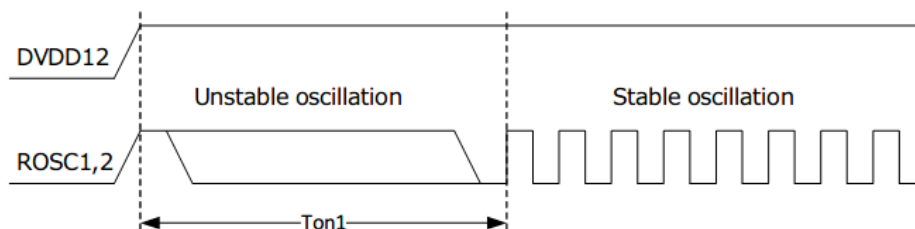


Figure 5-4 ROSC1, 2 Startup waveform

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5.6.3 Internal Fast Clock (ROSC2)

ROSC2 Electrical Characteristics is below Table 5-4. PD (Power Down) can be controlled by xmode1[11] register.

Table 5-4 ROSC2 Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit	Condition
Output frequency	F_{osc}	26	40	54	MHz	
Duty cycle	D	40	50	60	%	
Startup time when power on	T_{on1}		20		us	
Startup time when "PD" enabled	T_{on2}		20		us	

About T_{on1} and T_{on2} , please refer to Table 5-3 and Table 5-4. The unstable output at T_{on2} isn't blocked, and when PD is changed from 1 to 0, please wait for T_{on2} to start operation.

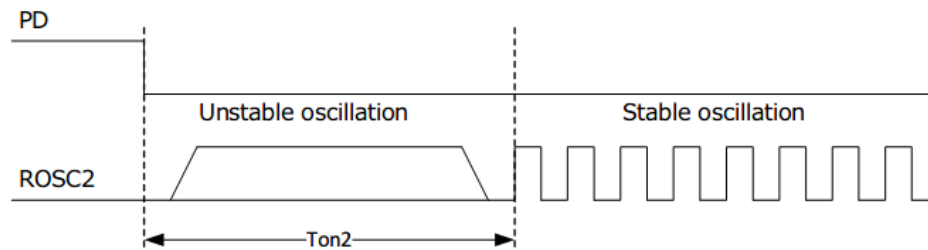


Figure 5-5 ROSC2 Startup Waveform (T_{on2})

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5.7. Low Power Modes

The device support three low power modes as below.

- Sleep mode

In sleep mode, only the paraForce is stopped. All clocks are running. When system clock is set internal low-speed (100kHz) during sleep mode, its mode is slow-CLK sleep mode. And when system clock is set internal high-speed (40MHz) or external clock input during sleep mode, its mode is fast-CLK sleep mode. In fast-CLK sleep mode, host device can access to frizz internal RAM and register. All peripherals continue to operate and can wake up the paraForce when an interrupt occurs.

- Stop mode

In stop mode, the paraForce is stopped and all clocks except the paraForce clock are stopped. It need to setting to register before the paraForece is stopped and can wake up the paraForce when an Awake interrupt occurs.

- Standby mode

The Standby mode is used to achieve the lowest power consumption. The internal power switch is off so that the 1.2V domain is powered off. All clocks is stopped except the internal low speed clock (100kHz). The device enters the Standby mode when external STANDBY pin is set to L, and exits it when external STANDBY pin is set to H. All SRAM and register is initialized when the device exits the Standby mode. Please refer to Table 5-5.

Table 5-5 Low power modes specifications¹

Low Power Mode		Sleep		Stop	Standby
		Fast-CLK	Slow-CLK		
Entry	Start	WAITI instruction	<-	STOPREG 1'b1 set and WAITI instruction	STANDBY pin H->L
Wake up	Start	All interrupt events	<-	The Awake timer interrupt	STANDBY pin L->H
	recovery time	<10us	<2ms	50us-2ms	(depend on boot program size)
Power consumption		<2mA	<100uA	<100uA	<10uA

¹ The recovery time and power consumption value is estimated by simulation, and there is no guarantee.

6. Host Interface Specifications

This is the interface to connect with Host Device and has two kinds of interfaces, SPI slave and I2C slave. The details of Host Interface are as follows.

6.1. Address Map

Figure 6-1 shows Address Map of Host Interface. SPI is accessible to address width of [13:0] area, and I2C is accessible to address width of [7:0] area.

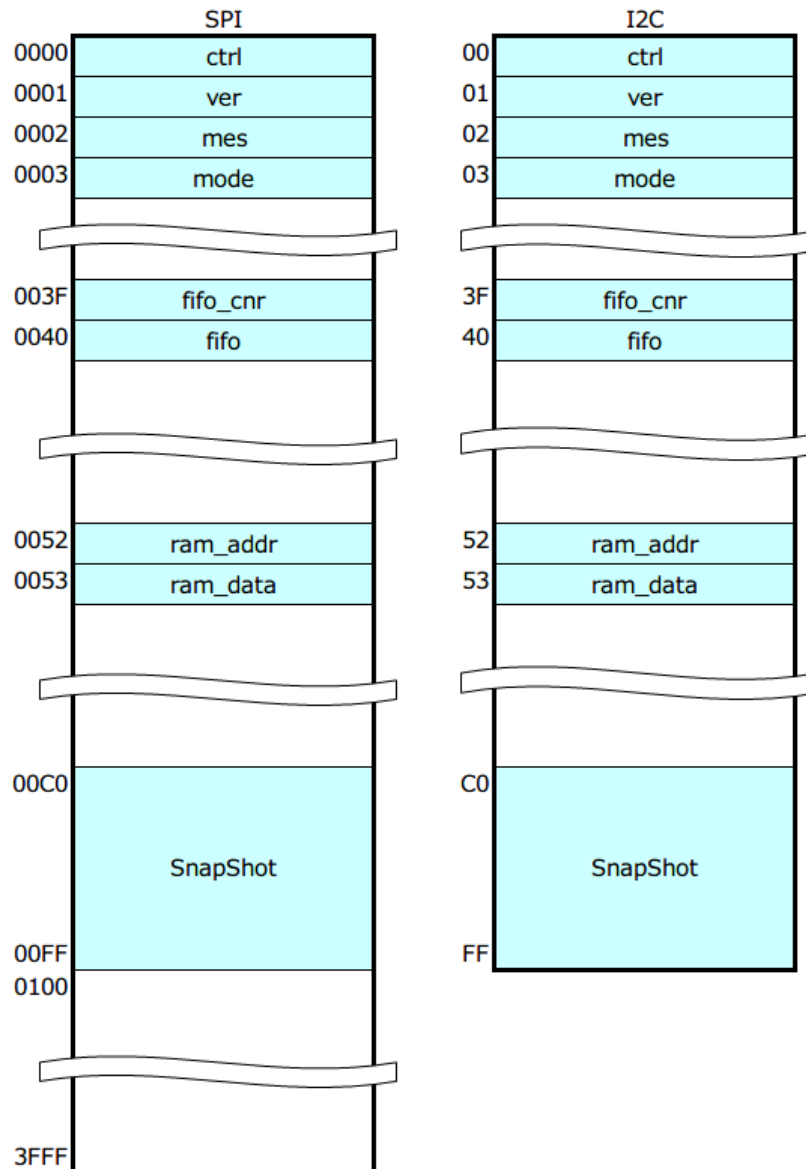


Figure 6-1 Address Map of Host Interface

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6.2. SPI/I2C

SPI (Serial Peripheral Interface) interface which multiplexed I2C is available. They are alternate function and can be operated in slave mode. The external pin SEL0 and SEL1 is selected SPI or I2C interface.

Figure 6-2 shows Host interface SPI timing diagram.

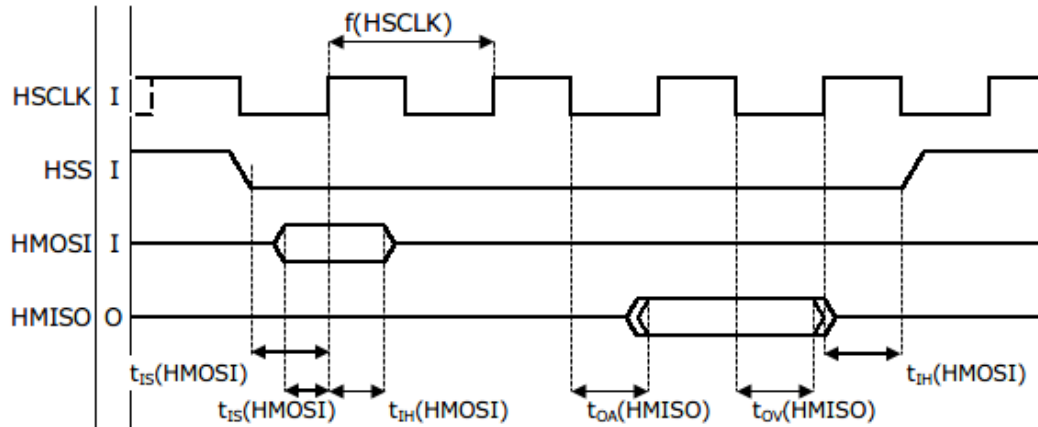


Figure 6-2 Host interface SPI timing diagram

Table 6-1 shows Host interface SPI dynamic characteristics.

Table 6-1 Host interface SPI dynamic characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
IO voltage 3.3V						
SPI Clock Frequency	f (HSCLK)		-	-	40	MHz
Data input setup Time	$t_{IS}(HMOSI)$		4	-	-	ns
	$t_{IS}(HSS)$		6	-	-	ns
Data input hold Time	$t_{IH}(HMOSI)$		1	-	-	ns
	$t_{IH}(HSS)$		1	-	-	ns
Data output Access time	$t_{OA}(HMISO)$	35pF load	-	-	9.5	ns
		20pF load	-	-	8.8	ns
		10pF load	-	-	8.2	ns
Data output Valid time	$t_{OV}(HMISO)$		1	-	-	ns
IO voltage 1.8V						
SPI Clock Frequency	f (HSCLK)		-	-	20	MHz
Data input setup Time	$t_{IS}(HMOSI)$		4	-	-	ns
	$t_{IS}(HSS)$		6	-	-	ns
Data input hold Time	$t_{IH}(HMOSI)$		1	-	-	ns
	$t_{IH}(HSS)$		1	-	-	ns
Data output Access time	$t_{OA}(HMISO)$	20pF load	-	-	14.0	ns
		10pF load	-	-	13.0	ns
Data output Valid time	$t_{OV}(HMISO)$		1	-	-	ns

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Figure 6-3 shows I2C waveform.

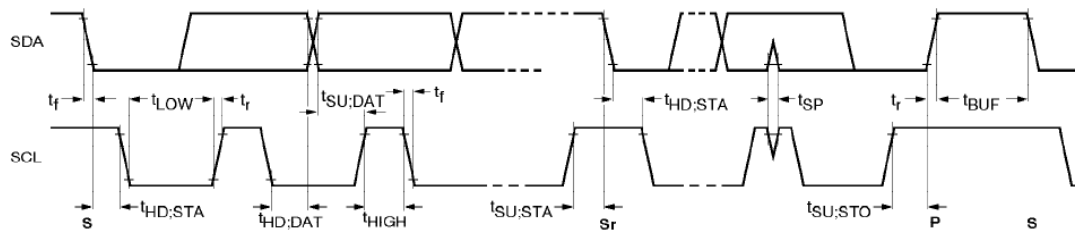


Figure 6-3 I2C waveform

Table 6-2 shows I2C Characteristics.

Table 6-2 I2C Characteristics

Symbol	Parameter	Condition	Standard-mode		Fast-mode		Fast-mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	0	1000	kHz
$t_{HD:STA}$	hold time (repeated) START condition	After this period, the first clock pulse is generated.	4.0	-	0.6	-	0.26	-	us
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	us
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	us
$t_{SU:STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	us
$t_{HD:DAT}$	data hold time		0	-	0	-	0	-	us
$t_{SU:DAT}$	data set-up time		250	-	100	-	50	-	ns
t_r	rise time of both SDA and SCL signals		-	1000	20	300	-	120	ns
t_f	fall time of both SDA and SCL signals		-	300	20* (VDD/ 5.5V)	300	20* (VDD/ 5.5V)	120	ns
$t_{SU:STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	us
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	us
$t_{VD:DAT}$	data valid time		-	3.45	-	0.9	-	0.45	us
$t_{VD:ACK}$	data valid acknowledge time		-	3.45	-	0.9	-	0.45	us

6.3. Access to DPBUF(Dual Purpose Buffer)

The data exchange between paraForce and Host Interface takes place via DPBUF (Dual Purpose Buffer). There are 2 operation modes, FIFO and Snapshot. The mode switching between FIFO and Snapshot is performed in register `fifo_ctr[1]`. Before switching mode, FIFO reset (register `ctrl[3]`) must be performed.

6.3.1 FIFO Mode

This is the mode to access to register `fifo`.

6.3.2 Snapshot Mode

This is the mode to access to 0x00C0-00FF area. Only read is available to access to this area from Host Interface.

6.4. Access to I-RAM/D-RAM

While stalling paraForce, internal I-RAM/D-RAM area can be accessible from Host Interface. The register `ram_adr` and `ram_data` are used to access from Host Interface to them. The address to set in register `ram_adr` must be 1 word unit. Table 6-3 shows the address number to set `ram_adr`. The address number is different from Sensor Interface Address Map Figure 7-1.

Table 6-3 the address number to set `ram_adr`

Access to RAM area	<code>ram_adr</code> to set address
D-RAM0	00000000h – 00007FFFh
D-RAM1	00008000h – 0000FFFFh
I-RAM0	00010000h – 00017FFFh
I-RAM1	00018000h – 0001FFFFh

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7. Sensor Interface and Peripheral Specifications

The device provides following interfaces to collect sensor data and connect to other devices.

- I2C master
- SPI master
- GPIO
- PWM
- UART
- Timer

These interfaces are controlled by paraForce and connect to Data Bus. The details of Sensor Interface and Peripherals are given below.

7.1. Address Map

Figure 7-1 shows Address Map of Sensor Interface.

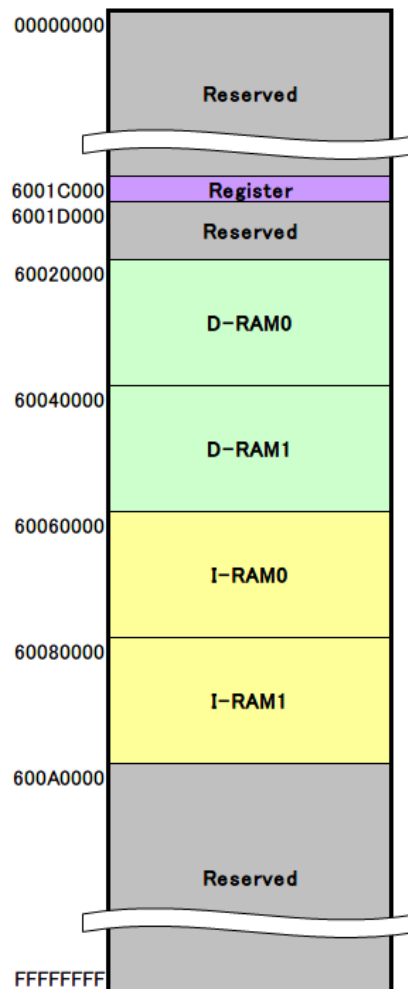


Figure 7-1 Address Map of Sensor Interface

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7.2. I2C

Table 7-1 shows Sensor Interface I2C implementation.

Table 7-1 Sensor Interface I2C implementation

Function	Content
Master/Slave	Master
Clock	CLK_PERI
Specification	<ul style="list-style-type: none"> • Data width : 8bit (ACK signal of 1 bit data is added after 8 bit data) • I2C bus format is based on Philips Update 1995. The device can distinguish between start-condition and stop-condition from the state of I2C bus line. • Standard-mode (transfer at rates of up to 100kbit/s) is available. • Fast-mode (transfer at rates of up to 400kbps) is available.
Interrupt signal	int_i2c

About I2C characteristics, please refer to Figure 6-3 and Table 6-2.

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7.3. SPI

Table 7-2 shows Sensor Interface SPI implementation.

Table 7-2 Sensor Interface SPI implementation

Function	Content
Master/Slave	Master
Clock	CLK_PERI
Specification	<ul style="list-style-type: none"> 3-wired serial interface Slave select signal can be available up to 4 Data width : 8bit Fast bit of serial data : Alternative of MSB or LSB
Interrupt signal	int_spim

Figure 7-2 shows Sensor Interface SPI Timing Diagram.

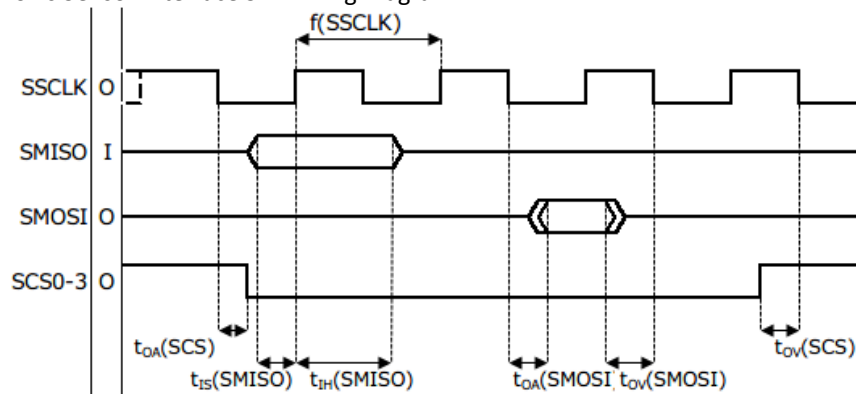


Figure 7-2 Sensor Interface SPI Timing Diagram

Table 7-3 shows Sensor Interface SPI dynamic characteristics.

Table 7-3 Sensor Interface SPI dynamic characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
SPI Clock Frequency	f(SSCLK)		-	8	10.8 ²	MHz
Data input setup Time	t _{IS} (SMISO)		14.5	-	-	ns
Data input hold Time	t _{IH} (SMISO)		0	-	-	ns
Data output Access time	t _{OA} (SMOSI)	output load 35pF@3.3V or 20pF@1.8V	-	-	2.5	ns
	t _{OA} (SCS)	↑	-	-	2.5	ns
Data output Valid time	t _{OV} (SMOSI)	↑	-	-	8	ns
	t _{OV} (SCS)	↑	-	-	8	ns

? SPI clock maximum frequency is one five of CLK_PERI.

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7.4. GPIO

Table 7-4 shows Peripheral GPIO implementation.

Table 7-4 Peripheral GPIO implementation

Function	Content
Port number	Up to 4 (alternative of SS signal for SPI, PWM output, and CTS/RTS signal for UART)
Specification	<ul style="list-style-type: none"> General purpose input and output Hi-Z output after reset-release GPIO2 and GPIO3 can be used external interrupt input.
Interrupt signal	int_gpio2, int_gpio3

7.5. PWM

Table 7-5 shows Peripheral PWM implementation.

Table 7-5 Peripheral PWM implementation

Function	Content
Channel number	Up to 2
Specification	<ul style="list-style-type: none"> Duty setting : 0.0015-99.9985% Period setting : Divide CLK_PERI into 1/2-1/65535 Minimum resolution : (2 / CLK_PERI) sec
Interrupt signal	(none)

7.6. UART

Table 7-6 shows Peripheral UART .

Table 7-6 Peripheral UART implementation

Function	Content
Clock	CLK_PERI
Specification	<ul style="list-style-type: none"> Baud rate : CLK_PERI / 4080 – CLK_PERI / 16 bps Format : <ul style="list-style-type: none"> Data bit : 5 - 8bits Stop bit : 1 or 2 bits Parity bit : odd, even, not use FIFO size : Transfer 128byte, Receiver 128byte Hardware flow control can be available
Interrupt signal	int_uart

7.7. Timer

7.7.1 General-purpose timers

Table 7-7 shows General-purpose timers implementation.

Table 7-7 General-purpose timers implementation

Function	Content
Channel number	3 independent channels
Specification	<ul style="list-style-type: none"> 32-bit resolution interval timer Counter clock : CLK_XT Interval period settings : $0 \sim 2^{32} - 1$
Interrupt signal	TIM0, TIM1, TIM2

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7.7.2 Awake timer

Table 7-8 shows Awake timer implementation.

Table 7-8 Awake timer implementation

Function	Content
Channel number	1
Specification	<ul style="list-style-type: none">• 32-bit resolution interval timer• Counter clock : ROSC1 (100kHz) or external clock• Interval period settings : $0 \sim 2^{32} - 1$
Interrupt signal	int_aware

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8. Interrupt

There are 16 interrupt at the paraForce, including 4 external interrupt. Please refer User's Manual about interrupt details.

Table 8-1 Interrupt controller

#	Name	Interrupt Event	Priority level	type
0	TIM0	General-purpose timer0	1	Timer
1	TIM1	General-purpose timer1	2	Timer
2	message		4	Level
3	TIM2	General-purpose timer	3	Timer
4	AWake	Awake timer	4	Level
5	I2C master		1	Level
6	UART Master		1	Level
7	GPIO3	External interrupt 1	1	Level
8	(not use)	-	-	-
9	SPI Master		1	Level
10	GPIO2	External interrupt 0	1	Level
11	(not use)	-	-	-
12	(not use)	-	-	-
13	FIFO RD	DPBUS FIFO	1	Edge
14	GPIO3	External interrupt 1	1	Edge
15	GPIO2	External interrupt 0	1	Edge

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9. Absolute Maximum Ratings

Table 9-1 Absolute Maximum Ratings

Ratings	Symbol	Min.	Max.	Unit
I/O Power Supply Voltage	DVDD18	-0.5	3.63	V
Core Power Supply Voltage	DVDD12	-0.5	1.32	V
Analog Power Supply Voltage	ROSC_AVDD	-0.5	1.32	V
IO Voltage	VPAD	-0.5	DVDD18 + 0.5	V
Junction Operating Temperature	Tj	-40	125	C
Storage Temperature range for packed material	-	5	35	C
Storage Humidity range for packed material	-	-	85	%RH

10. Recommended Operating Conditions

Table 10-1 Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
I/O Power Supply	DVDD18	1.8V	1.62	1.8	1.98	V
		2.5V	2.25	2.5	2.75	V
		2.8V	2.52	2.8	3.08	V
		3.0V	2.7	3	3.3	
		3.3V	2.97	3.3	3.63	V
Core Power Supply	DVDD12	1.2V	1.08	1.2	1.32	V
Analog Power Supply	ROSC_AVDD	1.2V	1.08	1.2	1.32	V
Ambient Temperature	Ta	-	-20	-	85	C

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11. DC Characteristics

Table 11-1 DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit		
High-Level Input Voltage	VIH	DVDD18=1.8V	-	0.7*DVDD18	-	DVDD18+0.3	V	
		DVDD18=3.3V	-	0.7*DVDD18	-	DVDD18+0.3	V	
Low-Level Input Voltage	VIL	DVDD18=1.8V	-	DVSS-0.3	-	0.3*DVDD18	V	
		DVDD18=3.3V	-	DVSS-0.3	-	0.3*DVDD18	V	
Hysteresis Schmitt Trigger	VHYS	-	-	0.4	-	-	V	
DC Current	IOH	DVDD18=1.8V VOH=DVDD18-0.4	2mA	3.6	-	-	mA	
			4mA	7.3	-	-	mA	
			8mA	9.8	-	-	mA	
			12mA	13.5	-	-	mA	
		DVDD18=2.5V VOH=DVDD18-0.4	2mA	3.8	-	-	mA	
			4mA	5.7	-	-	mA	
			8mA	9.5	-	-	mA	
			12mA	11.5	-	-	mA	
		DVDD18=3.3V VOH=DVDD18-0.4	2mA	4.9	-	-	mA	
			4mA	7.3	-	-	mA	
			8mA	12.3	-	-	mA	
			12mA	14.8	-	-	mA	
	IOL	DVDD18=1.8V VOH=0.4V	2mA	4.3	-	-	mA	
			4mA	8.7	-	-	mA	
			8mA	11.7	-	-	mA	
			12mA	16	-	-	mA	
		DVDD18=2.5V VOH=0.4V	2mA	4.4	-	-	mA	
			4mA	6.6	-	-	mA	
			8mA	11.1	-	-	mA	
			12mA	13.1	-	-	mA	
		DVDD18=3.3V VOH=0.4V	2mA	5.5	-	-	mA	
			4mA	8.2	-	-	mA	
			8mA	13.8	-	-	mA	
			12mA	16.6	-	-	mA	
Static Output Voltage High	VOH	DVDD18=1.62V	2mA	DVDD18-0.4	-	-	V	
			12mA	DVDD18-0.4	-	-	V	
		DVDD18=2.97V	2mA	DVDD18-0.4	-	-	-	V
			12mA	DVDD18-0.4	-	-	-	V
Static Output Voltage Low	VOL	DVDD18=1.62V	2mA	-	-	0.4	V	
			12mA	-	-	0.4	V	
		DVDD18=2.97V	2mA	-	-	0.4	V	
			12mA	-	-	0.4	V	
Pull-down current	IPD	DVDD18=1.8V	-	17	36	96	uA	
		DVDD18=3.3V	-	19	41	158	uA	
Pull-up current	IPU	DVDD18=1.8V	-	16	30	52	uA	
		DVDD18=3.3V	-	38	62	101	uA	

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12. AC Characteristics

Table 12-1 AC Characteristics (DVDD=1.8V)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Propagation Delay	tPD	Output 12mA	CLOAD=20pF	-	3.5	-	ns
		Input	CLOAD=0.2pF	-	1.1	-	ns
		Input with schmitt		-	1.2	-	ns
Rise Time 10% to 90%	tr	Output 12mA	CLOAD=20pF	-	2	-	ns
		Input	CLOAD=0.2pF	-	0.2	-	ns
		Input with schmitt		-	0.2	-	ns
Fall Time 90% to 10%	tf	Output 12mA	CLOAD=20pF	-	1.7	-	ns
		Input	CLOAD=0.2pF	-	0.2	-	ns
		Input with schmitt		-	0.2	-	ns

Table 12-2 AC Characteristics (DVDD=3.3V)

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Propagation Delay	tPD	Output 12mA	CLOAD=20pF	-	2.6	-	ns
		Input	CLOAD=0.2pF	-	0.7	-	ns
		Input with schmitt		-	0.9	-	ns
Rise Time 10% to 90%	tr	Output 12mA	CLOAD=20pF	-	1.6	-	ns
		Input	CLOAD=0.2pF	-	0.2	-	ns
		Input with schmitt		-	0.2	-	ns
Fall Time 90% to 10%	tf	Output 12mA	CLOAD=20pF	-	1.7	-	ns
		Input	CLOAD=0.2pF	-	0.2	-	ns
		Input with schmitt		-	0.2	-	ns

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13. Ball Map

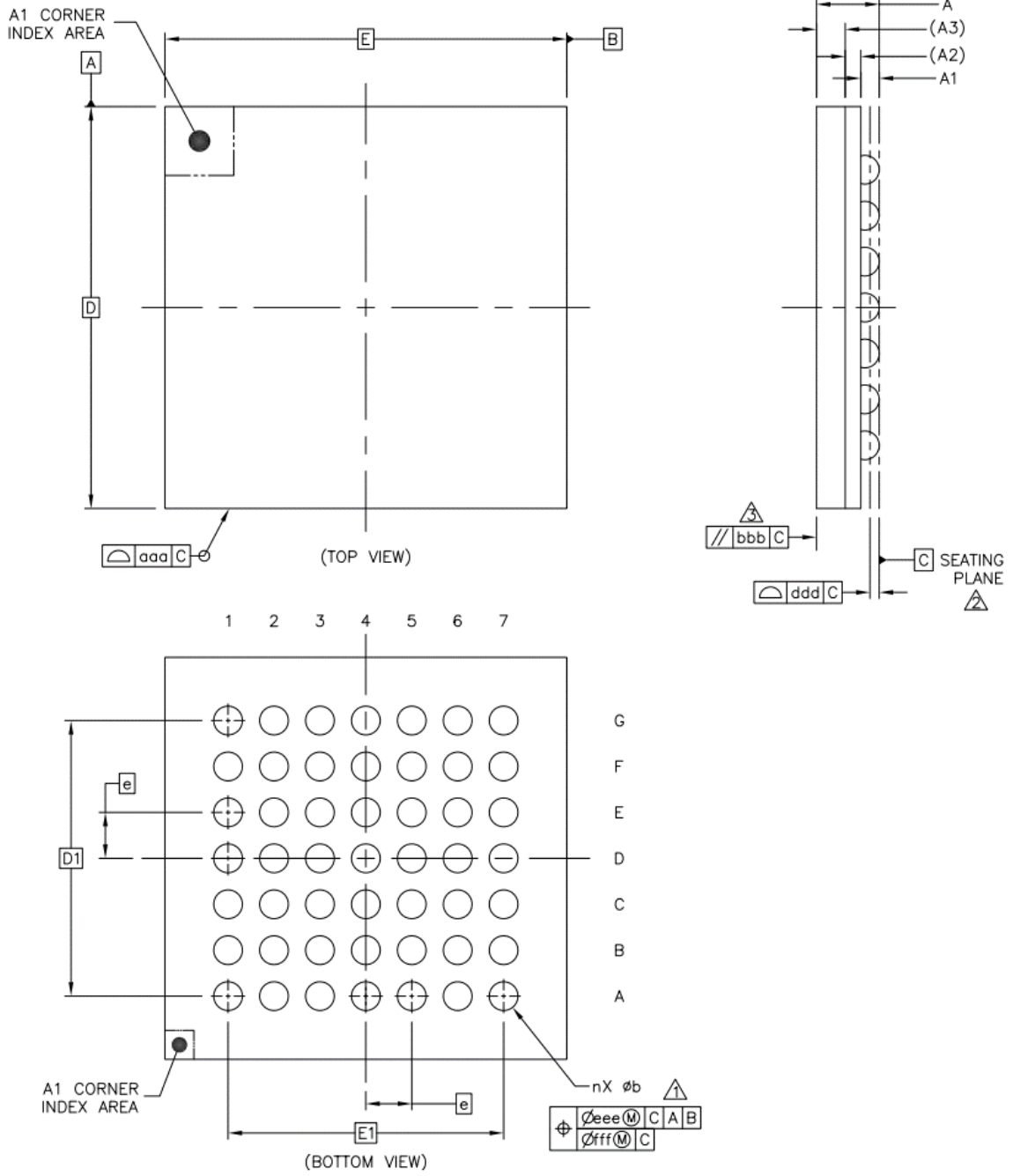
	1	2	3	4	5	6	7	
A	NC	DVSS	CLKIN	DVDD12	DVSS	DVDD18	NC	A
B	DVDD12	DVDD18	SELCLK	DSRUN	STANDBY	HSS	HMISO	B
C	GPIO0	GPIO3	SEL0	SEL1	SELVDD	HMOSI	HSCLK	C
D	JTCK	GPIO1	GPIO2	DVSS	SELRST	DVDD12	ROSC_AVDD	D
E	JTRST	JTDO	SRX	DVSS	RSTB	DVSS	ROSC_AVSS	E
F	JTMS	JTDI	STX	SMISO	SSCLK	SMOSI	DVDD18	F
G	NC	DVDD18	DVSS	DVDD12	SSCL	SSDA	NC	G
	1	2	3	4	5	6	7	

Figure 13-1 Ball Map (Top View)

In Figure 13-1, NC pin MUST be non-connection, take care not to connect to Power Pin (DVDD12, DVDD18, ROSC_AVDD), GND pin (DVSS, ROSC_DVSS), and other signal pins.

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14. Outline Drawing



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	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	0.65
STAND OFF	A1	0.11	---	0.21
SUBSTRATE THICKNESS	A2	0.136		REF
MOLD THICKNESS	A3	0.25		REF
BODY SIZE	D	3.5		BSC
	E	3.5		BSC
BALL DIAMETER		0.25		
BALL OPENING		0.22		
BALL WIDTH	b	0.2	---	0.3
BALL PITCH	e	0.4		BSC
BALL COUNT	n	49		
EDGE BALL CENTER TO CENTER	D1	2.4		BSC
	E1	2.4		BSC
BODY CENTER TO CONTACT BALL	SD	---		BSC
	SE	---		BSC
PACKAGE EDGE TOLERANCE	aaa	0.1		
MOLD FLATNESS	bbb	0.1		
COPLANARITY	ddd	0.08		
BALL OFFSET (PACKAGE)	eee	0.15		
BALL OFFSET (BALL)	fff	0.08		

NOTES:

- ⚠ DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
- ⚠ DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- ⚠ PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 14-1 Package Outline Drawing³⁴⁵

³⁴⁵ The unit of package outline drawing is a millimeter.

³⁴⁶ REF stands for Reference. BSC stands for Basic Spacing between Centers.

³⁴⁷ BALL DIAMETER means ball size before ball mount, BALL WIDTH means ball size after ball mount.

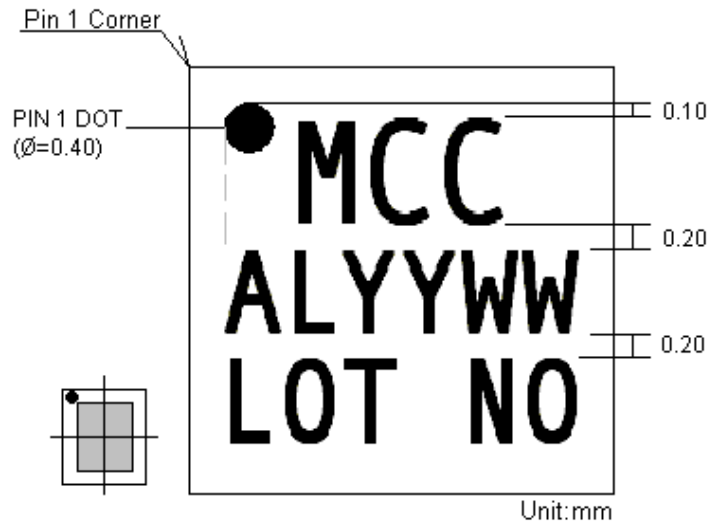
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15. Marking Specification



	Description	Position	Font Type	Height	Width	Space	Max Width	Max chars
				↓	↔	↔	↔	
Line 1	MCC	Center	ARIAL-0.FNT	0.88 mm	0.50 mm	0.10 mm	1.70 mm	3
Line 2	ALYYWW	Center	ARIAL-0.FNT	0.70 mm	0.40 mm	0.10 mm	2.90 mm	6
Line 3	LOT NO	Center	ARIAL-0.FNT	0.70 mm	0.40 mm	0.10 mm	2.90 mm	6

Figure 15-1 Marking Specification

16. Recommended Land Pattern

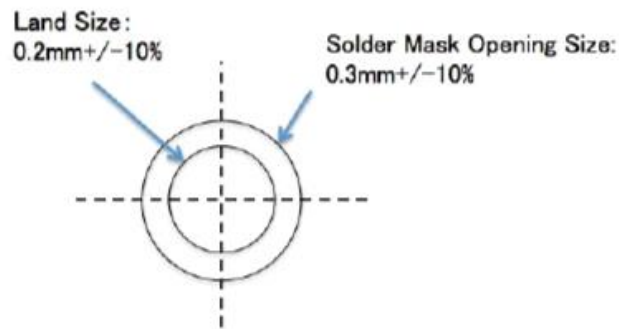


Figure 16-1 Recommended Land Pattern

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17. Power Sequence

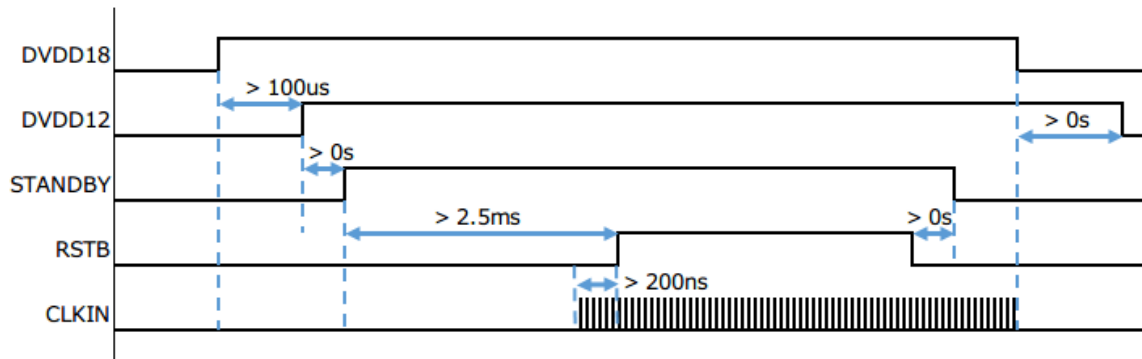


Figure 17-1 Power Sequence

Please set voltage of 1.2V power supply not to exceed voltage of 3.3V power supply at startup and shutdown.

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18. Pin Process/ Peripherals

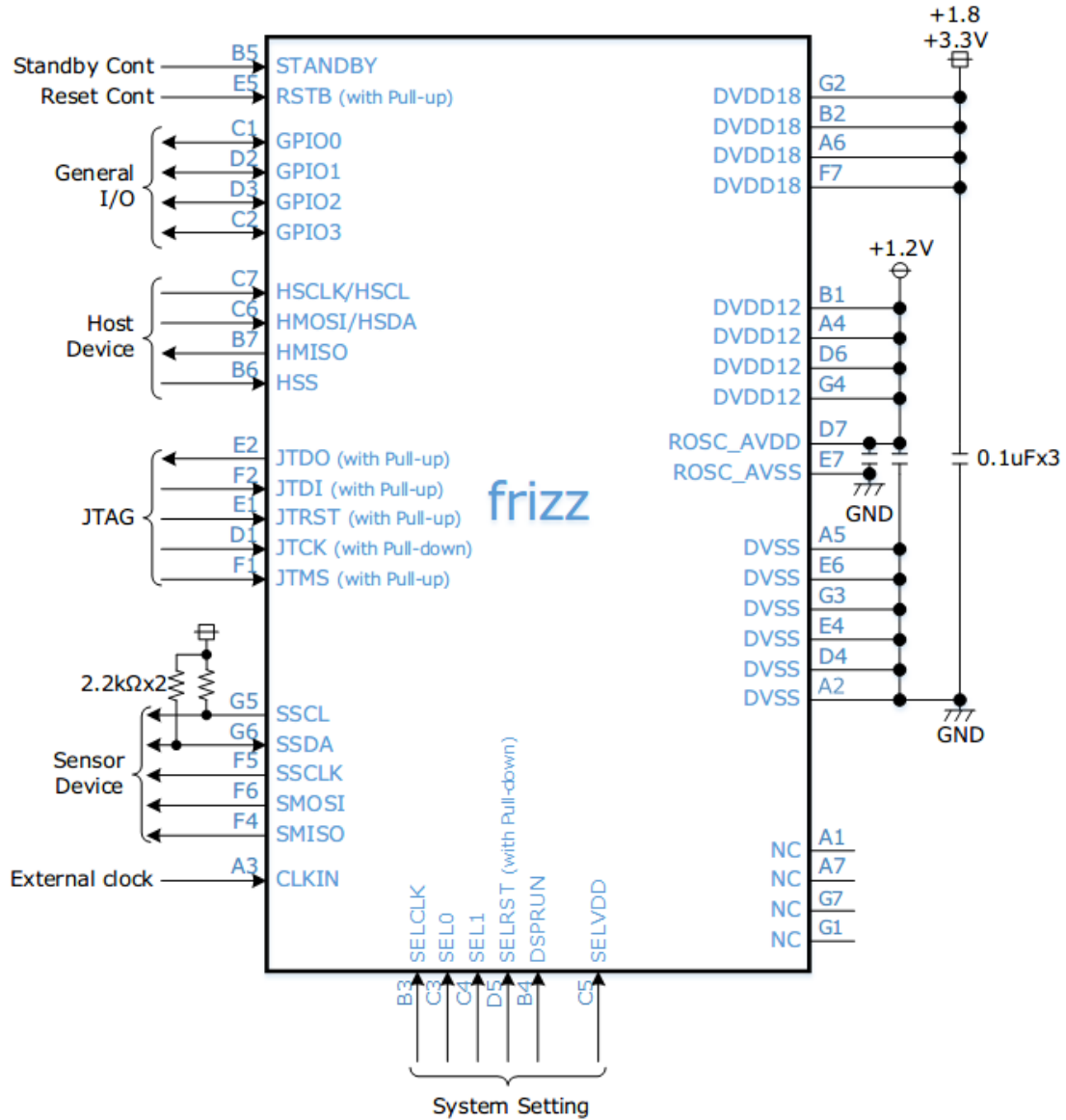


Figure 18-1 Pin Process/Peripherals

Definition/Revision History						
Standard	frizz ES1 Product Specification		No.	SPS-MA60000-EN		
Date of D/R/A	Rev.	Contents of Definition/Revision	D/R/A by			
			Final Aprv.	Aprv.	Rvw.	Crt.
/ /2014		Released		Naka-mura	Matsu-moto	Yoshi-mura