Rapid Charge™ AC/DC Digital Quasi-Resonant PWM Controller

1.0 Features

- Supports rapid charge technologies such as Qualcomm® Quick Charge™ 2.0 (QC2.0) technology to provide 5V/9V/12V with user-selected various output current limit combinations
- Proprietary secondary-to-primary digital communication and built-in decoder eliminate discrete decoder and significantly simplify system design
- Single opto-coupler for all the rapid charge information: output voltage request, output current limit, output voltage undershoot, and over-voltage protection
- Tight multi-level constant-voltage and multi-level constant-current regulation with primary-side feedback and control
- Ultra-low no-load power consumption with lowest system cost (< 10mW at $230V_{AC}$ with typical 5V2A setting using Schottky diode rectifer; < 20mW at $230V_{AC}$ with typical 5V2A setting using synchronous rectifier)
- Fast dynamic load response (DLR) with secondary-side load transient detection
- Proprietary optimized line/load adaptive maximum constant frequency PWM switching with quasi-resonant operation achieves best size, efficiency, and common mode noise
- Multi-mode PWM/PFM control improves efficiency at various load conditions
- User-configurable 5-level cable drop compensation independant of output votlage
- EZ-EMI® design enhances manufacturability
- Built-in single-point fault protections against output short-circuit including soft short and half short, output over-voltage, and output over-current
- SmartDefender™ smart hiccup technology helps address issues of soft shorts in cables and connectors by effectively reducing the average output power at fault conditions without latch
- User-configurable external shutdown control
- No audible noise over entire operating range

2.0 Description

The iW1780 is a high performance AC/DC power supply controller for rapid charge that uses digital control technology to build peak-current mode PWM flyback power supplies. The device operates in quasi-resonant mode to provide high efficiency and a number of key built-in protection features. The iW1780 can achieve tight multi-level constant voltage and multi-level constant current regulation without traditional secondary-feedback circuit. It also eliminates the need for loop compensation components while maintaining stability over all operating conditions.

The iW1780 is optimized to work with Dialog's secondary-side controller for QC 2.0 interface and secondary-primary communication, iW626, to achieve fast and smooth voltage transition upon request by portable devices (PD). When paired with the iW626, the iW1780 eliminates the discrete decoders in the primary side, minimizes the external component count and simplifies system designs. The iW626 can communicate with the iW1780 through one opto-coupler for all the necessary rapid charge information including output voltage requests, output current limits, output voltage undershoot and output over-voltage.

Dialog's innovative proprietary technology ensures that power supplies designed with the iW1780 and iW626 can provide 5V/9V/12V output voltage configuration, with user-selected various output current limit combinations. Furthermore, the chipset can achieve <10mW no-load power consumption at 5V2A output setting and fast dynamic load response in typical AC/DC HVDCP adapter designs.

3.0 Applications

- Rapid-charging AC/DC adapters for smart phones, tablets and other portable devices (5V-12V, 1A-3A).

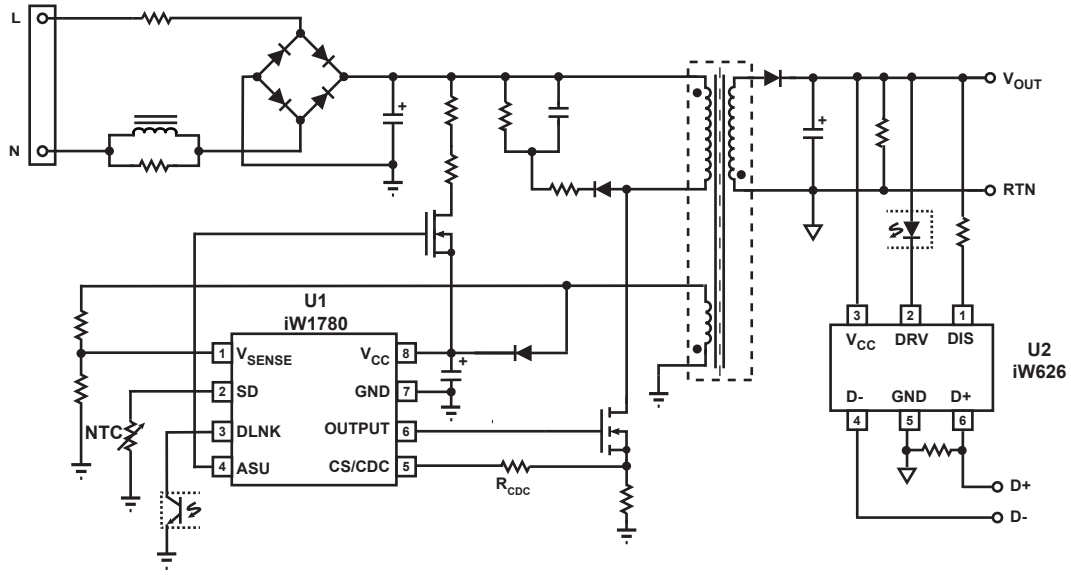

Figure 3.1: iW1780 Typical Application Circuit for Multi-Level Output Voltage and Current
(Using iW626 as Secondary-Side Controller for QC2.0. Achieving < 10mW No-Load Power Consumption)

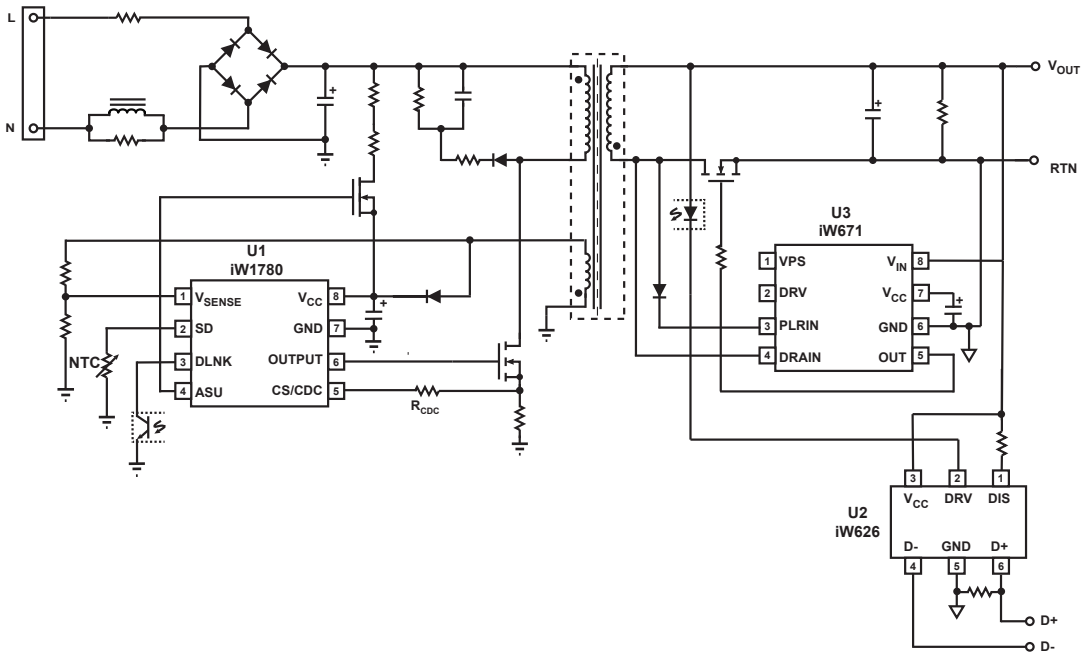

Figure 3.2: iW1780 Typical Application Circuit for Multi-Level Output Voltage and Current
(Using iW626 as Secondary-Side Controller for QC2.0 and iW671 as Synchronous Rectifier Controller.
Achieving < 20mW No-Load Power Consumption)

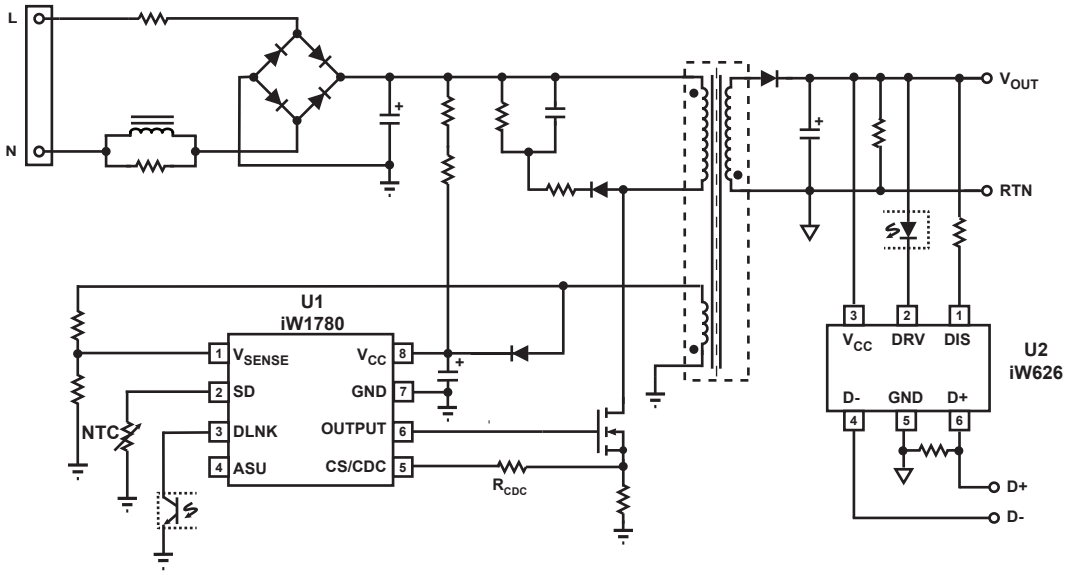

Figure 3.3: iW1780 Typical Low Cost Application Circuit for Multi-Level Output Voltage and Current (Using iW626 as Secondary-Side Controller for QC2.0. Achieving < 50mW No-Load Power Consumption Without Using Active Start-up Device)

4.0 Pinout Description

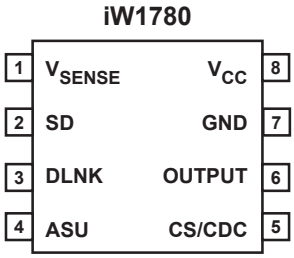

Figure 4.1: 8-Lead SOIC Package

Pin #	Name	Type	Pin Description
1	V_{SENSE}	Analog Input	Auxiliary voltage sense. Used for primary-side regulation.
2	SD	Analog Input	External shutdown control. Can be configured for external over-temperature protection (OTP) by connecting an NTC resistor from this pin to Ground.
3	DLNK	Analog Input	Digital communication link signal. Used for secondary-side to primary-side communication for all rapid charge information, which includes output voltage requests, output current limits, output voltage undershoot, and over-voltage protection.
4	ASU	Output	Control signal. Used for active start-up device (BJT or depletion mode N-FET).
5	CS/CDC	Analog Input	Primary-side current sense and external cable drop compensation (CDC). Used for cycle-by-cycle peak-current control and limit in primary-side CV/CC regulation. Also used for CDC configuration.
6	OUTPUT	Output	Gate drive for external MOSFET switch.
7	GND	Ground	Ground.
8	V_{CC}	Power Input	IC power supply.

5.0 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to Electrical Characteristics in Section 6.0.

Parameter	Symbol	Value	Units
DC supply voltage range (pin 8, I_{CC} = 20mA max)	V_{CC}	-0.3 to 25.0	V
Continuous DC supply current at V_{CC} pin (V_{CC} = 15V)	I_{CC}	20	mA
ASU output (pin 4)		-0.3 to 19.0	V
OUTPUT (pin 6)		-0.3 to 20.0	V
V_{SENSE} input (pin 1, I_{Vsense} ≤ 10mA)		-0.7 to 10.0	V
CS/CDC input (pin 5)		-0.3 to 4.0	V
SD (pin 2)		-0.3 to 4.0	V
DLINK (pin 3)		-0.3 to 4.0	V
Maximum junction temperature	T_{JMAX}	150	°C
Operating junction temperature	T_{JOPT}	-40 to 150	°C
Storage temperature	T_{STG}	-65 to 150	°C
Thermal resistance junction-to-ambient	θ_{JA}	160	°C/W
ESD rating per JEDEC JESD22-A114		±2,000	V
Latch-up test per JESD78A		±100	mA

6.0 Electrical Characteristics

V_{CC} = 12V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{SENSE} SECTION (Pin 1)						
Input leakage current	I_{BVS}	V_{SENSE} = 2V			1	µA
Nominal voltage threshold at 5V output	$V_{SENSE\_5V(NOM)}$	5V V_{OUT}, T_A=25°C, negative edge	1.521	1.536	1.551	V
Output OVP threshold with no CDC compensation at 5V output (Note 1)	$V_{SENSE\_5V(MAX)}$	5V V_{OUT}, T_A=25°C, negative edge		1.838		V
CS/CDC SECTION (Pin 5)						
Switching-cycle over-current threshold	V_{OCP}		1.11	1.15	1.19	V
CS regulation upper limit (Note 2)	$V_{IPK(HIGH)}$			1.00		V
CS regulation lower limit (Note 2)	$V_{IPK(LOW)}$	(Note 2)		0.23		V
Input leakage current	I_{LK}	$V_{CS/CDC}$ = 1.0V			1	µA
SD SECTION (Pin 2)						
Shutdown threshold (falling edge)	$V_{SD-TH(F)}$		0.95	1.0	1.05	V
Shutdown threshold before start-up	$V_{SD-TH(ST\_F)}$		1.14	1.2	1.26	V

Electrical Characteristics (cont.)

V_{CC} = 12V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown current source	I_{SD}		95	100	105	µA
DLINK SECTION (Pin 3)						
Detection threshold (falling edge)	$V_{DLINK-TH(F)}$			1.7		V
Recovery threshold (rising edge)	$V_{DLINK-TH(R)}$			2.0		V
DLINK current source	I_{DLINK}			200		µA
OUTPUT SECTION (Pin 6)						
Driver pull-down ON-resistance	$R_{DS(ON)PD}$	I_{SINK} = 5mA		16		Ω
Driver pull-up ON-resistance	$R_{DS(ON)PU}$	I_{SOURCE} = 5mA		80		Ω
Rise time (Note 2)	t_R	T_A = 25°C, C_L = 330pF 10% to 90%		95		ns
Fall time (Note 2)	t_F	T_A = 25°C, C_L = 330pF 90% to 10%		14		ns
Maximum switching frequency at 5V V_{OUT} PWM mode (Note 3)	$f_{SW\_5V\_PWM}$	At PWM mode		70		kHz
Maximum switching frequency at 9V/12V V_{OUT} PWM mode (Note 3)	$f_{SW\_9V\_12V\_PWM}$	At PWM mode		89		kHz
V_{CC} SECTION (Pin 8)						
Operating voltage (Note 2)	V_{CC}				20	V
Start-up threshold	$V_{CC(ST)}$	V_{CC} rising	12.7	13.7	14.7	V
Under-voltage lockout threshold	$V_{CC(UVL)}$	V_{CC} falling		6.5		V
Latch release threshold	$V_{CC(RLS)}$	V_{CC} falling		4.5		V
V_{CC} over-voltage protection level (Note 2)	$V_{CC(OVP)}$	V_{CC} rising		23		V
Start-up current	$I_{IN(ST)}$	V_{CC} = 12V		7.6		µA
Quiescent current	I_{CCQ}	C_L = 330pF, V_{SENSE} = 1.5V		4.1		mA
No-load operating current (Note 2 & 4)	I_{CC_NL}	No-load operation		0.25		mA
ASU SECTION (Pin 4)						
Maximum operating voltage (Note 2)	$V_{ASU(MAX)}$				16	V
Resistance between V_{CC} and ASU	R_{Vcc_ASU}			1100		kΩ
THERMAL CHARACTERISTICS						
Thermal Shutdown Threshold (Note 2)	T_{SD}			150		°C
Thermal Shutdown Recovery (Note 2)	T_{SD-R}			TBD		°C

Electrical Characteristics (cont.)

V_{CC} = 12V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Notes:

Note 1: The output OVP threshold depends on the CDC setup, see Section 9.13 for more details.

Note 2: These parameters are not 100% tested. They are guaranteed by design and characterization.

Note 3: Operating frequency varies based on the load conditions, see Section 9.6 for more details.

Note 4: See Section 9.6 and 9.7 for details.

7.0 Typical Performance Characteristics

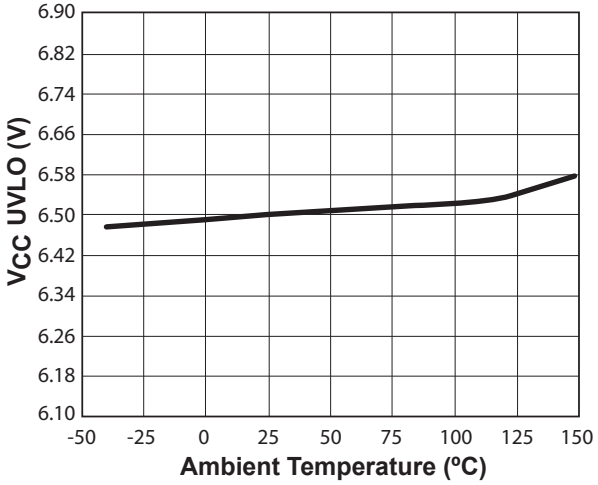

Figure 7.1 : V_{CC} UVLO vs. Temperature

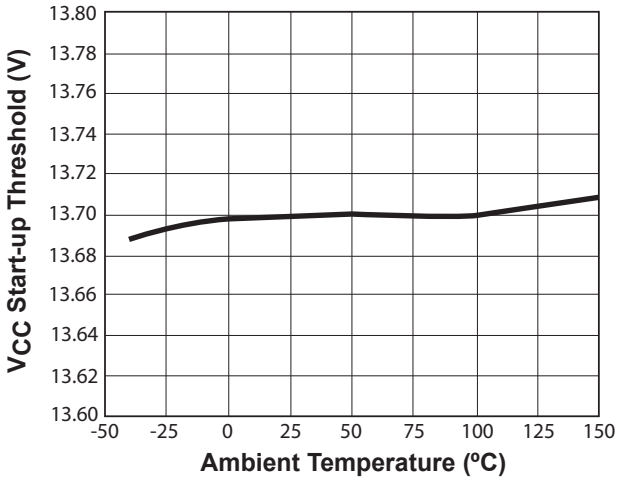

Figure 7.2 : Start-Up Threshold vs. Temperature

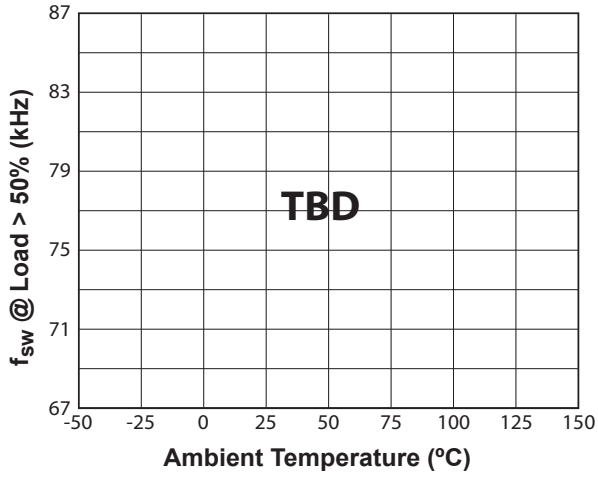

Figure 7.3 : Switching Frequency vs. Temperature[1]

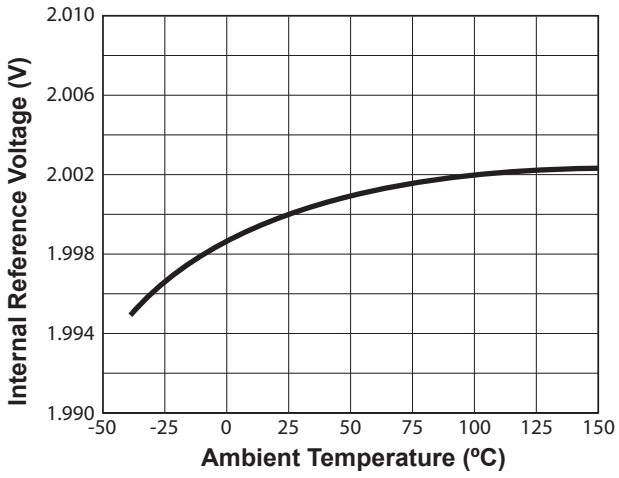

Figure 7.4 : Internal Reference vs. Temperature

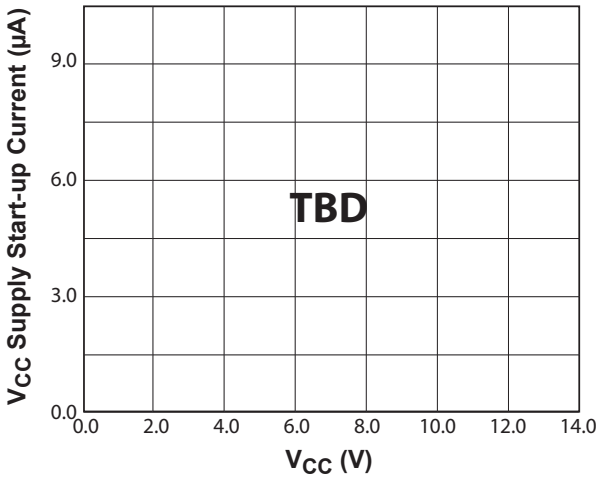

Figure 7.5 : V_{CC} vs. V_{CC} Supply Start-up Current

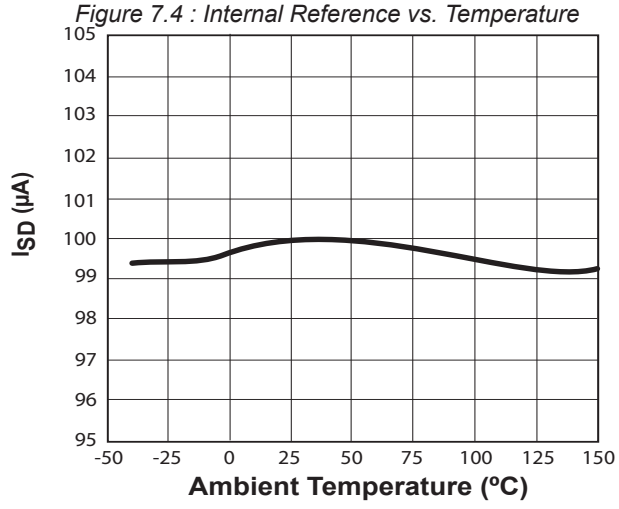

Figure 7.6 : I_{SD} vs. Temperature

Notes:

Note 1. Operating frequency varies based on the load conditions, see Section 9.6 for more details.

8.0 Functional Block Diagram

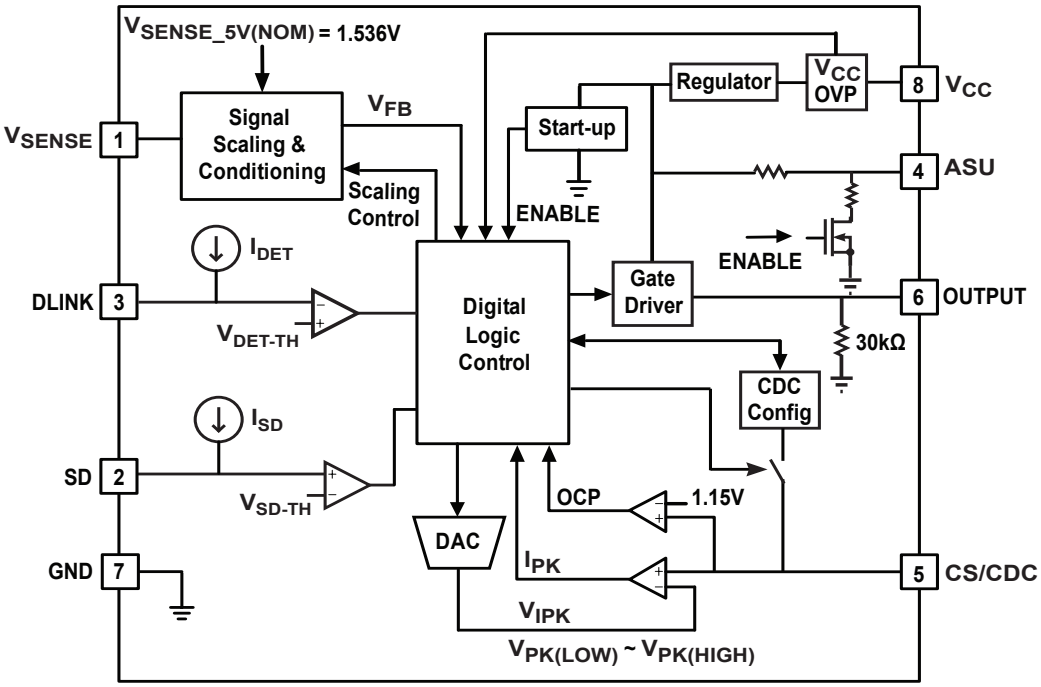

Figure 8.1 : iW1780 Functional Block Diagram

9.0 Theory of Operation

The iW1780 is a digital controller for rapid charge, which uses a proprietary primary-side control technology to eliminate secondary regulation and feedback circuits required in traditional designs. The core PWM processor uses fixed-frequency Discontinuous Conduction Mode (DCM) operation at higher power levels and switches to variable frequency operation at light loads to maximize efficiency. Furthermore, Dialog's digital control technology enables fast dynamic response, tight multi-level output voltage and multi-level current regulation, and full-featured circuit protections. The iW1780 is optimized to work with Dialog's secondary-side controller for QC2.0 interface and secondary-to-primary-side communication, iW626, to achieve fast and smooth voltage and current transition upon request from portable devices (PD). When paired with the iW626, the iW1780 eliminates the discrete decoders on the primary side, minimizes the external component count and simplifies system designs. The iW626 can communicate with the iW1780 through one opto-coupler for all the necessary rapid charge information including output voltage requests, output current limits, output voltage undershoot and output over-voltage.

Figure 8.1 shows the iW1780 operates in peak current mode control. The digital logic control block generates the switching on-time and off-time information based on the output voltage and current feedback signal and provides commands to dynamically control the external MOSFET gate voltage. The CS/CDC pin is an analog input configured to sense the primary current in a voltage form after CDC configuration is finished. In order to achieve the peak current mode control and cycle-by-cycle current limit, the V_{IPK} sets the threshold for the CS/CDC pin voltage to compare with, and it varies in the range of $V_{IPK(LOW)}$ to $V_{IPK(HIGH)}$ under different line and load conditions. The system loop is automatically compensated internally by a digital error amplifier. Adequate system phase margin and gain margin are guaranteed by design and no external analog components are required for loop compensation. The iW1780 uses an advanced digital control algorithm to reduce system design time and increase reliability.

Furthermore, accurate secondary constant current operation is achieved without the need for traditional secondary-side feedback and control circuits.

The iW1780 uses adaptive multi-mode PWM/PFM control to dynamically change the MOSFET switching frequency for efficiency, EMI, and power consumption optimization. In addition, it achieves unique MOSFET quasi-resonant switching to further improve efficiency and reduce EMI. The built-in single-point fault protection features include over-voltage protection (OVP), output short-circuit protection (SCP), over-current protection (OCP), and current sense fault detection. In particular, it ensures that power supplies built with the iW1780 can achieve less than 20mW no-load power consumption in a typical 15W multi-level output voltage AC/DC off-line power adapter applications such as QC2.0 power adapters for cellular phones and tablets.

Dialog's digital control scheme is specifically designed to address the challenges and trade-offs of power conversion design. This innovative technology is ideal for balancing new regulatory requirements for green mode operation with more practical design considerations such as lowest possible cost, smallest size and high performance output control.

9.1 Pin Detail

Pin 1 – V_{SENSE}

Sense signal input from auxiliary winding. This provides the secondary voltage feedback used for output regulation.

Pin 2 – SD

External shutdown control. If the voltage at this pin is lower than 1.2V (typical) at the beginning of start-up or lower than 1.0V (typical) during normal operation, then the IC shuts down. Leave this pin unconnected if the shutdown control is not used (Refer to Section 9.14).

Pin 3 – DLINK

Digital communication link signal. Used for secondary-side to primary-side communication for all rapid charge information, including output voltage requests, output current limits, output voltage undershoot, and over-voltage protection.

Pin 4 – ASU

Control signal for active startup device. This signal is pulled low after start-up is finished to cut off the active device.

Pin 5 – CS/CDC

Primary-side current sense and external cable drop compensation (CDC). Used for cycle-by-cycle peak current control and limit. It is also used to configure CDC at the beginning of start-up.

Pin 6 – OUTPUT

Gate drive for the external power MOSFET switch.

Pin 7 – GND

Ground.

Pin 8 – V_{CC}

Power supply for the controller during normal operation. The controller starts up when V_{CC} reaches 13.7V (typical) and shuts down when the V_{CC} voltage drops below 6.5V (typical). A decoupling capacitor of 0.1µF or so should be connected between the V_{CC} pin and GND.

9.2 Active Start-up and Soft-Start

Refer to Figure 3.1 for active start-up circuits using external depletion mode NFET. Prior to start-up, the ENABLE signal is low, and the ASU pin voltage closely follows the V_{CC} pin voltage, as shown in Figure 9.1. Consequently, the depletion mode NFET is switched on, allowing the start-up current to charge the V_{CC} bypass capacitor. When the V_{CC} bypass capacitor is charged to a voltage higher than the start-up threshold $V_{CC(ST)}$, the ENABLE signal becomes active and the iW1780 begins to perform the initial OTP check (See Section 9.14), followed by CDC configuration (See Section 9.13). Afterwards, the iW1780 commences the soft-start function. During this start-up process an adaptive soft-start control algorithm is applied, where the initial output pulses are small and gradually get larger until the full pulse width is achieved. The peak current is limited cycle by cycle by the I_{PEAK} comparator. If at any time the V_{CC} voltage drops below the under-voltage lockout (UVLO) threshold $V_{CC(UVL)}$ then the iW1780 goes to shutdown. At this time the ENABLE signal becomes low and the V_{CC} capacitor begins to charge up again towards the start-up threshold to initiate a new soft-start process.

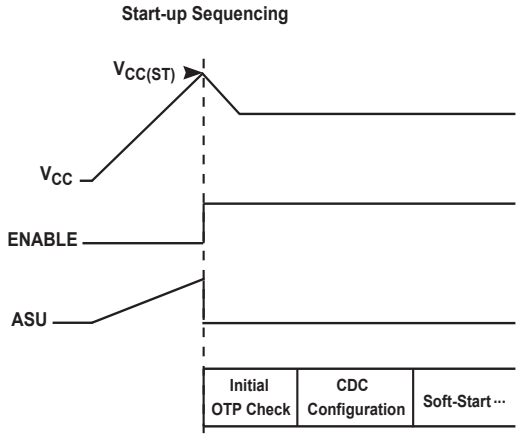

Figure 9.1: Start-up Sequencing Diagram

While the ENABLE signal initiates the soft-start process, it also pulls down the ASU pin voltage, which turns off the depletion NFET, minimizing the no-load standby power consumption.

In applications where active start-up is not needed, the start-up resistor can be directly connected to the V_{CC} pin without using the active start-up device, and the ASU pin can be left unconnected.

It is recommended that the V_{SENSE} voltage divider is set to 5V default output voltage. The power adapter starts up to default 5V state and waits for further voltage/current requests.

9.3 Understanding Primary Feedback

Figure 9.2 illustrates a simplified flyback converter. When the switch Q1 conducts during $t_{ON}(t)$, the current $i_g(t)$ is directly drawn from the rectified. The energy $E_g(t)$ is stored in the magnetizing inductance L_M. The rectifying diode D1 is reverse biased and the load current I_O is supplied by the secondary capacitor C_O. When Q1 turns off, D1 conducts and the stored energy $E_g(t)$ is delivered to the output.

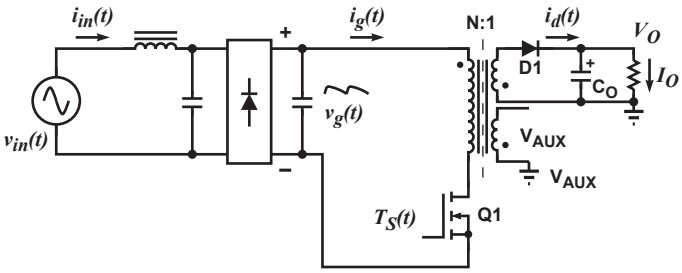

Figure 9.2: Simplified Flyback Converter

In order to tightly regulate the output voltage, the information about the output voltage and load current needs to be accurately sensed. In the DCM flyback converter, this information can be read via the auxiliary winding or the primary magnetizing inductance (L_M). During the Q1 on-time, the load current is supplied from the output filter capacitor C_O. The voltage across L_M is $v_g(t)$, assuming the voltage dropped across Q1 is zero. The current in Q1 ramps up linearly at a rate of:

$$\frac{di_g(t)}{dt} = \frac{v_g(t)}{L_M} \qquad (9.1)$$

At the end of on-time, the current has ramped up to:

$$i_{g\_peak}(t) = \frac{v_g(t) \times t_{ON}}{L_M} \qquad (9.2)$$

This current represents a stored energy of:

$$E_g = \frac{L_M}{2} \times i_{g\_peak}(t)^2 \qquad (9.3)$$

When Q1 turns off at t_O, $i_g(t)$ in L_M forces a reversal of polarities on all windings. Ignoring the communication-time caused by the leakage inductance L_K at the instant of turn-off t_O, the primary current transfers to the secondary at a peak amplitude of:

$$i_d(t) = \frac{N_P}{N_S} \times i_{g\_peak}(t) \qquad (9.4)$$

Assuming the secondary winding is master, and the auxiliary winding is slave,

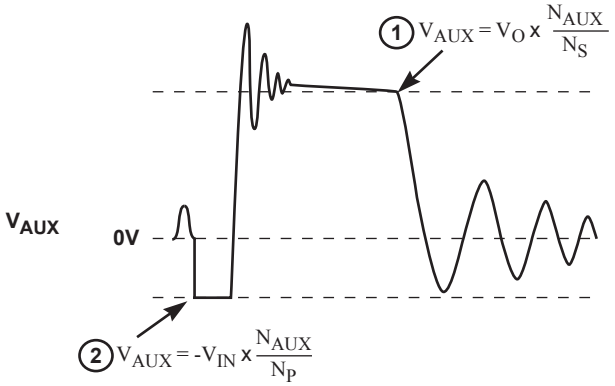

Figure 9.3: Auxiliary Voltage Waveforms

The auxiliary voltage is given by:

$$V_{AUX} = \frac{N_{AUX}}{N_S}(V_O + \Delta V) \qquad (9.5)$$

and reflects the output voltage as shown in Figure 9.3.

The voltage at the load differs from the secondary voltage by a diode drop and IR losses. Thus, if the secondary voltage is always read at a constant secondary current, the difference between the output voltage and the secondary voltage is a fixed ΔV. Furthermore, if the voltage can be read when the secondary current is small, ΔV is also small. With the iW1780, ΔV can be ignored.

The real-time waveform analyzer in the iW1780 reads this information cycle by cycle. The part then generates a feedback voltage V_{FB}. The V_{FB} signal precisely represents the output voltage under most conditions and is used to regulate the output voltage.

9.4 Multi-Level Constant Voltage Operation

The iW1780 is designed for the Dialog's Rapid Charge technology and it is optimized to work with Dialog's secondary-side controllers, such as the iW626. The iW626 has a built-in encoder to generate different pulse patterns and drive the internal switch of DRV pin so that the different voltage information together with the associated current limit setting can be sent to the primary side through an opto-coupler. These patterns function as digital communication signals and are received at the DLINK pin of iW1780. They are then decoded into different information including voltage requests, current limit settings, over-voltage and under-voltage.

After a soft-start has been completed, the default output voltage should be 5V and the actual output voltage is related to the external V_{SENSE} voltage divider network and transformer secondary-to-auxiliary winding turns ratio. The digital control block measures the output conditions. It determines the output power levels and adjusts the control system according to a light load or heavy load. If this is in the normal range, the device operates in the Constant Voltage (CV) mode, and changes the pulse width (t_{ON}) and off time (T_{OFF}) in order to meet the output voltage regulation requirements. At the steady-state CV operation of 5V setting, the V_{SENSE} pin voltage at the instant corresponding to point 1 (as indicated in Figure 9.3) is regulated to $V_{SENSE\_5V(NOM)}$ in most conditions, e.g. 1.536V (typical). If the default output voltage is set to 5V, the iW1780 changes the output voltage to 9V or 12V upon request from the secondary-side controller with the built-in primary-side feedback, scaling, and control. Then this V_{SENSE} pin voltage changes in proportion to the different output voltage levels.

If no voltage is detected on V_{SENSE}, it is assumed that the auxiliary winding of the transformer is either open or shorted and the iW1780 shuts down.

9.5 Multi-Level Current Limit and Constant Current Operation

The iW1780 also receives the constant current (CC) limit information associated with voltage request from the iW626. The CC limit is given by

$$I_{CC\_LIMIT} = \frac{k}{2} \times \frac{N}{R_S} \times \eta_x \qquad (9.6)$$

where N is the transformer primary to secondary side winding turns ratio, R_S is the current sense resistor, η_X is the transformer conversion efficiency, and k is a coefficient

set by the iW626 (see iW626 datasheet for pre-defined k information).

In an overload condition, the iW1780 enters CC mode to limit the output current on a cycle-by-cycle basis. In this mode of operation the output current is limited to a constant level regardless of the output voltage, while avoiding continuous conduction mode operation. In case of very heavy loading when the output voltage is low enough, the iW1780 shuts down.

The iW1780 senses the load current indirectly through the primary current, which is detected by the pin I_{SENSE} through a resistor from the MOSFET source to ground.

When operating in the CC mode, with the decrease of equivalent load resistance or battery voltage, both the output voltage and V_{CC} decrease. After the V_{CC} voltage is below UVLO threshold the iW1780 shuts down (see Section 9.10). Meanwhile, the iW1780 monitors the output voltage, and shuts down the system when the detected output voltage is lower than certain level; this is known as the“CC shutdown voltage.” The shutdown can occur under either one of the above two conditions.

Unless specified, the iW1780 provides a “CC shutdown voltage” of 3V, 6.5V and 10V for the output voltage of 5V, 9V and 12V respectively. The “CC shutdown voltage” here refers to the voltage at the cable end, and the output voltage at the PCB end is the sum of the “CC shutdown voltage” and the “cable comp” (specified in Section 9.12). As a result, the “CC shutdown voltage” option can adaptively match the cable voltage drop at CC mode. For instance, at 5V/2A operation state, if the cable resistance is around 150mΩ, the voltage drop across the cable is around 300mV under both the CV mode full load and CC mode conditions. If no CDC is configured, at CV full load, the voltage at the PCB end is around 5V, and the voltage at the cable end is around 4.7V. Then the CC shutdown occurs when the voltage at the PCB end decreases to 3V, and the voltage at the cable end decreases to 2.7V. Normally a CDC is needed in this design to achieve a desirable voltage regulation at CV mode, for example, the CDC is configured as 300mV. Then at CV full load, the voltage at the PCB end is around 5.3V, and the voltage at the cable end is around 5V. Correspondingly the CC shutdown occurs when the voltage at the PCB end decreases to 3.3V, and the voltage at the cable end decreases to 3V.

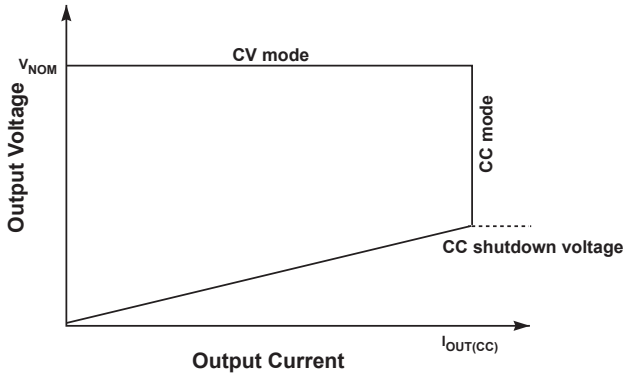

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Figure 9.4: Power Envelope

9.6 Multi-Mode PWM/PFM Control and Quasi-Resonant Switching

The iW1780 uses a proprietary load/line adaptive multi-mode PWM/PFM control to dramatically improve the light-load efficiency and thus the overall average efficiency.

During the constant voltage (CV) operation, the iW1780 normally operates in a pulse-width-modulation (PWM) mode under heavy load conditions. In the PWM mode, the switching frequency keeps around constant. As the output load I_{OUT} is reduced, the on-time t_{ON} is decreased, and the controller adaptively transitions to a pulse-frequency-modulation (PFM) mode. During the PFM mode, the MOSFET is turned on for a set duration under a given instantaneous rectified AC input voltage, but its off time is modulated by the load current. With a decreasing load current, the off-time increases and thus the switching frequency decreases.

When the switching frequency approaches to human ear audio band, the iW1780 transitions to a second level of PWM mode, namely the Deep PWM mode (DPWM). During the DPWM mode, the switching frequency keeps around 22kHz in order to avoid audible noise. As the load current is further reduced, the iW1780 transitions to a second level of PFM mode, namely the Deep PFM mode (DPFM), which can reduce the switching frequency to a very low level. Although the switching frequency drops across the audible frequency range during the DPFM mode, the output current in the power converter has reduced to an insignificant level in the DPWM mode before transitioning to the DPFM mode. Therefore, the power converter practically produces no audible noise, while achieving high efficiency across varying load conditions.

The iW1780 also incorporates a unique proprietary quasi-resonant switching scheme that achieves valley-mode turn on for every PWM/PFM switching cycle, during all

PFM and PWM modes and in both CV and CC operations. This unique feature greatly reduces the switching loss and dv/dt across the entire operating range of the power supply. Due to the nature of quasi-resonant switching, the actual switching frequency can vary slightly cycle by cycle, providing the additional benefit of reducing EMI. The innovative digital control architecture and algorithms together enable the iW1780 to achieve the highest overall efficiency and lowest EMI, without causing audible noise over the entire operating range.

9.7 Less Than 20mW No-Load Power at Typical 5V2A Output Setting

Under the no-load condition, the iW1780 is operating in the DPFM mode, where the switching frequency can drop as low as 140Hz and still maintain a tight closed-loop control of output voltage. The distinctive DPFM operation allows the use of a relatively large pre-load resistor which helps to reduce the no-load power consumption. In the meantime, the iW1780 implements an intelligent low-power management technique that achieves ultra-low chip operating current at the no-load less than 300µA. In addition, the active start-up scheme with depletion NFET eliminates the startup resistor power consumption after the ENABLE signal becomes active. Altogether these features ensure with the lowest system cost power supplies built with the iW1780 can achieve less than 20mW no-load power consumption with output synchronous rectification or less than 10mW with Schottky diode rectification at typical 5V2A output setting and maintain very tight constant voltage and constant current regulation over the entire operating range including the no-load operation. No load power consumption is usually measured with load disconnected. The power supply designed with the iW1780 and iW626 can detect the load disconnection or portable device unplug and change the output voltage to default 5V. Therefore, even the adapter is at 9V or 12V state, it goes to 5V state when no load power consumption is measured with load removed.

9.8 Fast Dynamic Load Response with Secondary-Side Voltage Undershoot Detection

While achieving ultra-low no-load power consumption, the iW1780 implements innovative proprietary digital control technology to receive and respond to secondary-side voltage undershoot signal caused by load transient events through the DLINK pin to ensure adaptive fast dynamic load response.

When a load transient event from a light load to a heavy load happens, the output voltage drops. If the output voltage drops to the voltage undershoot threshold, the iW626 turns on the LED of the opto-coupler by controlling the DRV pin sink current, and the DLNK pin of the iW1780 is pulled down by the transistor of the opto-coupler. After the iW1780 receives this DLNK pin signal, it can intelligently confirm if this signal is caused by an undershoot event and distinguish it from a voltage and current request, and then it promptly increases the switching frequency and the t_{ON} to delivery more power to the secondary side in order to bring the output voltage back to regulation.

9.9 Variable Frequency Operation Mode

During each of the switching cycles, the falling edge of V_{SENSE} is checked. If the falling edge of V_{SENSE} is not detected, the off-time is extended until the falling edge of V_{SENSE} is detected. The maximum allowed transformer reset time is 110µs. When the transformer reset time reaches 110µs, the iW1780 shuts off.

9.10 Internal Loop Compensation

The iW1780 incorporates an internal Digital Error Amplifier with no requirement for external loop compensation. For a typical power supply design, the loop stability is guaranteed to provide at least 45 degrees of phase margin and -20dB of gain margin.

9.11 Voltage Protection Features

The secondary maximum output DC voltage V_{BUS} is limited by the iW1780. In most conditions, when the V_{SENSE} signal at point 1 as indicated in Figure 9.3 exceeds the output OVP threshold, the iW1780 shuts down. While the iW1780 can protect against the V_{OUT} over-voltage through the V_{SENSE} signal in most conditions, it is difficult for the iW1780 to protect the over-voltage caused by output voltage setting mismatch between the iW1780 and the iW626 in some abnormal scenarios. For example, if the iW626 is reset to 5V due to a reset signal from PD or certain other abnormal signals while the iW1780 stays at present 9V or 12V setting, the over-voltage cannot be detected through V_{SENSE} at the primary side. The iW1780/iW626 chipset added one more layer of OVP. When the V_{OUT} rises to above the over-voltage threshold of the iW626's present state, the iW626 drives the DRV pin in a special switching pattern serving as an OVP signal and turns on both the fast and slow discharge. After the iW1780 receives this OVP signal, it shuts down the power supply promptly.

In case of the communication channel failure including the opto-coupler always on or always off, the iW626 is not able to send the OVP signal to the iW1780, the iW1780 has a

built-in protection scheme to detect the communication channel failures and go to the default 5V state.

Although there is no pin available to directly sense the input voltage, the iW1780 uses an innovative proprietary digital control method to detect and analyze the switch ON time, which provides real-time indirect sensing and monitoring of the magnitude and shape of the DC bulk capacitor voltage. This enables the iW1780 to determine and distinguish various conditions of the AC input voltage such as brown-out, brown-in and unplug, and to take appropriate actions. When the AC input voltage drops to a below normal operation range and the power supply input is still connected to the AC source, the iW1780 initiates a brown-out protection and shuts down the power supply adaptively according to the power supply load condition. Meanwhile, a brown-in input voltage threshold is set with hysteresis. In the case of the power supply input being unplugged or disconnected from the AC source, the iW1780 continues to control the switching actions to discharge the DC bulk capacitor voltage to a safe level before shutting down the power supply.

Also, the iW1780 monitors the voltage on the V_{CC} pin, and the IC shuts down immediately when the voltage on this pin is below the UVLO threshold. The iW1780 also has a V_{CC} over-voltage protection (V_{CC} OVP). During an abnormal event, if the V_{CC} voltage is higher than the protection threshold, the switching is stopped and the iW1780 shuts down.

When any of these faults are met the IC remains biased to discharge the V_{CC} supply. Once the V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues to attempt a start-up until the fault condition is removed. The V_{SENSE}-based OVP is implemented as auto-restart or latched mode, depending on the production options. The iW626-based OVP and V_{CC} OVP are auto-restart only. For the latched OVP version, the controller can only start up when the fault is removed and input is unplugged from AC mains to allow V_{CC} to drop to 2.0V below the UVLO threshold.

9.12 PCL, Switching Cycle, OCP, and SRS Protection

The peak-current limit (PCL), switching cycle, over-current protection (OCP) and sense-resistor-short protection (SRSP) are features built into the iW1780. With the CS/CDC pin the iW1780 is able to monitor the peak primary current. This allows for a cycle-by-cycle peak current control and limit. Once an abnormal condition occurs where the peak primary current multiplied by the current sense resistor is greater than 1.15V, a switching cycle over-current is detected and the IC immediately turns off the gate driver until the next cycle. The output driver sends out a switching pulse in the next cycle, and the switching pulse continues if the OCP threshold is not reached; or, the switching pulse turns off again if the OCP threshold is reached. If the OCP occurs for several consecutive switching cycles, the iW1780 shuts down.

If the current sense resistor is shorted prior to the power supply startup there is a potential danger that an over-current condition may not be detected. Thus, the IC is designed to detect this sense-resistor-short fault before start-up and the startup process is not pursued if the fault exists. The V_{CC} is discharged since the IC remains biased. Once V_{CC} drops below the UVLO threshold, the controller resets itself and then initiates a new soft-start cycle. The controller continues attempting to start up, but does not fully start up until the fault condition is removed.

9.13 CDC Configuration

The iW1780 incorporates an innovative approach to allow users to configure cable drop compensation (CDC) externally. This configuration is only performed once. It is completed after the initial OTP check but before the soft-start commences. During the CDC configuration, the internal digital control block senses the external resistance value between the CS/CDC pin and ground, and then sets a corresponding CDC level to allow the device to compensate for IR drop in the secondary circuitry during normal operation.

Figure 3.1 shows a simple circuit to set CDC level by connecting a resistor, R_{CDC}, immediately to the CS/CDC pin. This resistor should not be installed too close to the power MOSFET drain to avoid switching noise being coupled to the I_{SENSE} signal The iW1780 provides five levels of CDC configurations: 0, 75mV, 150mV, 300mV, and 450mV. Table 9.1 on the following page shows the resistance range for each of the five CDC levels. In practice, it is recommended to select resistance in the middle of the range wherever possible.

The “Cable Comp” specified in Table 9.1 refers to the voltage increment at the PCB end from no-load to full-load conditions in the CV mode, with the assumption that the secondary diode voltage drop can be ignored at the point when the secondary voltage is sensed. Also, the “Cable Comp” is specified based on the CC limit of 5V output and is independent of output voltage. For output voltages of 9V/12V, the actual voltage increment can be the same or lower depending on the CC limit setting. For example, CDC at 9V and 12V output are 80% and 50% of the “Cable Comp” specified in Table 9.1, if iW626-01 is paired with the iW1780 with CC limit coefficients k=0.5/0.411/0.322 for 5V/9V/12V V_{OUT}. Another example: CDC at 9V and 12V output are 100% and 80% of the “Cable Comp” specified in Table 9.1, if

iW626-04 is paired with the iW1780 with CC limit coefficients k=0.411/0.411/0.322 for 5V/9V/12V V_{OUT}.

To calculate the amount of cable compensation needed, take the resistance of the cable and connector and multiply it by the maximum output current.

9.14 External OTP

The iW1780 can be configured to provide external OTP by connecting a Negative-Temperature-Coefficient (NTC) resistor from the SD pin to GND. Internally, a 100µA current source is injected to the SD pin, which generates a voltage proportional to the NTC resistance. At high ambient temperature, the NTC resistance becomes low, which results in a low voltage at the SD pin. If the SD pin voltage drops below an internally-set threshold, then the OTP is triggered, and the iW1780 shuts down.

In the iW1780, the external OTP has a built-in hysteresis by having two thresholds. Before start-up, the OTP is triggered if the SD pin voltage is less than 1.2V; otherwise the device begins the CDC configuration (See Section 9.13), which is then followed by a normal soft-start process. During normal operation, the OTP threshold is switched to 1.0V, and the device only shuts down when the SD pin voltage is less than 1.0V.

9.15 Latch and Release

In the iW1780, both OTP and V_{SENSE}-based OVP can be latched whereby the iW1780 does not attempt to start again even with the fault cleared. In the latch state, the controller recycles itself by periodically ramping the V_{CC} up and down between the $V_{CC(ST)}$ and $V_{CC(UVL)}$, and the controller does not start up, if the input stays connected to the AC source. To get out of the latch state, unplugging the input from the AC source is required, so that the V_{CC} is allowed to drop to 2.0V below $V_{CC(UVL)}$ to release the latch.

For a fast release, the V_{CC} capacitor can be charged directly from the AC source before the diode-bridge rectifier instead of the bulk capacitor. In this way, when the input is unplugged, the V_{CC} capacitor is immediately cut off from the bulk capacitor, allowing for much faster discharging to release the latch, and initiate a normal start-up thereafter.

9.16 Internal OTP

The iW1780 features an internal OTP which shuts down the device if the internal die junction temperature reaches above T_{SD}. The device is kept off until the junction temperature drops below T_{SD-R}, when the device initiates a new soft-start process to build up the output voltage.

9.17 SmartDefender™ Smart Hiccup Technology

In the traditional AC/DC adapter designs, once the control IC detects a fault and shuts down, there are two common ways to respond to a default:

(a) Shutdown and auto-restart—The switching pulses are sent out in every power-on-reset (POR) cycle after V_{CC} reaches the startup threshold. In case of the USB cable short or partial short, this can have a high average output current from the USB and high average input power in the adapter, it may generate excessive heat and cause damages. The auto-restart is commonly called “hiccup”.

(b) Shutdown and latch—This normally requires the users to unplug the adapter from the AC input and recycle the power, which can create an inconvenient or bad experience.

To address this issue, the iW1780 implements a Dialog’s innovative and proprietary SmartDefender smart hiccup protection function. With SmartDefender technology, during the smart hiccup, the power supply only re-starts after a certain number of POR cycles (which means sending the switching pulses after V_{CC} reaches the startup threshold) instead of auto-restart in every POR cycle. In the iW1780 the SmartDefender function applies to the faults including output short and “CC shutdown,” etc. Once these faults are detected, the iW1780 allows 2 cycles of auto-restart POR,

CDC Level	1	2	3	4	5
R_{CDC} Range (kΩ)	0 – 2.20	2.37 – 3.21	3.40 – 4.64	4.87 – 6.65	6.98 – 8.25
Cable comp (mV)	0	75	150	300	450
V_{SENSE}-based OVP Threshold at 5V setting (V)	1.838	1.861	1.884	1.930	1.976

Table 9.1: Recommended resistance range and corresponding CDC levels for 5V output

and then block the next 6 cycles of auto-restart POR. This is equivalent to a 2/6 duty cycle. This operation mode continues until the faults are removed. In this way the SmartDefender technology effectively reduces the average output power at the fault conditions without latch.

9.18 Design Considerations

This section provides some design considerations for the iW1780.

IC V_{CC} Supply

Most Rapid Charge applications support multiple output voltages ranging from 5V to 12V and V_{CC} voltage is usually supplied from an auxiliary winding during normal operation. While V_{CC} should be above UVLO with sufficient margin at 5V output, V_{CC} can exceed its maximum operating voltage of 20V at 12V output depending on the transformer design. A simple LDO circuit with a transitor or MOSFET should be used to limit V_{CC} within its normal operating voltage range. (See Figure 9.5)

Multi-Level Output Voltage Setting

The default 5V output voltage setting is still determined by the transformer secondary-to-auxiliary winding turns ratio and the external voltage divider connected to the V_{SENSE} pin. Once the 5V default output is set correctly, 9V and 12V output voltage regulation is guaranteed by an internal circuit and digital controller automatically.

Output Current Limit Setting

The output CC limit setting is determined by Equation 9.6. Once the iW626 product option, transformer turns ratio, and current sense resistor are determined, the CC limits for 5V/9V/12V are all set.

Slow Opto-Coupler On-Off Speed Acceleration for Secondary-Based OVP Signal

To ensure a reliable secondary-based OVP signal is sent through the opto-coupler and to improve the switching speed of certain slow opto-couplers, an opto-coupler acceleration circuit with a resistor between V_{CC} and the opto-coupler collector, and a diode between the DLNK pin and opto-coupler collector is recommended as shown in Figure 9.5.

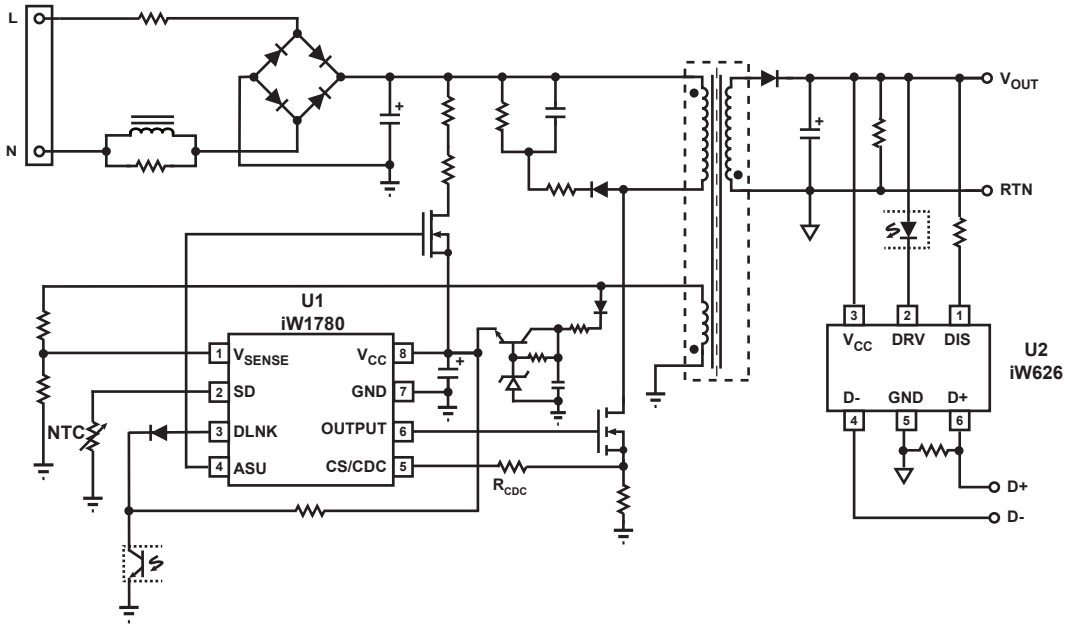
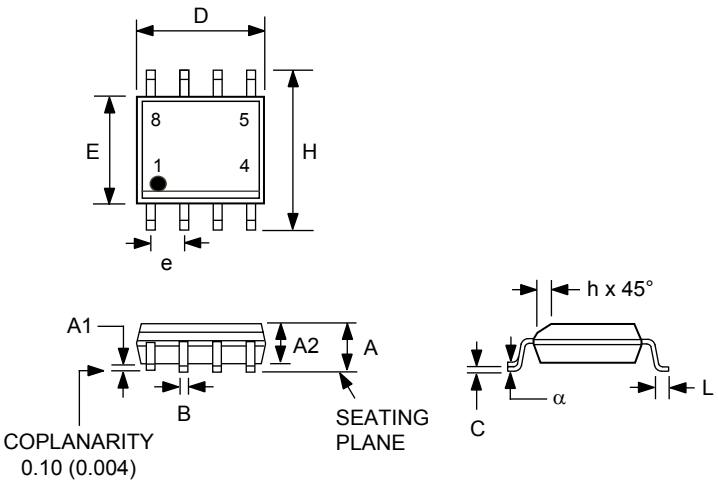


Figure 9.5: Typical Application Circuit with V_{CC} LDO and Opto-Coupler Acceleration

10.0 Physical Dimensions

8-Lead Small Outline (SOIC) Package



Symbol	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.0040	0.010	0.10	0.25
A2	0.049	0.059	1.25	1.50
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
h	0.10	0.020	0.25	0.50
L	0.016	0.049	0.4	1.25
α	0°	8°		

Compliant to JEDEC Standard MS12F

Controlling dimensions are in inches; millimeter dimensions are for reference only

This product is RoHS compliant and Halide free.

Soldering Temperature Resistance:

[a] Package is IPC/JEDEC Std 020D moisture sensitivity level 1

[b] Package exceeds JEDEC Std No. 22-A111 for solder immersion resistance; package can withstand 10 s immersion < 260˚C

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 mm per side.

The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.

11.0 Ordering Information

Part Number	Options	Package	Description
iW1780-00	For applications with same CC limit for 5V/9V, 3V CC shutdown voltage[1] for 5V V_{OUT}, paired with iW626-02/04	SOIC-8	Tape & Reel[2]
iW1780-01	For applications with different CC limits for 5V/9V, 3V CC shutdown voltage for 5V V_{OUT}, smart hiccup with 2/6 duty cycle, paired with iW626-00	SOIC-8	Tape & Reel[2]
iW1780-03	For applications with different CC limits for 5V/9V, 3V CC shutdown voltage for 5V V_{OUT}, smart hiccup with 2/6 duty cycle, optimized for Schottky diode output rectification, paired with iW626-00	SOIC-8	Tape & Reel[2]
iW1780-04	For applications with same CC limit for 5V/9V, 2.7V CC shutdown voltage for all V_{OUT}, paired with iW626-02/04	SOIC-8	Tape & Reel[2]
iW1780-07	For applications with same CC limit for 5V/9V, 3.5V CC shutdown voltage for 5V V_{OUT}, paired with iW626-02/04	SOIC-8	Tape & Reel[2]

Note 1: Unless specified, the default CC shutdown voltages are 6.5V for 9V V_{OUT} and 10V for 12V V_{OUT}.
Note 2: Tape & Reel packing quantity is 2,500/reel. Minimum ordering quantity is 2,500.

Rapid Charge™ AC/DC Digital Quasi-Resonant PWM Controller

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