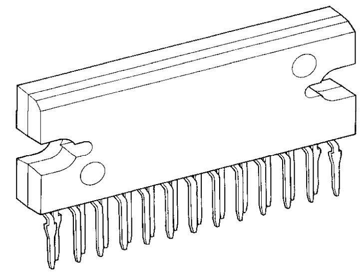
TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA8435H

PWM CHOPPER TYPE BIPOLAR STEPPING MOTOR DRIVER.

The TA8435H is PWM chopper type sinusoidal micro step bipolar stepping motor driver.
Sinusoidal micro step operation is accomplished only a clock signal inputting by means of built-in hard ware.



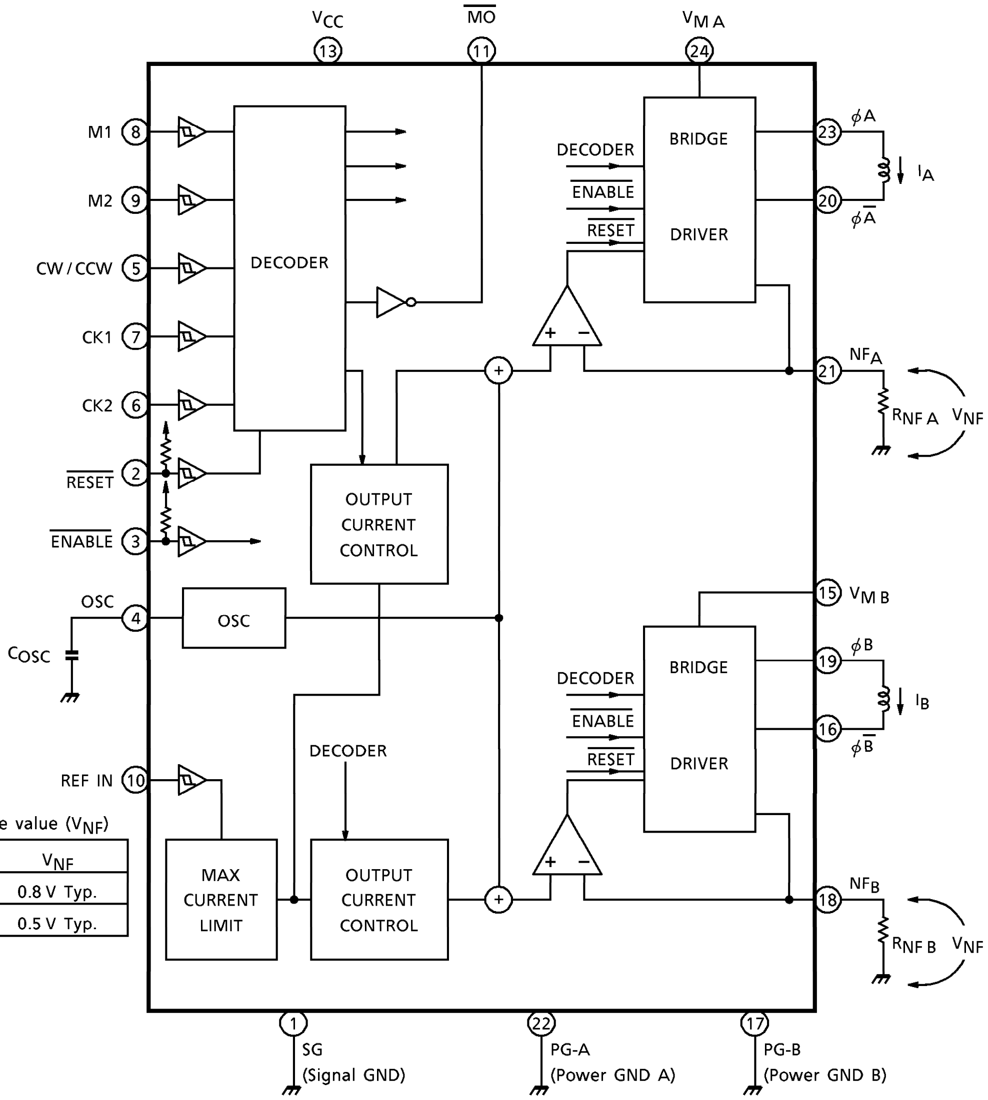
HZIP25-P-1.27

Weight : 9.86 g (Typ.)

FEATURES

- 1 chip bipolar sinusoidal micro step stepping motor driver.
- Output current up to 1.5 A (AVE.) and 2.5 A (PEAK).
- PWM chopper type.
- Structured by high voltage Bi-CMOS process technology.
- Forward and reverse rotation are available.
- 2, 1-2, W1-2, 2W1-2 phase 1 or 2 clock drives are selectable.
- Package : HZIP25-P
- Input Pull-up Resistor equipped with $\overline{\text{RESET}}$ Terminal : R = 100 kΩ (Typ.)
- Output Monitor available with $\overline{\text{MO}}$. $I_{O\,(\overline{MO})}$ = ±2 mA (MAX.)
- Reset and Enable are available with $\overline{\text{RESET}}$ and $\overline{\text{ENABLE}}$.

BLOCK DIAGRAM

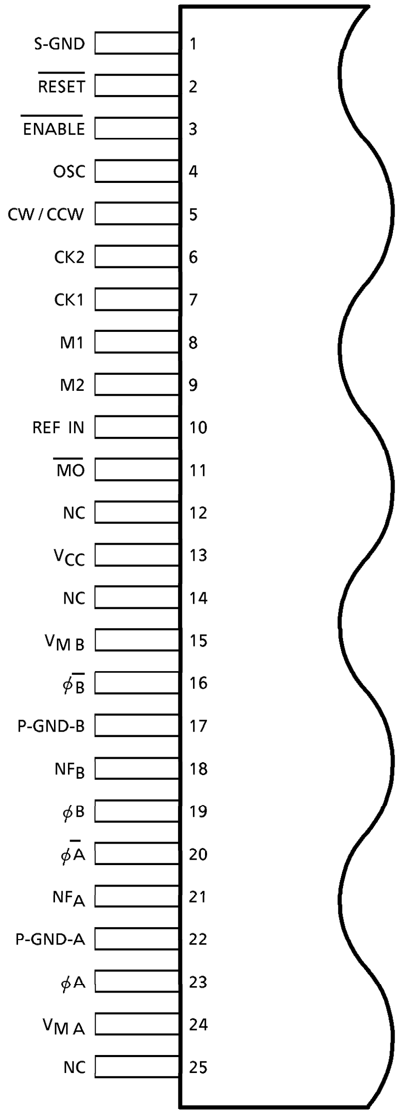


Output reference value (V_{NF})

REF IN	V_{NF}
H	0.8 V Typ.
L	0.5 V Typ.

Pull-up resistance : 100 kΩ (Typ.)
Pin⑫、⑭、㉕ : Non connection

PIN CONNECTION (Top view)

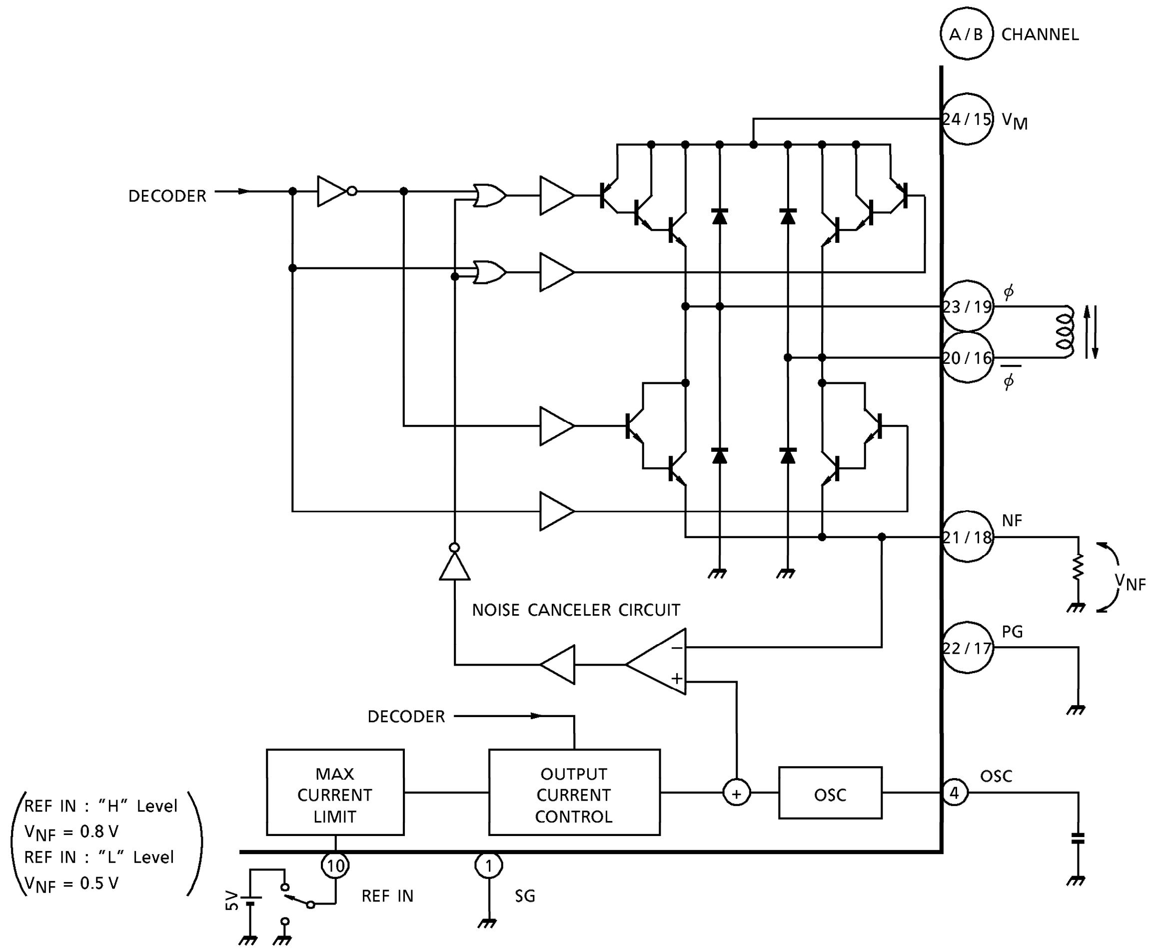


(Note) : NC : No connection

PIN FUNCTION

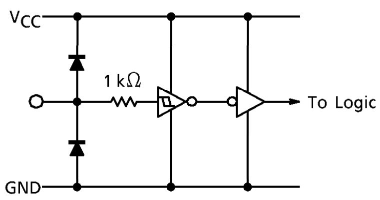
PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION
1	SG	Signal GND.
2	$\overline{\text{RESET}}$	L : RESET.
3	$\overline{\text{ENABLE}}$	L : ENABLE, H : OFF.
4	OSC	Chopping oscillation is determined by the external capacitor.
5	CW / CCW	Forward / Reverse switching terminal.
6	CK2	Clock input terminal.
7	CK1	Clock input terminal.
8	M1	Excitation control input
9	M2	Excitation control input
10	REF IN	V_{NF} control input
11	$\overline{\text{MO}}$	Monitor output
12	NC	No connection.
13	V_{CC}	Voltage supply for logic.
14	NC	No connection.
15	$V_{M\ B}$	Output power supply terminal.
16	$\phi\overline{B}$	Output $\phi\overline{B}$
17	PG-B	Power GND.
18	NF_B	B-ch output current detection terminal.
19	ϕB	Output ϕB
20	$\phi\overline{A}$	Output $\phi\overline{A}$
21	NF_A	A-ch output current detection terminal.
22	PG-A	Power GND
23	ϕA	Output ϕA
24	V_{MA}	Output power supply terminal.
25	NC	No connection.

OUTPUT CIRCUIT

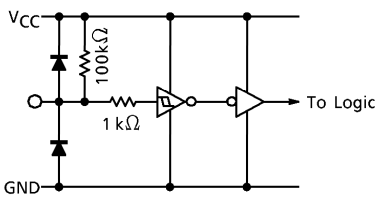


INPUT CIRCUIT

- CK1, CK2, CW / CCW, M1, M2, REF IN : Terminals

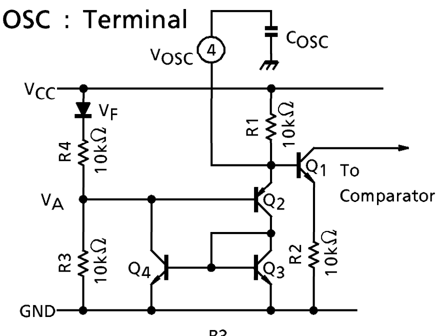


- $\overline{\text{RESET}}$, $\overline{\text{ENABLE}}$: Terminals



100 kΩ of Pull-up Resister is equipped.

- OSC : Terminal



$$V_A = (V_{CC} - V_F)\frac{R3}{R3 + R4} \fallingdotseq 2.15\ \text{V}$$

OSC FREQUENCY CALCULATION

Sawtooth OSC circuit consists of Q_1 through Q_4 and R1 through R4.
Q_2 is turned "off" when V_{OSC} is less than the voltage of 2.5 V + V_{BE} Q_2 approximately equal to 2.85 V.
V_{OSC} is increased by C_{OSC} charging through R1.
Q_3 and Q_4 are turned "on" when V_{OSC} becomes 2.85 V (Higher level.)
Lower level of V ④ pin is equal to V_{BE} Q_2 + V_{SAT} Q_4 approximately equal to 1.4 V.
V_{OSC} is calculated by following equation.

$$V_{OSC} = 5 \cdot \left[1 - \exp\left(- \frac{t}{C_{OSC} \cdot R1}\right) \right] \quad \text{.........} \quad ①$$

Assuming that V_{OSC} = 1.4 V (t = t_1) and = 2.85 V (t = t_2)
C_{OSC} is external capacitance connected to pin④ and R1 is on-chip 10 kΩ resistor.
Therefore, OSC frequency is calculated as follows.

$$t_1 = -C_{OSC} \cdot R1 \cdot \ell n \left(1 - \frac{1.4}{5}\right) \quad \text{..................} \quad ②$$

$$t_2 = -C_{OSC} \cdot R1 \cdot \ell n \left(1 - \frac{2.85}{5}\right) \quad \text{.................} \quad ③$$

$$f_{OSC} = \frac{1}{t_2 - t_1} = \frac{1}{C_{OSC} \left(R1 \cdot \ell n \left(1 - \frac{1.4}{5}\right) - R1 \cdot \ell n \left(1 - \frac{2.85}{5}\right) \right)}$$

$$= \frac{1}{5.15 \cdot C_{OSC}} \text{ (kHz) } (C_{OSC} : \mu F)$$

$\overline{\text{ENABLE}}$ AND $\overline{\text{RESET}}$ FUNCTION AND $\overline{\text{MO}}$ SIGNAL

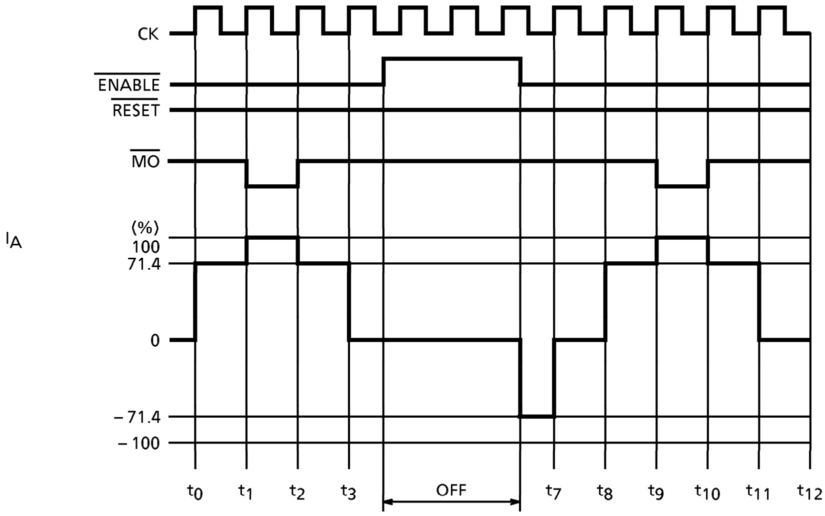


Fig.1 1-2 Phase drive mode (M1 : H, M2 : L)

$\overline{\text{ENABLE}}$ Signal disables only Output Signal.
Internal logic functions are proceeded by CK signal without regard to $\overline{\text{ENABLE}}$ signal.
Therefore, Output Current is initiated from the proceeded timing point of internal logic circuit after release of disable mode.
Fig.1 shows the $\overline{\text{ENABLE}}$ functions, when the system is selected in 1-2 Phase drive mode.

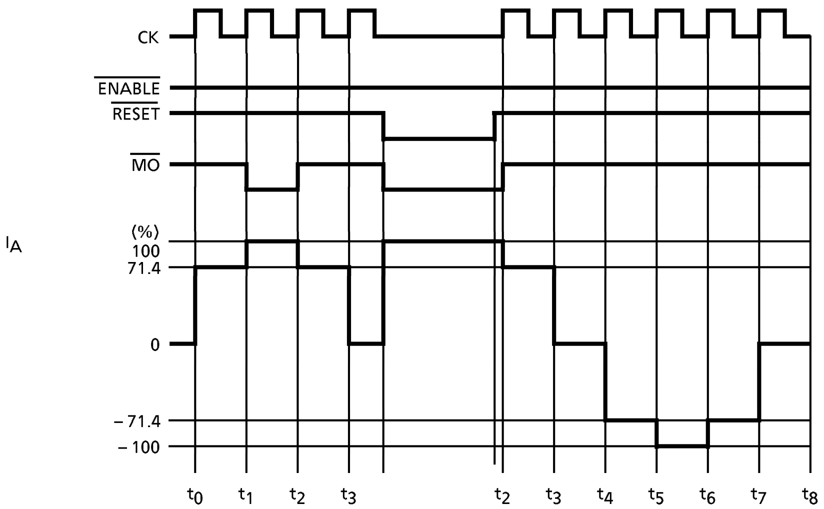


Fig.2 1-2 Phase drive mode (M1 : H, M2 : L)

Low level active of $\overline{\text{RESET}}$ Signal offs not only the Outputs but also stops internal CK functions and $\overline{\text{MO}}$ to low.
Outputs are initiated from the initial point after release of $\overline{\text{RESET}}$ (High) as shown in Fig.2.
$\overline{\text{MO}}$ (Monitor Output) Signals can be used as rotation and initial signal for stable rotation checking.

FUNCTION

INPUT					MODE
CK1	CK2	CW / CCW	$\overline{\text{RESET}}$	$\overline{\text{ENABLE}}$	
↑	H	L	H	L	CW
⎍	L	L	H	L	INHIBIT (Note)
H	↑	L	H	L	CCW
L	⎍	L	H	L	INHIBIT (Note)
↑	H	H	H	L	CCW
⎍	L	H	H	L	INHIBIT (Note)
H	↑	H	H	L	CW
L	⎍	H	H	L	INHIBIT (Note)
X	X	X	L	L	RESET
X	X	X	X	H	Z

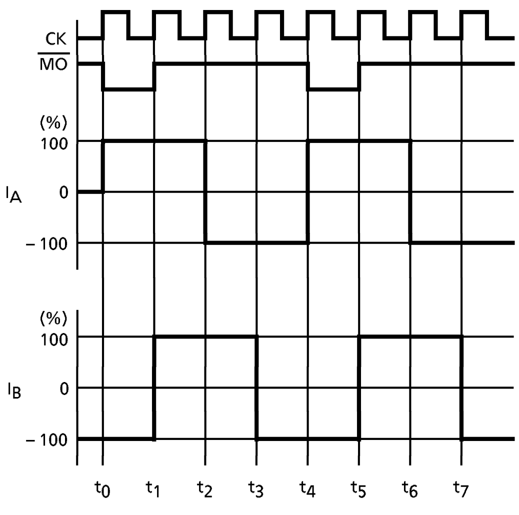
INITIAL MODE

EXCITATION MODE	A PHASE CURRENT	B PHASE CURRENT
2 Phase	100%	− 100%
1-2 Phase	100%	0%
W1-2 Phase	100%	0%
2W1-2 Phase	100%	0%

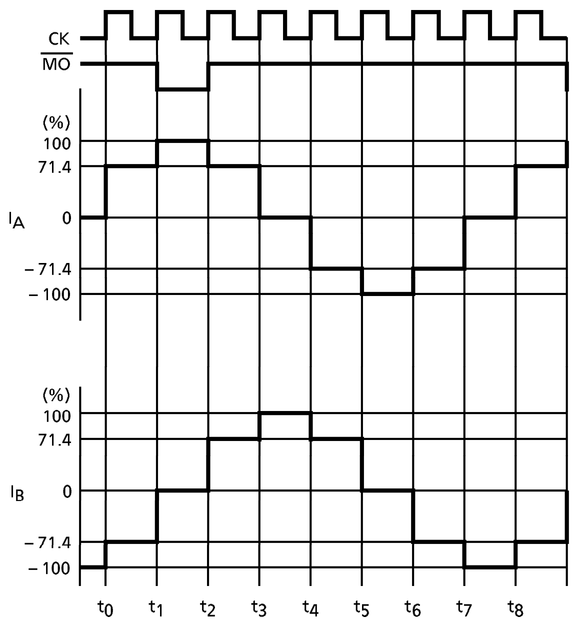
Z : High impedance
X : Don't Care

INPUT		MODE (EXCITATION)
M1	M2	
L	L	2 Phase
H	L	1-2 Phase
L	H	W1-2 Phase
H	H	2W1-2 Phase

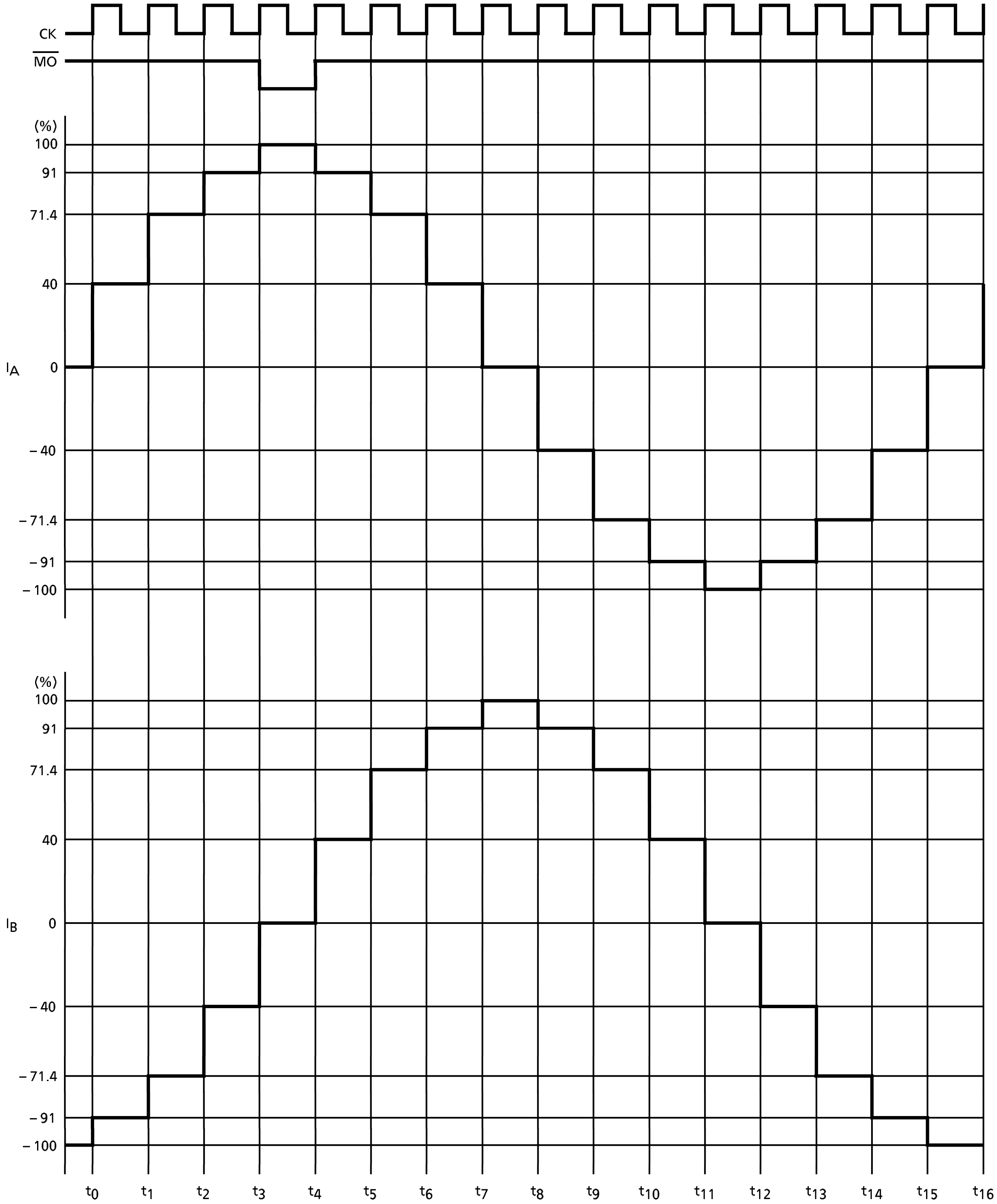
2 PHASE EXCITATION (M1 : L, M2 : L, CW MODE)



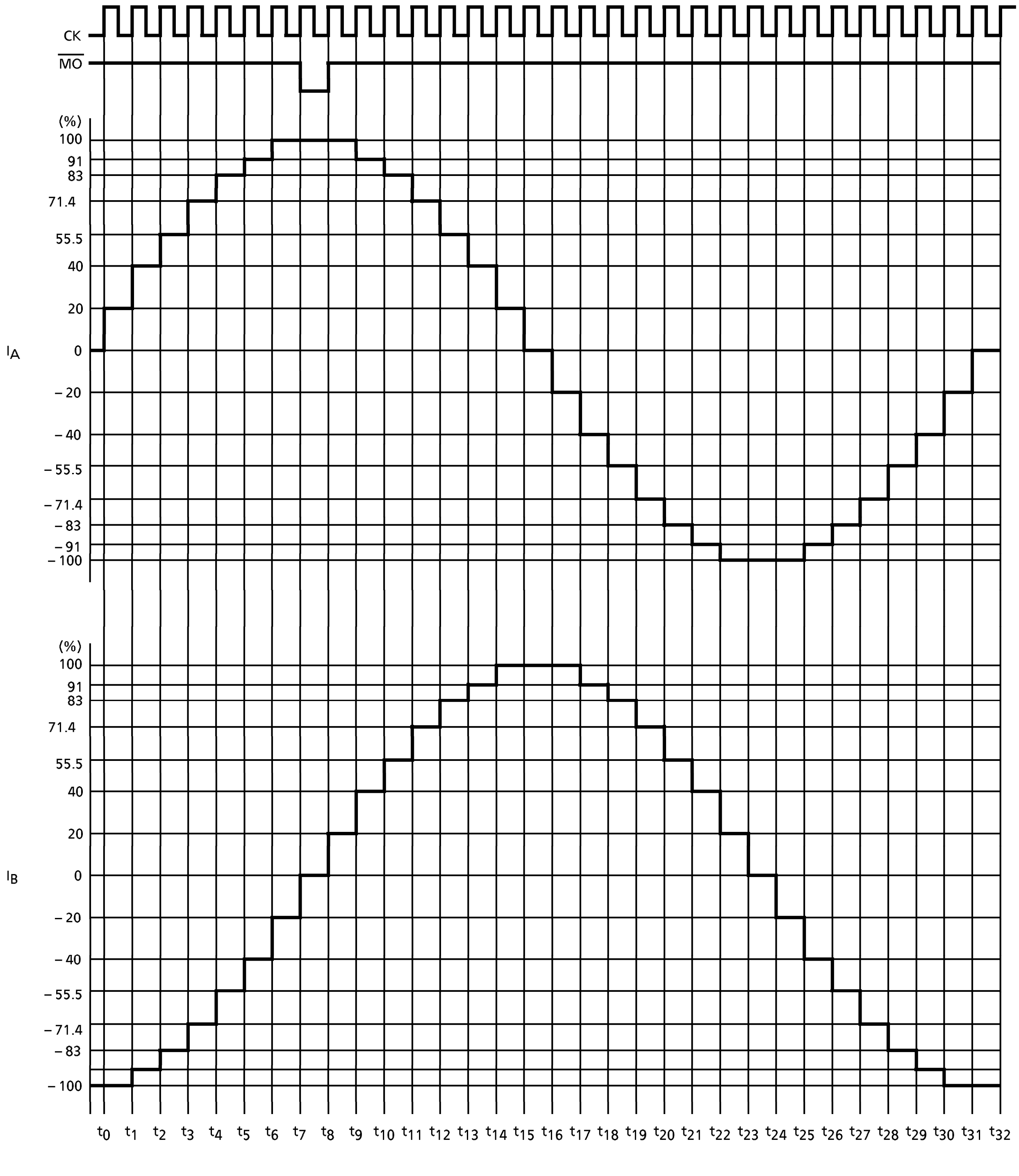
1-2 PHASE EXCITATION (M1 : H, M2 : L, CW MODE)



W1-2 PHASE EXCITATION (M1 : L, M2 : H, CW MODE)



2W1-2 PHASE EXCITATION (M1 : H, M2 : H, CW MODE)



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	5.5	V
Output Voltage		V_M	40	V
Output Current	PEAK	$I_{O\,(PEAK)}$	2.5	A
	AVE.	$I_{O\,(AVE.)}$	1.5	
$\overline{MO}$ Output Current		$I_{O\,(\overline{MO})}$	±2	mA
Input Voltage		V_{IN}	~V_{CC}	V
Power Dissipation		P_D	5 (Note 1)	W
			43 (Note 2)	
Operating Temperature		T_{opr}	−40~85	°C
Storage Temperature		T_{stg}	−55~150	°C
Feed Back Voltage		V_{NF}	1.0	V

(Note 1) : No heat sink
(Note 2) : Tc = 85°C

RECOMMENDED OPERATING CONDITIONS (Ta = −20~75°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	—	4.5	5.0	5.5	V
Output Voltage	V_M	—	21.6	24	26.4	V
Output Current	I_{OUT}	—	—	—	1.5	A
Input Voltage	V_{IN}	—	—	—	V_{CC}	V
Clock Frequency	f_{CK}	—	—	—	5	kHz
OSC Frequency	f_{OSC}	—	15	—	80	kHz

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 5 V, V_M = 24 V)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Voltage	High	$V_{IN\,(H)}$	1	M1, M2, CW / CCW, REF IN $\overline{ENABLE}$, CK1, CK2 $\overline{RESET}$	3.5	—	V_{CC} + 0.4	V
	Low	$V_{IN\,(L)}$			GND − 0.4	—	1.5	
Input Hysteresis Voltage		V_H			—	600	—	mV
Input Current		$I_{IN\text{-}1\,(H)}$	1	M1, M2, REF IN, V_{IN} = 5.0 V	—	—	100	nA
		$I_{IN\text{-}1\,(L)}$		$\overline{RESET}$, $\overline{ENABLE}$, V_{IN} = 0 V, INTERNAL PULL-UP RESISTOR	10	50	100	μA
		$I_{IN\text{-}2\,(L)}$		SOURCE TYPE, V_{IN} = 0 V	—	—	100	nA
Quiescent Current V_{CC} Terminal		I_{CC1}	1	Output Open, $\overline{RESET}$: H, $\overline{ENABLE}$: L (2, 1-2 Phase excitation)	—	10	18	mA
		I_{CC2}		Output Open, $\overline{RESET}$: H, $\overline{ENABLE}$: L (W1-2, 2W1-2 Phase excitation)	—	10	18	
		I_{CC3}		$\overline{RESET}$: L, $\overline{ENABLE}$: H	—	5	—	
		I_{CC4}		$\overline{RESET}$: H, $\overline{ENABLE}$: H	—	5	—	
Comparator Reference Voltage	High	$V_{NF\,(H)}$	3	REF IN H Output Open (Note)	0.72	0.8	0.88	V
	Low	$V_{NF\,(L)}$		REF IN L Output Open (Note)	0.45	0.5	0.55	
Output Differential		ΔV_O	—	B / A, C_{OSC} = 0.0033 μF, R_{NF} = 0.8 Ω	− 10	—	10	%
$V_{NF\,(H)}$ − $V_{NF\,(L)}$		ΔV_{NF}	—	$V_{NF\,(L)}$ / $V_{NF\,(H)}$ C_{OSC} = 0.0033 μF, R_{NF} = 0.8 Ω	56	63	70	%
NF Terminal Current		I_{NF}	—	SOURCE TYPE	—	170	—	μA
Maximum OSC Frequency		$f_{OSC\,(MAX.)}$	—	—	100	—	—	kHz
Minimum OSC Frequency		$f_{OSC\,(MIN.)}$	—	—	—	—	10	kHz
OSC Frequency		f_{OSC}	—	C_{OSC} = 0.0033 μF	25	44	62	kHz
Minimum Clock Pulse Width		$t_{W\,(CK)}$	—	—	—	1.0	—	μs
Output Voltage		V_{OH} ($\overline{MO}$)	—	I_{OH} = − 40 μA	4.5	4.9	V_{CC}	V
		V_{OL} ($\overline{MO}$)		I_{OL} = 40 μA	GND	0.1	0.5	

(Note) : 2 Phase excitation, R_{NF} = 0.7 Ω, C_{OSC} = 0.0033 μF

OUTPUT BLOCK

CHARACTERISTIC				SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Output Saturation Voltage	Upper Side			$V_{SAT\ U1}$	4	I_{OUT} = 1.5 A		—	2.1	2.8	V
	Lower Side			$V_{SAT\ L1}$				—	1.3	2.0	
	Upper Side			$V_{SAT\ U2}$		I_{OUT} = 0.8 A		—	1.8	2.2	
	Lower Side			$V_{SAT\ L2}$				—	1.1	1.5	
	Upper Side			$V_{SAT\ U3}$		I_{OUT} = 2.5 A Pulse width 30 ms		—	2.5	3.0	
	Lower Side			$V_{SAT\ L3}$				—	1.8	2.2	
Diode Forward Voltage	Upper Side			$V_{F\ U1}$	5	I_{OUT} = 1.5 A		—	2.0	3.0	V
	Lower Side			$V_{F\ L1}$				—	1.5	2.1	
	Upper Side			$V_{F\ U2}$		I_{OUT} = 2.5 A Pulse width 30 ms		—	2.5	3.3	
	Lower Side			$V_{F\ L2}$				—	1.8	2.5	
Output Dark Current (A + B Channels)				I_{M1}	2	$\overline{\text{ENABLE}}$: "H" Level, Output Open $\overline{\text{RESET}}$: "L" Level		—	—	50	μA
				I_{M2}		$\overline{\text{ENABLE}}$: "L" Level Output Open $\overline{\text{RESET}}$: "H" Level		—	8	15	mA
A-B Chopping Current (Note)	2W1-2ϕ	W1-2ϕ	1-2ϕ	VECTOR	—	θ = 0	REF IN : H R_{NF} = 0.8 Ω C_{OSC} = 0.0033 μF	—	100	—	%
	2W1-2ϕ	—	—			θ = 1 / 8		—	100	—	
	2W1-2ϕ	W1-2ϕ	—			θ = 2 / 8		86	91	96	
	2W1-2ϕ	—	—			θ = 3 / 8		78	83	88	
	2W1-2ϕ	W1-2ϕ	1-2ϕ			θ = 4 / 8		66.4	71.4	76.4	
	2W1-2ϕ	—	—			θ = 5 / 8		50.5	55.5	60.5	
	2W1-2ϕ	W1-2ϕ	—			θ = 6 / 8		35	40	45	
	2W1-2ϕ	—	—			θ = 7 / 8		15	20	25	
	2 Phase Excitation Mode VECTOR					—		—	100	—	

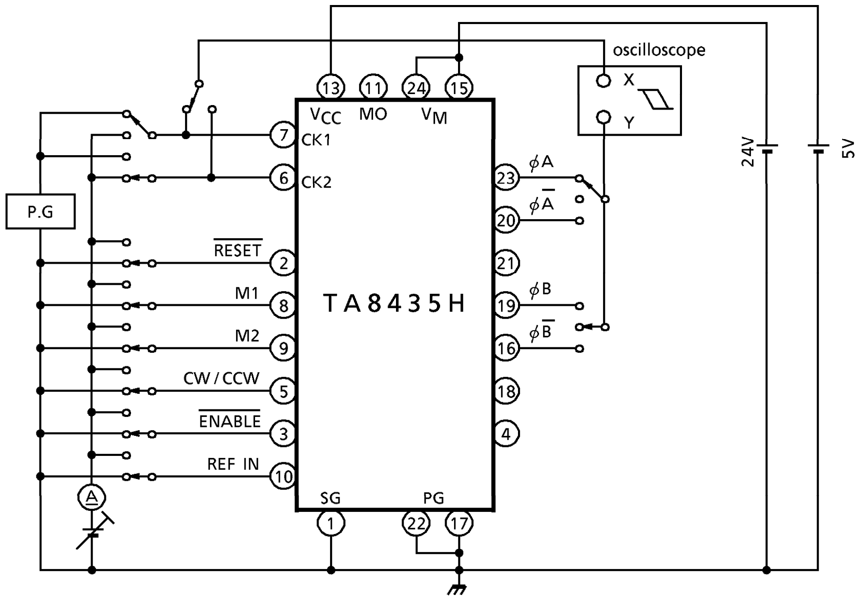
(Note) : Maximum current (θ = 0) : 100%
2W1-2ϕ : 2W1, 2 phase excitation mode
W1-2ϕ : W1, 2 phase excitation mode
1-2ϕ : 1, 2 phase excitation mode

CHARACTERISTIC				SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
A-B Chopping Current (Note)	2W1-2ϕ	W1-2ϕ	1-2ϕ	VECTOR	—	θ = 0	REF IN : L, R_{NF} = 0.8 Ω, C_{OSC} = 0.0033 μF	—	100	—	%
	2W1-2ϕ	—	—			θ = 1/8		—	100	—	
	2W1-2ϕ	W1-2ϕ	—			θ = 2/8		86	91	96	
	2W1-2ϕ	—	—			θ = 3/8		78	83	88	
	2W1-2ϕ	W1-2ϕ	1-2ϕ			θ = 4/8		66.4	71.4	76.4	
	2W1-2ϕ	—	—			θ = 5/8		50.5	55.5	60.5	
	2W1-2ϕ	W1-2ϕ	—			θ = 6/8		35	40	45	
	2W1-2ϕ	—	—			θ = 7/8		15	20	25	
	2 Phase Excitation Mode VECTOR					—		—	100	—	
Feed Back Voltage Step				ΔV_{NF}	—	$\Delta\theta$ = 0/8 − 1/8	REF IN : H, R_{NF} = 0.8 Ω, C_{OSC} = 0.0033 μF	—	0	—	mV
						$\Delta\theta$ = 1/8 − 2/8		32	72	112	
						$\Delta\theta$ = 2/8 − 3/8		24	64	104	
						$\Delta\theta$ = 3/8 − 4/8		53	93	133	
						$\Delta\theta$ = 4/8 − 5/8		87	127	167	
						$\Delta\theta$ = 5/8 − 6/8		84	124	164	
						$\Delta\theta$ = 6/8 − 7/8		120	160	200	
Output T_r Switching Characteristics				t_r	7	R_L = 2 Ω, V_{NF} = 0 V, C_L = 15 pF		—	0.3	—	μs
				t_f				—	2.2	—	
				t_{pLH}		CK~Output		—	1.5	—	
				t_{pHL}				—	2.7	—	
				t_{pLH}		OSC~Output		—	5.4	—	
				t_{pHL}				—	6.3	—	
				t_{pLH}		$\overline{\text{RESET}}$~Output		—	2.0	—	
				t_{pHL}				—	2.5	—	
				t_{pLH}		$\overline{\text{ENABLE}}$~Output		—	5.0	—	
				t_{pHL}				—	6.0	—	
Output Leakage Current	Upper Side			I_{OH}	6	V_M = 30 V		—	—	50	μA
	Lower Side			I_{OL}				—	—	50	

(Note) : Maximum current (θ = 0) : 100%
2W1-2ϕ : 2W1, 2 phase excitation mode
W1-2ϕ : W1, 2 phase excitation mode
1-2ϕ : 1, 2 phase excitation mode

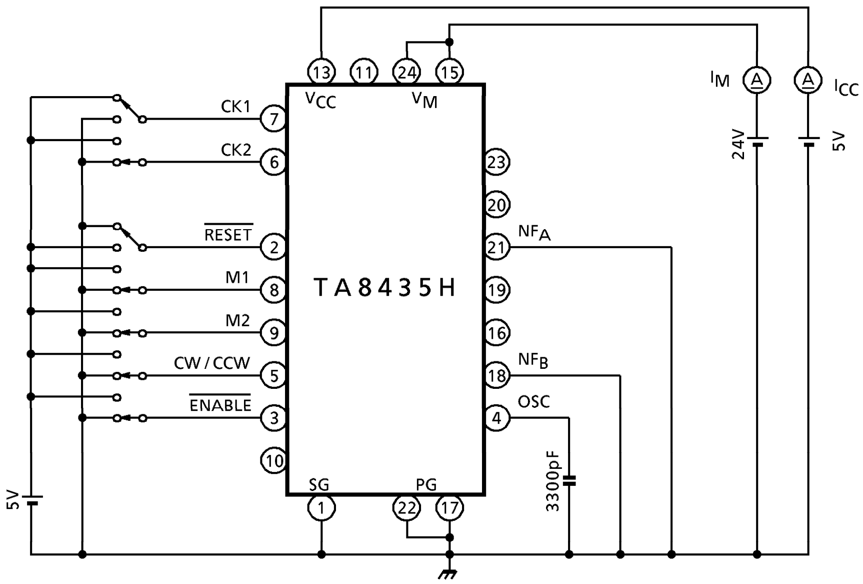
TEST CIRCUIT 1

$V_{IN (H)}$, (L), $I_{IN (H)}$, (L)



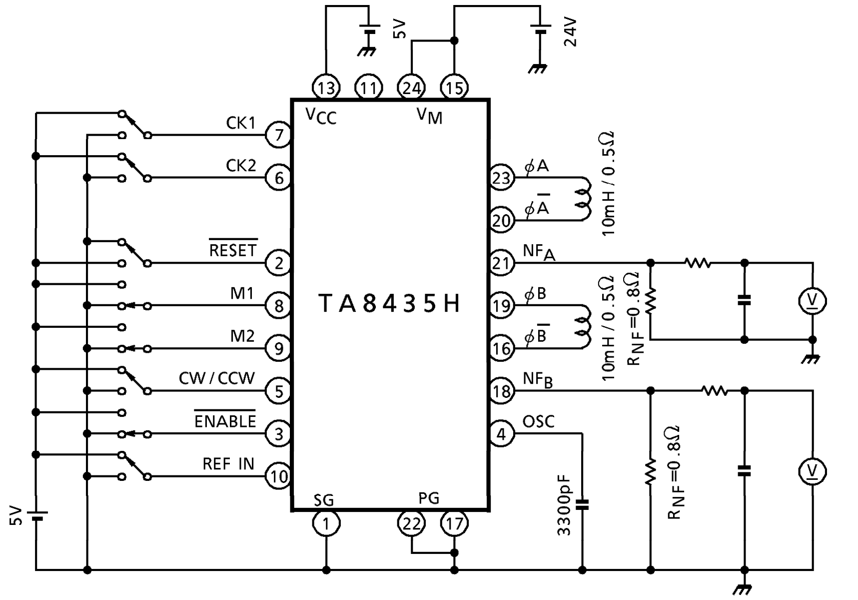
TEST CIRCUIT 2

I_{CC}, I_{M}



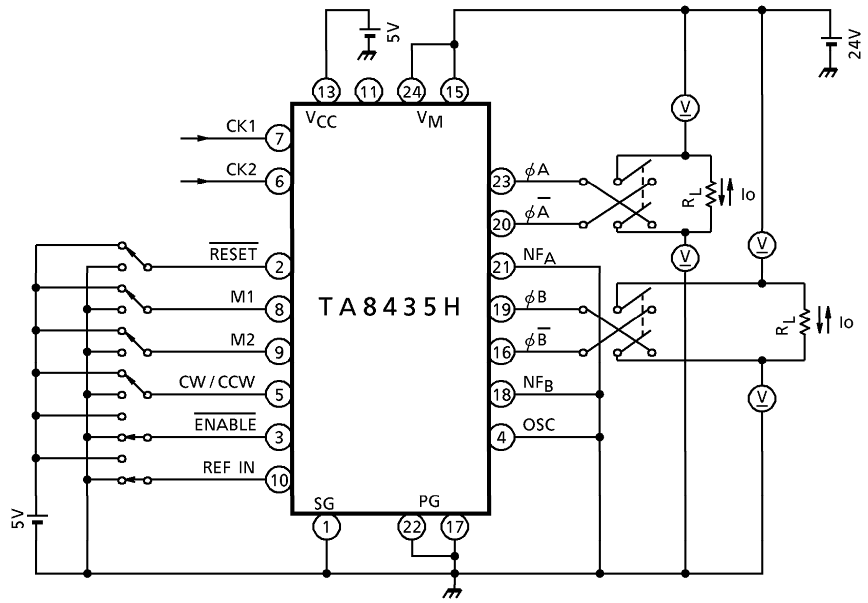
TEST CIRCUIT 3

$V_{NF\,(H)}$, (L)



TEST CIRCUIT 4

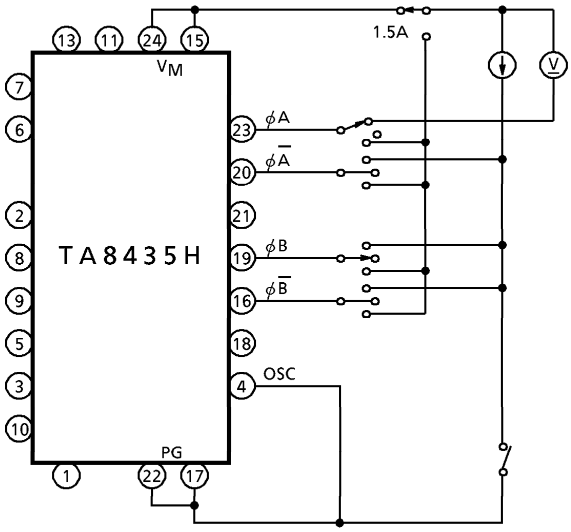
$V_{CE\,(SAT)}$ UPPER SIDE, LOWER SIDE



(Note) : Calibrate Io to 1.5 A / 0.8 A by R_L

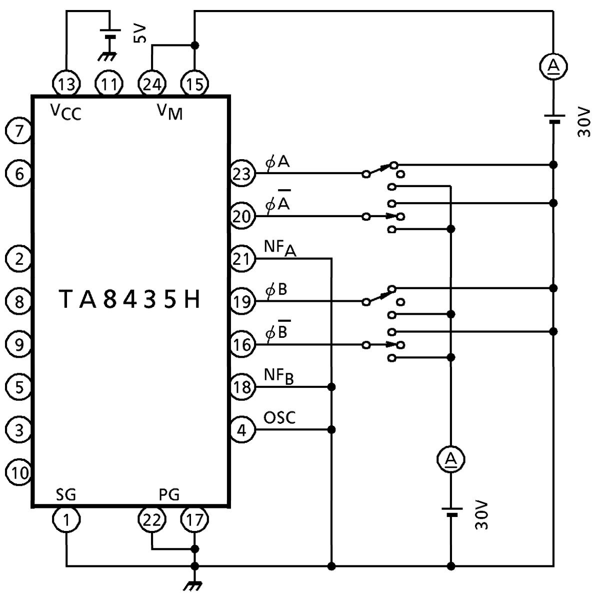
TEST CIRCUIT 5

V_{FU}, V_{FL}



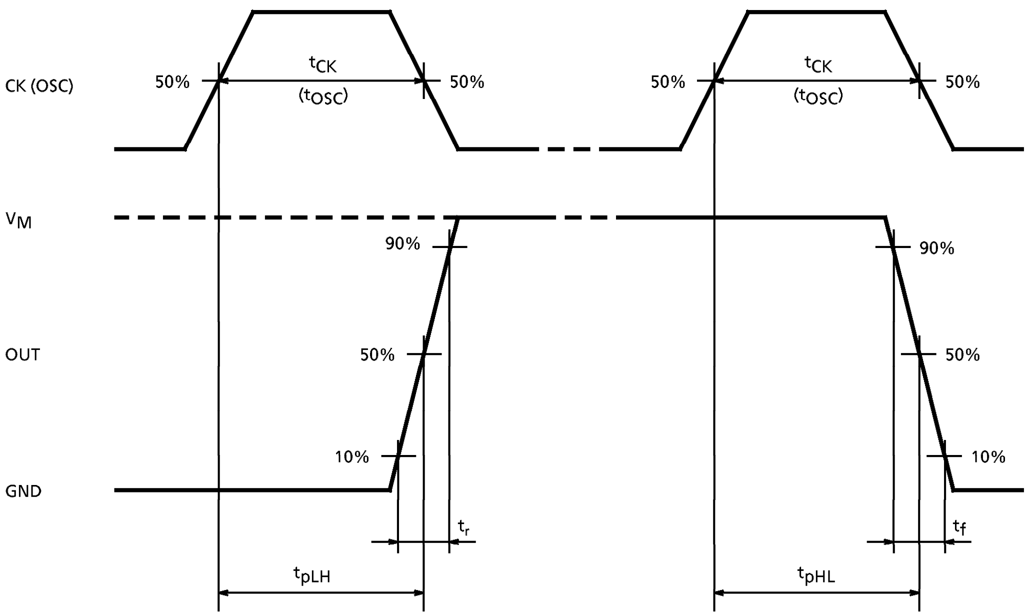
TEST CIRCUIT 6

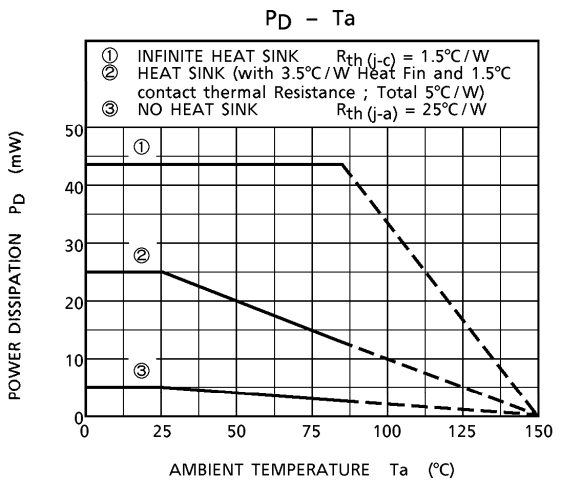
I_{OH}, I_{OL}

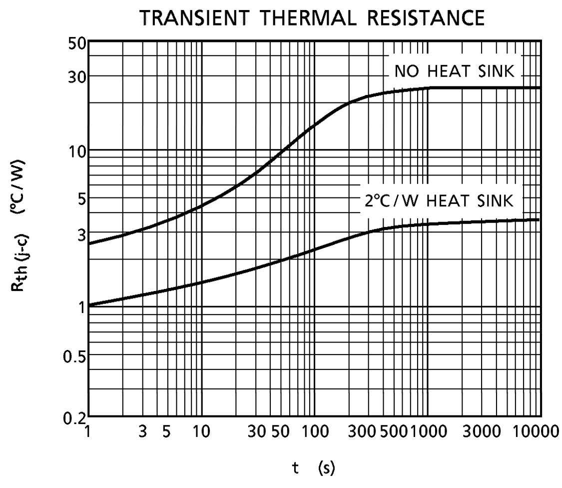


AC ELECTRICAL CHARACTERISTICS, MEASUREMENT WAVE

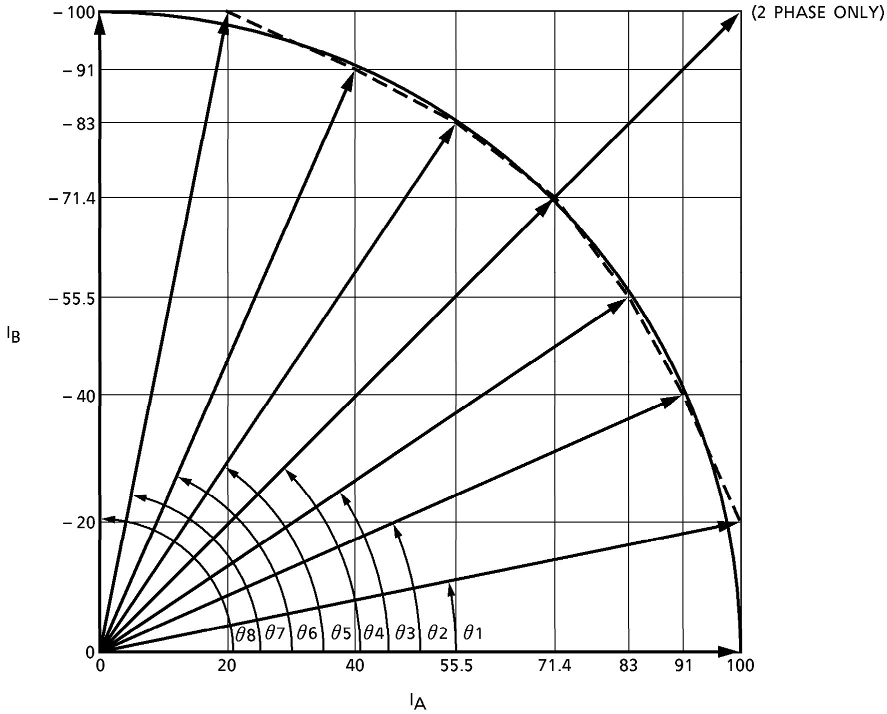
CK (OSC)-OUT





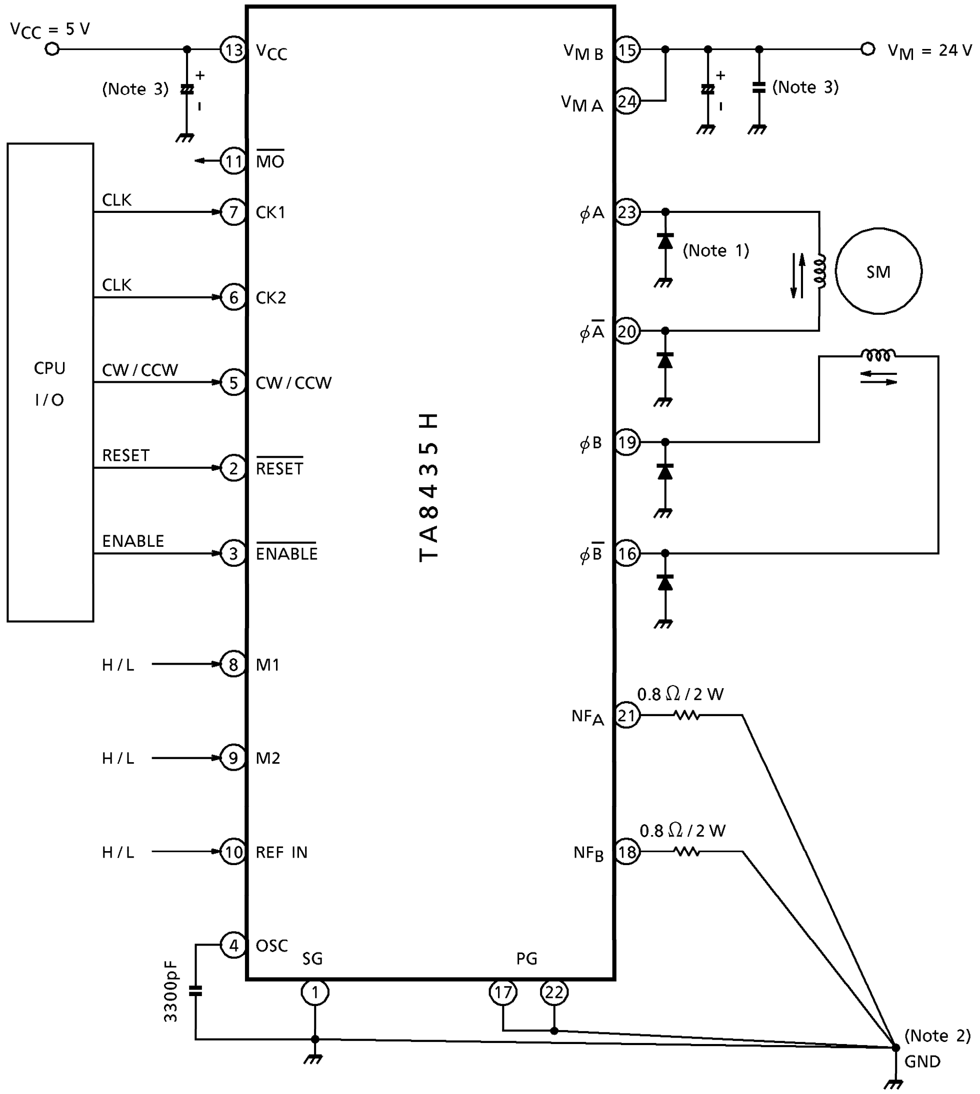


OUTPUT CURRENT VECTOR ORBIT (Normalize to 90° for each one step)



θ	ROTATION ANGLE		VECTOR LENGTH		
	IDEAL	TA8435H	IDEAL	TA8435H	
θ0	0°	0°	100	100.00	—
θ1	11.25°	11.31°	100	101.98	—
θ2	22.5°	23.73°	100	99.40	—
θ3	33.75°	33.77°	100	99.85	—
θ4	45°	45°	100	100.97	141.42
θ5	56.25°	56.23°	100	99.85	—
θ6	67.5°	66.27°	100	99.40	—
θ7	78.75°	78.69°	100	101.98	—
θ8	90°	90°	100	100.00	—
			1-2 / W1-2 / 2W1-2 Phase		2 Phase

APPLICATION CIRCUIT



(Note 1) : Schottky diode (3GWJ42) to be connected additionally between each output (pin 16 / 19 / 20 / 23) and GND for preventing Punch-Through Current

(Note 2) : GND pattern to be laid out at one point in order to prevent common impedance.

(Note 3) : Capacitor for noise suppression to be connected between the Power Supply (V_{CC}, V_M) and GND to stabilize the operation.

(Note 4) : Utmost care is necessary in the design of the output line, V_M and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

When using TA8435H

0. Introduction

   The TA8435H controls PWM to set the stepping motor winding current to constant current. The device is a micro-step driver IC used to efficiently drive the stepping motor at low vibration.

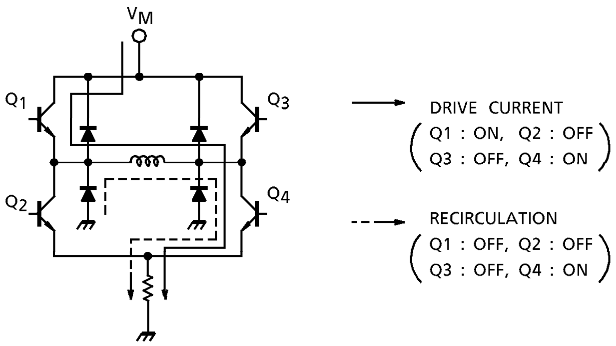
1. About micro-step drive

   The TA8435H drives a stepping motor in micro steps with a maximum resolution of 1 / 8 of the 2-phase stepping angle (in 2W1-2 phase mode).
   In micro steps, A-phase and B-phase current levels are set inside the IC so that the composite vector size and the rotation angle are even. Just inputting clock signals rotates the stepping motor in micro steps.

2. About PWM control and output current setting

   (1) Output current path (PWM control)

   The TA8435H controls PWM by turning the upper power transistor on / off.
   In such a case, current flows as shown in the figure below.



   (2) Setting of output current by REF-IN input and current detection resistor

   The motor current (maximum current for micro-step drive) I_O is set as shown in the following equation, using REF-IN input and the external current detection resistor R_{NF}.

$I_O = V_{REF} / R_{NF}$

where,

REF − IN = High, $V_{REF} = 0.8\ V$

REF − IN = Low, $V_{REF} = 0.5\ V$

3. Logic control

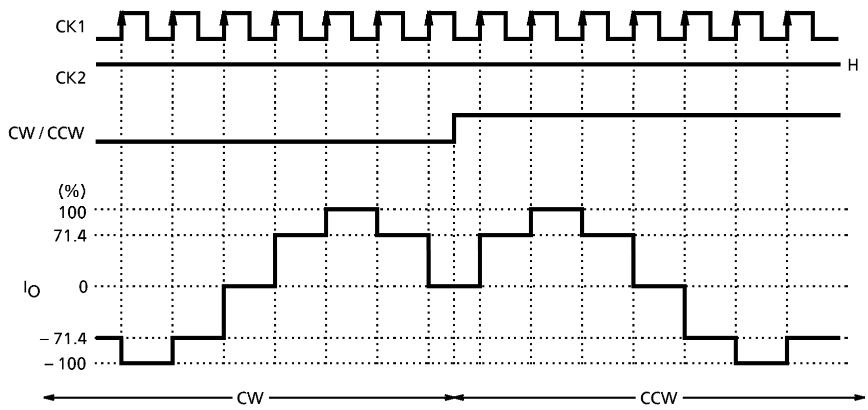
(1) Clock input for rotation direction control

To switch rotation between forward and reverse, there are two clock input types: 1-clock input and 2-clock input.

(a) 1-clock input

Uses either clock pin CK1 or CK2.
Switches rotation between forward or reverse using the CW or CCW signal.

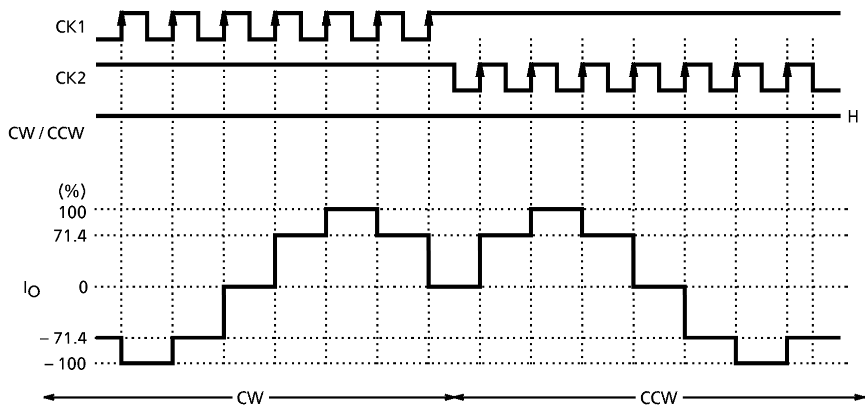
<Input signal example: 1-2 phase mode>



(b) 2-clock input

Uses both clock pins CK1 and CK2.
Switching between CK1 and CK2 controls forward / reverse rotation.

<Input signal example: 1-2 phase mode>



(2) Mode setting

Setting M1 and M2 selects one of the following modes: 2-phase, 1-2 phase, W1-2 phase, and 2W1-2 phase modes.

(3) Monitor ($\overline{MO}$) output

Supports the monitor output used to monitor the current waveform location.
For 2-phase mode, $\overline{MO}$ output is Low at the timing of A-phase current = 100% and B-phase current = −100%.
For 1-2 phase, W1-2 phase, or 2W1-2 phase mode, $\overline{MO}$ output is Low at the timing of A-phase current = 100% and B-phase current = 0%.

(4) Reset pin

Supports reset input used to reset the internal counter.
Setting RESET to Low resets the internal counter, forcing the output current to the same value as that when the $\overline{MO}$ output is Low.

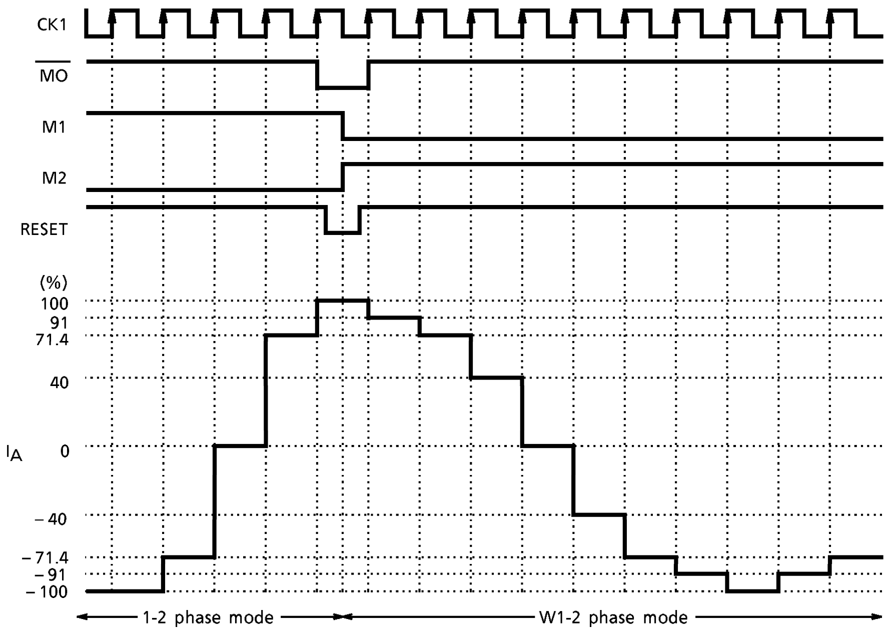
(5) Phase mode switching

To avoid the step changing during motor rotation, current must not fluctuate at phase mode switching. Pay attention to the following points.

(a) When switching between 2-phase and other phase modes, current fluctuates.

(b) When switching between phase modes other than 2-phase, current can be switched without fluctuation at the timing of $\overline{MO}$ output = Low.
However, when switching as follows, set RESET to Low beforehand:
From 1-2 phase to W1-2 phase or 2W1-2 phase mode
From W1-2 phase to 2W1-2 phase mode

<Example of Input Signal>



4. About PWM oscillation frequency (external capacitor setting)

   An external capacitor connected to the OSC pin is used to internally generate a sawtooth waveform. PWM is controlled using this frequency.
   Toshiba recommend 3300 pF for the capacitance by taking variation between ICs into consideration.

5. About external Schottky diode

   A parasitic diode is created on the lower side of the output. When PWM is controlled, current flows to the parasitic diode. This current results in a punch-through current and micro-step waveform fluctuation. Therefore, make sure to externally connect a Schottky barrier diode.
   The external diode can reduce heat generated in the IC.

6. Power dissipation

   The IC power dissipation is determined by the following equation (In a case where shottky diode is connected between Output pin and GND):

   $$P = V_{CC} \times I_{CC} + VM \times IM + I_O (t_{ON} \times V_{SAT}\text{-U} + V_{SAT}\text{-L})$$
   $$t_{ON} = T_{ON} / T_S \text{ (PWM control ON duty)}$$

   The higher the ambient temperature, the smaller the power dissipation.
   Check the P_D-Ta curve and design heat dissipation with a sufficient margin.

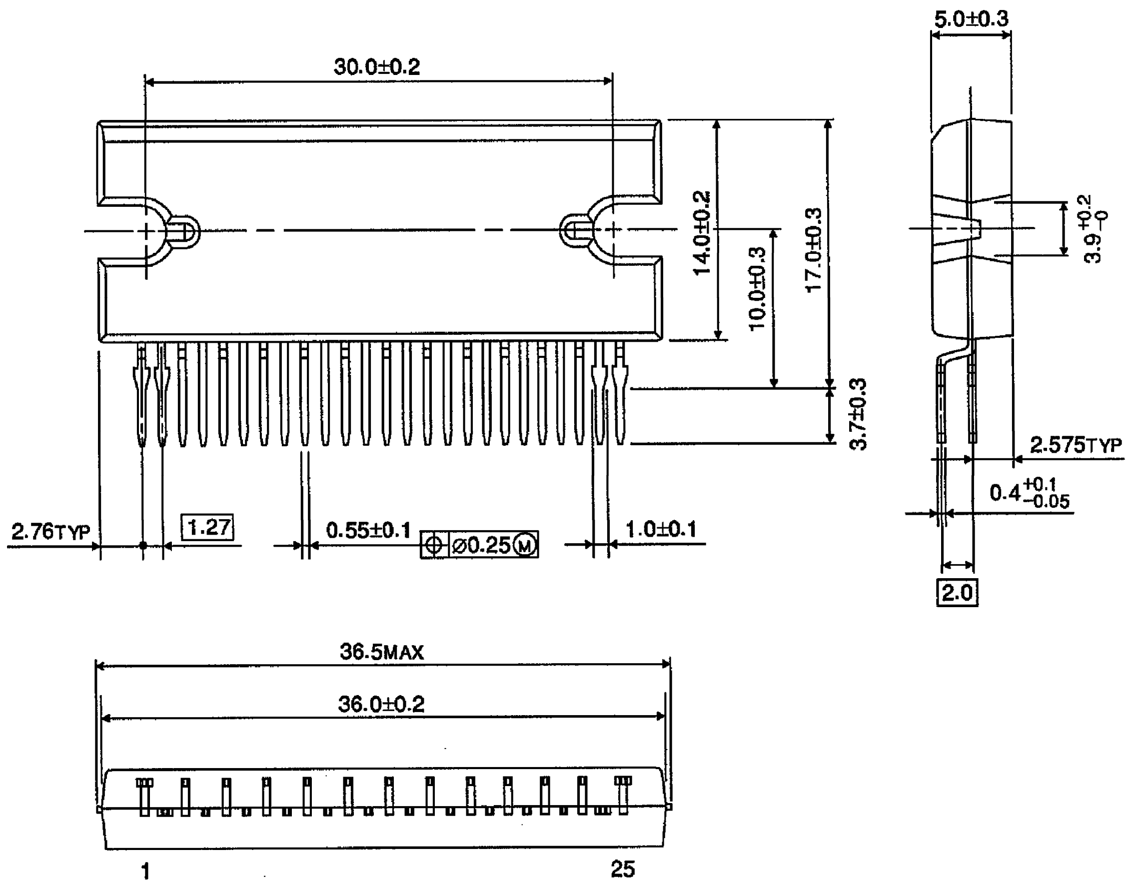
7. About heatsink fin processing

   The IC fin (rear) is electrically connected to the rear of the chip.
   When current flows to the fin, the IC malfunctions.
   If there is any possibility of a voltage being generated between the IC GND and the fin, either ground the fin or insulate it.

OUTLINE DRAWING

HZIP25-P-1.27

Unit : mm



Weight : 9.86 g (Typ.)