A13 Datasheet

V1.12

2012.3.29

Revision History

Version	Date	Section/ Page	Changes
V1.00	2011.12.9		Initial version
V1.10	2011.12.30	Pin Description	GPIOE[0]/[1]/[2] and GPIOG[0]/[1]/[2] are changed for INPUT only.
V1.11	2012.1.10	Pin Dimension	Pin Dimension
V1.12	2012.3.29	Audio Codec	Revise some description

Table of Contents

1. Introduction

Allwinner Tech has expanded its processor lineup to include a new ***ARM Cortex-A8*** chip A13 which is even more competitive for Android tablets with higher performance (ManyCore Lite), lower power consumption, and lower total system cost. As the brains of ***Android 4.0***, A13 makes multitasking smoother, apps loading more quickly, and anything you touch responds instantly. What's more important, A13 is available in ***eLQFP176 package with Audio Codec and R-TP integrated***.

2. Feature

CPU

- ARM Cortex-A8 Core
- 32KB I-Cache/32KB D-Cache/256KB L2 Cache
- Using NEON for video, audio, and graphic workloads eases the burden of supporting more dedicated accelerators across the SoC and enables the system to support the standards of tomorrow
- RCT JAVA-Accelerations to optimize just in time(JIT) and dynamitic adaptive compilation(DAC), and reduces memory footprint up to three times

GPU

3D Graphic Engine

- Support Open GL ES 1.1/ 2.0 and open VG 1.1

VPU

- Video Decoding (FULL HD)
  - Support all popular video formats, including VP6/8, AVS, H.264, H.263 , MPEG-1/2/4,

etc

- Support 1920*1080@ 30fps in all formats

- Video Encoding
  - Support encoding in H.264 MP format
  - Up to 1920*1080@30fps

Display Processing Ability

- Four moveable and size-adjustable layers
- Support multi-format image input
- Support image enhancement processor
- Support Alpha blending /anti-flicker
- Support Hardware cursor
- Support output color correction (luminance / hue / saturation etc)

Display Output Ability

- Flexible LCD interface (CPU / Sync RGB)

Image Input Ability

- Camera sensor interface (CSI)

Memory

- 16-bit SDRAM controller
  - Support DDR2 SDRAM and DDR3 SDRAM up to 533MHz
  - Memory Capacity up to 512MB
- 8-bit NAND Flash Controller with 2 CE and 2 RB signals
  - Support SLC/MLC/TLC/DDR NAND

- 64-bit ECC

Peripherals

- One USB 2.0 OTG controller for general application and one USB EHCI/OHCI controller for host application
- Three high-speed memory controllers supporting SD version 3.0 and eMMC version 4.3
- One UART with only TX/RX and one UART with RTS/CTS
- Three SPI controllers
- Three Two-Wire Interfaces
- IR controller supporting CIR remoter
- 6-bit LRADC for line control
- Internal 4-wire touch panel controller with pressure sensor and 2-point touch
- Internal 24-bit Audio Codec for 2-Ch headphone and 1-Ch microphone
- PWM controller

System

- 8-Ch normal DMA and 8-Ch dedicated DMA
- Internal 48K SRAM on chip
- 6 asynchronic timers, 2 synchronic timers, 1 watchdog, and 2 AVS counters

Security

- Security System
- Support DES/3DES/AES encryption and decryption.
- Support SHA-1, MD5 message digest
- Support 160-bit hardware PRNG with 192-bit seed
- 128-bit EFUSE chip ID

Package

- eLQFP176 package

3. Functional Block Diagram

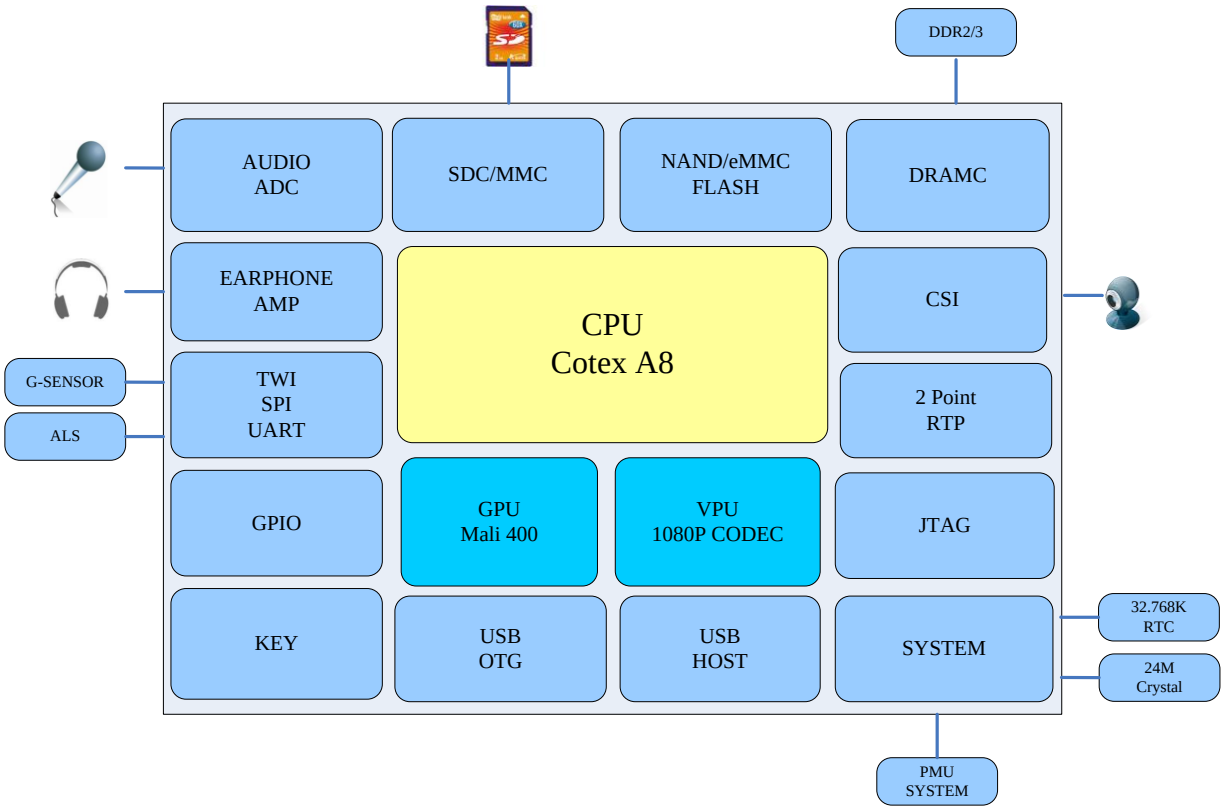


Figure 3. A13 Block Diagram

4. Pin Assignment

4.1. Pin Map

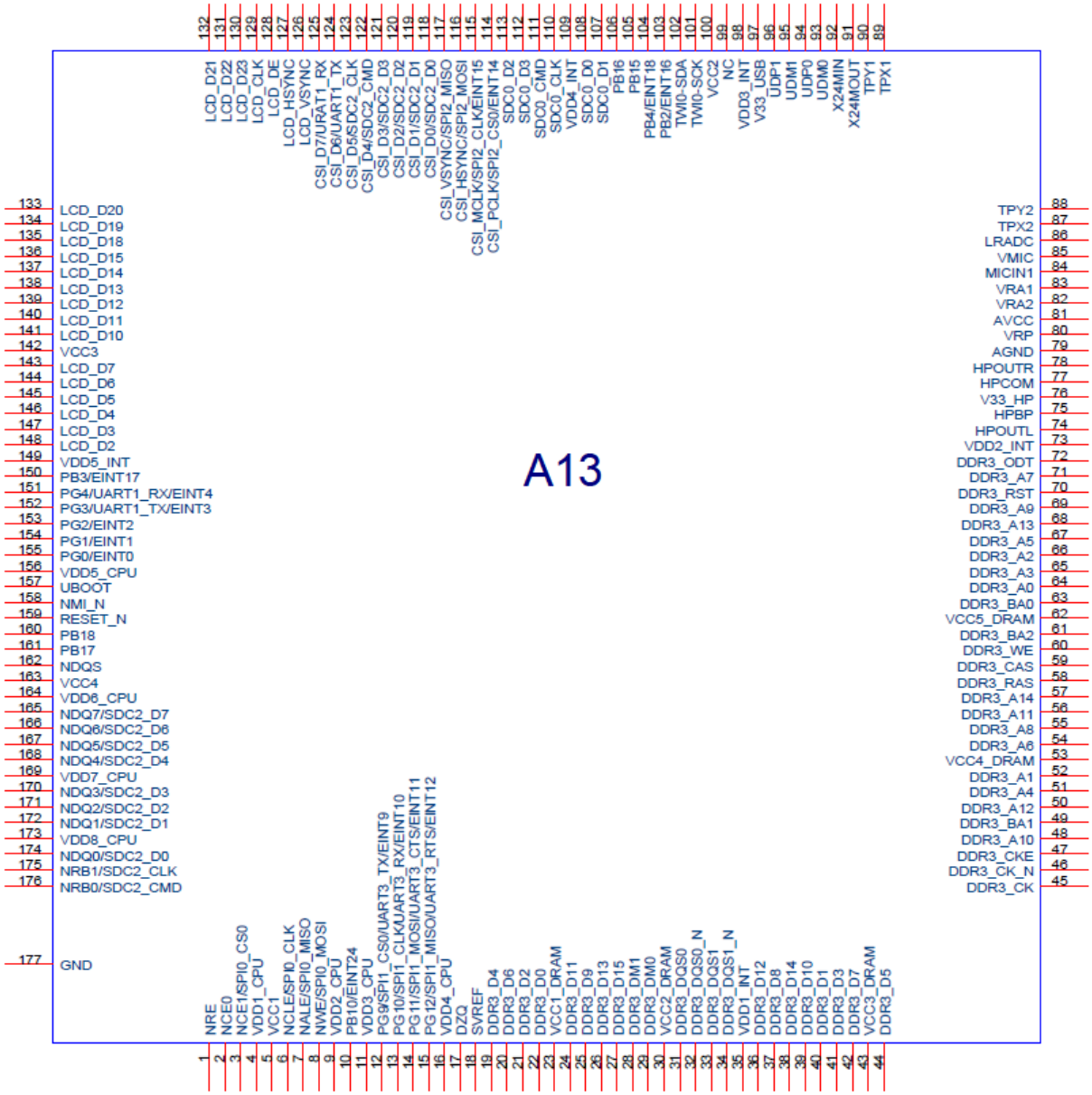


Figure 4-1. A13 eLQFP 176 Package

4.2. Pin Dimension

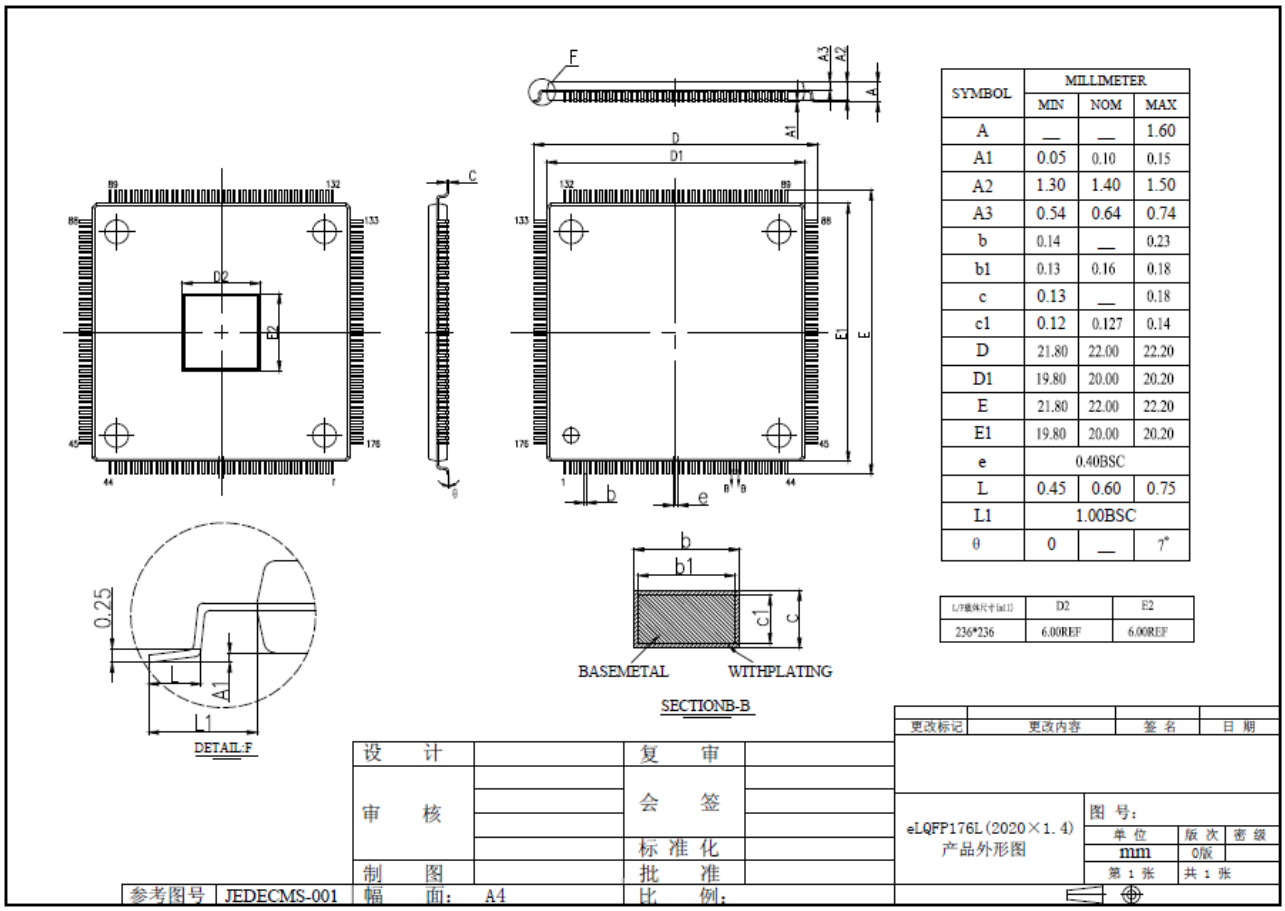


Figure 4-2. A13 Pin Dimension

5. Pin Description

5.1. Pin Characteristics

1. **Pin Number:** Ball numbers on the bottom side associated with each signals on the bottom.
2. **Pin Name:** Names of signals multiplexed on each pin No. (also notice that the name of the pin is the signal name in function 0).
3. **Type:** signal direction
   - I = Input
   - O = Output
   - I/O = Input/Output
   - A = Analog
   - AIO = Analog Input/Output
   - PWR = Power
   - GND = Ground
4. **Pin Reset State:** The state of the terminal at reset (power up).
   - 0: The buffer drives VOL(pull down/pull up resistor not activated)
   - 0 (PD): The buffer drives V_{OL} with an active pull down resistor.
   - 1: The buffer drives VOH (pull down/pull up resistor not activated).
   - 1 (PU): The buffer drives V_{OH} with an active pull up resistor.
   - Z: High-impedance
   - L: High-impedance with an active pull down resistor.
   - H: High-impedance with an active pull up resistor.
5. **Pull Up/Down:** Denotes the presence of an internal pull up or pull down resister. Pull up and pull down resistor can be enabled or disabled via software.
6. **Buffer Strength:** Drive strength of the associated output buffer.
7. Note that the P[B:G] in the following table stands for GPIO [B:G].

Pin No.	Pin Name	Type	Pin Reset State	Pull Up/Down	Buffer Strength
1	NRE	O			
	PC5				
2	NCE0	O		Pull-up	
	PC4				
3	NCE1	O		Pull-up	
	SPI0_CS0				
	PC3				
4	VDD1_CPU	PWR			
5	VCC1	PWR			
6	NCLE	O			
	SPI0_CLK				
	PC2				
7	NALE	O			
	SPI0_MISO				
	PC1				
8	NWE	O			
	SPI0_MOSI				
	PC0				
9	VDD2_CPU	PWR			
10	PB10	I/O			
	EINT24				
11	VDD3_CPU	PWR			
12	PG9	I/O			
	SPI1_CS0				
	UART3_TX				

	EINT9				
13	PG10	I/O			
	SPI1_CLK				
	UART3_RX				
	EINT10				
14	PG11	I/O			
	SPI1_MOSI				
	UART3_CTS				
	EINT11				
15	PG12	I/O			
	SPI1_MISO				
	UART3_RTS				
	EINT12				
16	VDD4_CPU	PWR			
17	DZQ	A			
18	SVREF	P			
19	DDR3_D4	I/O			
20	DDR3_D6	I/O			
21	DDR3_D2	I/O			
22	DDR3_D0	I/O			
23	VCC1_DRAM	PWR			
24	DDR3_D11	I/O			
25	DDR3_D9	I/O			
26	DDR3_D13	I/O			
27	DDR3_D15	I/O			
28	DDR3_DM1	O			
29	DDR3_DM0	O			
30	VCC2_DRAM	PWR			
31	DDR3_DQS0	I/O			

32	DDR3_DQS0_N	I/O			
33	DDR3_DQS1	I/O			
34	DDR3_DQS1_N	I/O			
35	VDD1_INT	PWR			
36	DDR3_D12	I/O			
37	DDR3_D8	I/O			
38	DDR3_D14	I/O			
39	DDR3_D10	I/O			
40	DDR3_D1	I/O			
41	DDR3_D3	I/O			
42	DDR3_D7	I/O			
43	VCC3_DRAM	PWR			
44	DDR3_D5	I/O			
45	DDR3_CK	O			
46	DDR3_CK_N	O			
47	DDR3_CKE	O			
48	DDR3_A10	O			
49	DDR3_BA1	O			
50	DDR3_A12	O			
51	DDR3_A4	O			
52	DDR3_A1	O			
53	VCC4_DRAM	PWR			
54	DDR3_A6	O			
55	DDR3_A8	O			
56	DDR3_A11	O			
57	DDR3_A14	O			
58	DDR3_RAS	O			
59	DDR3_CAS	O			
60	DDR3_WE	O			

61	DDR3_BA2	O			
62	VCC5_DRAM	PWR			
63	DDR3_BA0	O			
64	DDR3_A0	O			
65	DDR3_A3	O			
66	DDR3_A2	O			
67	DDR3_A5	O			
68	DDR3_A13	O			
69	DDR3_A9	O			
70	DDR3_RST	O			
71	DDR3_A7	O			
72	DDR3_ODT	O			
73	VDD2_INT	PWR			
74	HPOUTL	O			
75	HPBP	O			
76	V33_HP	PWR			
77	HPCOM	O			
78	HPOUTR	O			
79	AGND	GND			
80	VRP	A			
81	AVCC	PWR			
82	VRA2	A			
83	VRA1	A			
84	MICIN1	I			
85	VMIC	PWR			
86	LRADC	I			
87	TPX2	I			
88	TPY2	I			
89	TPX1	I			

90	TPY1	I			
91	X24MOUT	O			
92	X24MIN	I			
93	UDM0	I/O			
94	UDP0	I/O			
95	UDM1	I/O			
96	UDP1	I/O			
97	V33_USB	PWR			
98	VDD3-INT	PWR			
99	NC				
100	VCC2	PWR			
101	TWI0-SCK	I/O			
	PB0				
102	TWI0-SDA	I/O			
	PB1				
103	PB2/EINT16	I/O			
104	PB4/EINT18	I/O			
105	PB15	I/O			
106	PB16	I/O			
107	SDC0_D1	I/O			
	PF0				
108	SDC0_D0	I/O			
	PF1				
109	VDD4_INT	PWR			
110	SDC0_CLK	I/O			
	PF2				
111	SDC0_CMD	I/O			
	PF3				
112	SDC0_D3				

	PF4				
113	SDC0_D2				
	PF5				
114	CSI_PCLK	I/O			
	SPI2_CS0				
	EINT14				
	PE0				
115	CSI_MCLK	I/O			
	SPI2_CLK				
	EINT15				
	PE1				
116	CSI_HSYNC	I/O			
	SPI2_MOSI				
	PE2				
117	CSI_VSYNC	I/O			
	SPI2_MISO				
	PE3				
118	CSI_D0	I/O			
	SDC2_D0				
	PE4				
119	CSI_D1	I/O			
	SDC2_D1				
	PE5				
120	CSI_D2	I/O			
	SDC2_D2				
	PE6				
121	CSI_D3	I/O			
	SDC2_D3				
	PE7				

122	CSI_D4	I/O			
	SDC2_CMD				
	PE8				
123	CSI_D5	I/O			
	SDC2_CLK				
	PE9				
124	CSI_D6	I/O			
	UART1_TX				
	PE10				
125	CSI_D7	I/O			
	UART1_RX				
	PE11				
126	LCD_VSYNC	I/O			
	PD27				
127	LCD_HSYNC	I/O			
	PD26				
128	LCD_DE	I/O			
	PD25				
129	LCD_CLK	I/O			
	PD24				
130	LCD_D23	I/O			
	PD23				
131	LCD_D22	I/O			
	PD22				
132	LCD_D21	I/O			
	PD21				
133	LCD_D20	I/O			
	PD20				
134	LCD_D19	I/O			

	PD19				
135	LCD_D18	I/O			
	PD18				
136	LCD_D15	I/O			
	PD15				
137	LCD_D14	I/O			
	PD14				
138	LCD_D13	I/O			
	PD13				
139	LCD_D12	I/O			
	PD12				
140	LCD_D11	I/O			
	PD11				
141	LCD_D10	I/O			
	PD10				
142	VCC3	PWR			
143	LCD_D7	I/O			
	PD7				
144	LCD_D6	I/O			
	PD6				
145	LCD_D5	I/O			
	PD5				
146	LCD_D4	I/O			
	PD4				
147	LCD_D3	I/O			
	PD3				
148	LCD_D2	I/O			
	PD2				
149	VDD5_INT	PWR			

150	PB3	I/O			
	EINT17				
151	PG4	I/O			
	UART1_RX				
	EINT4				
152	PG3	I/O			
	UART1_TX				
	EINT3				
153	PG2	I/O			
	EINT2				
154	PG1	I/O			
	EINT1				
155	PG0	I/O			
	EINT0				
156	VDD5_CPU	PWR			
157	UBOOT	IO		Pull-up	
158	NMI_N	A		No pull	
159	RESET_N	A			
160	PB18	I/O			
161	PB17	I/O			
162	NDQS	I/O			
	PC19				
163	VCC4	PWR			
164	VDD6_CPU	PWR			
165	NDQ7	I/O			
	SDC2_D7				
	PC15				
166	NDQ6	I/O			
	SDC2_D6				

	PC14				
167	NDQ5	I/O			
	SDC2_D5				
	PC13				
168	NDQ4	I/O			
	SDC2_D4				
	PC12				
169	VDD7_CPU	PWR			
170	NDQ3	I/O			
	SDC2_D3				
	PC11				
171	NDQ2	I/O			
	SDC2_D2				
	PC10				
172	NDQ1	I/O			
	SDC2_D1				
	PC9				
173	VDD8_CPU	PWR			
174	NDQ0	I/O			
	SDC2_D0				
	PC8				
175	NRB1	I		Pull-up	
	SDC2_CLK				
	PC7				
176	NRB0	I		Pull-up	
	SDC2_CMD				
	PC6				

Table 5-1 Pin Characteristic

5.2. Multiplexing Characteristics

The following tables provide a description of the A13 multiplexing on the eLQFP176 package.

PortB(PB)	Multiplex Function Select			
	Default	Multi1	Multi2	Multi3
PB0	TWI0_SCK			
PB1	TWI0_SDA			
PB2	PWM			EINT16
PB3	PB	IR_TX		EINT17
PB4	PB	IR_RX		EINT18
PB10	PB	SPI2_CS1		EINT24
PB15	TWI1_SCK			
PB16	TWI1_SDA			
PB17	TWI2_SCK			
PB18	TWI2_SDA			

Table 5-2 Port B(PB) Multiplex Function Select

PortC(PC)	Multiplex Function Select			
	Default	Multi1	Multi2	Multi3
PC0	NWE	SPI0_MOSI		
PC1	NALE	SPI0_MISO		
PC2	NCLE	SPI0_CLK		
PC3	NCE1	SPI0_CS0		
PC4	NCE0			
PC5	NRE			
PC6	NRB0	SDC2_CMD		
PC7	NRB1	SDC2_CLK		
PC8	NDQ0	SDC2_D0		
PC9	NDQ1	SDC2_D1		

PC10	NDQ2	SDC2_D2		
PC11	NDQ3	SDC2_D3		
PC12	NDQ4	SDC2_D4		
PC13	NDQ5	SDC2_D5		
PC14	NDQ6	SDC2_D6		
PC15	NDQ7	SDC2_D7		
PC19	NDQS			

Table 5-3 Port C(PC) Multiplex Function Select Table

PortD(PD)	Multiplex Function Select			
	Default	Multi1	Multi2	Multi3
PD2	LCD_D2			
PD3	LCD_D3			
PD4	LCD_D4			
PD5	LCD_D5			
PD6	LCD_D6			
PD7	LCD_D7			
PD10	LCD_D10			
PD11	LCD_D11			
PD12	LCD_D12			
PD13	LCD_D13			
PD14	LCD_D14			
PD15	LCD_D15			
PD18	LCD_D18			
PD19	LCD_D19			
PD20	LCD_D20			
PD21	LCD_D21			
PD22	LCD_D22			
PD23	LCD_D23			

PD24	LCD_CLK			
PD25	LCD_DE			
PD26	LCD_HSYNC			
PD27	LCD_VSYNC			

Table 5-4 Port D(PD) Multiplex Function Select Table

PortE(PE)	Multiplex Function Select			
	Default	Multi1	Multi2	Multi3
PE0	CSI_PCLK	SPI2_CS0		EINT14
PE1	CSI_MCLK	SPI2_CLK		EINT15
PE2	CSI_HSYNC	SPI2_MOSI		
PE3	CSI_VSYNC	SPI2_MISO		
PE4	CSI_D0	SDC2_D0		
PE5	CSI_D1	SDC2_D1		
PE6	CSI_D2	SDC2_D2		
PE7	CSI_D3	SDC2_D3		
PE8	CSI_D4	SDC2_CMD		
PE9	CSI_D5	SDC2_CLK		
PE10	CSI_D6	UART1_TX		
PE11	CSI_D7	UART1_RX		

Note: The PE0/PE1/PE2 are for input only.

Table 5-5 Port E(PE) Multiplex Function Select Table

PortF(PF)	Multiplex Function Select			
	Default	Multi1	Multi2	Multi3
PF0	SDC0_D1			
PF1	SDC0_D0			
PF2	SDC0_CLK			
PF3	SDC0_CMD			

PF4	SDC0_D3			
PF5	SDC0_D2			

Table 5-6 Port F(PF) Multiplex Function Select Table

PortG(PG)	Multiplex Function Select			
	Default	Multi1	Multi2	Multi3
PG0	PG			EINT0
PG1	PG			EINT1
PG2	PG			EINT2
PG3	PG	UART1_TX		EINT3
PG4	PG	UART1_RX		EINT4
PG9	PG	SPI1_CS0	UART3_TX	EINT9
PG10	PG	SPI1_CLK	UART3_RX	EINT10
PG11	PG	SPI1_MOSI	UART3_CTS	EINT11
PG12	PG	SPI1_MISO	UART3_RTS	EINT12

Note: The PG0/PG1/PG2 are for input only.

Table 5-7 Port G(PG) Multiplex Function Select Table

5.3. Power and Miscellaneous Signals

Many signals are available on multiple pins according to the software configuration of the multiplexing options.

1. Signal Name: The signal name
2. Description: Description of the signal
3. Type: Pin type for this specific function:
   - I = Input
   - O = Output
   - Z = High-impedance

- A = Analog
- PWR = Power
- GND = Ground

4. Pin #: Associated ball(s) number

5.3.1. Power Domain Signal Description

Signal Name	Description	Pin Name	Pin No.
Audio DAC Power			
V33_HP	Headphone Power Supply	V33_HP	76
Audio ADC Power			
VMIC	Microphone ADC Power Supply	VMIC	85
USB Power			
V33_USB	USB Power Supply	UVCC	97
IO Power			
VCC	IO Power Supply	VCC(4)	5/100/163/142
CPU Power			
VDD_CPU		VDD2(8)	4/9/11/16/156/164/169/173
Interrupt Power			
VDD_INT	Interrupt Power Supply	VDD_INT(5)	35/73/98/109/149
DRAM Power			
VCC_DRAM	DRAM Power Supply	VCC(5)	23/30/43/53/62
Analog Power			
AVCC	Analog Power Supply	AVCC	81
AGND	Analog Ground	AGND	79

Table 5-8 Power Domain Signal Description

5.3.2. Miscellaneous Signal Description

Signal Name	Description	Type	Pin Name	Pin No.
Clock				
X24MIN	Main 24MHz crystal Input for internal OSC	I	X24MIN	92
X24MOUT	Main 24MHz crystal Output for internal OSC	O	X24MOUT	91
Reset				
RESET_N	System Reset		RESET_N	159
FIQ				
NMI_N	External Fast Interrupt Request		NMI_N	158
Boot				
UBOOT	Boot Mode	I	BOOT	157
Others				
VRP	=AVCC=3.0V	A	VRP	80
VRA1	=1.5V	A	VRA1	83
VRA2	=0V	A	VRA2	82

Table 5-9 Miscellaneous Signal Description

6. Electrical Characteristics

6.1. Absolute Maximum Ratings

The absolute maximum ratings (shown in Table 6-1) define limitations for electrical and thermal stresses. These limits prevent permanent damage to the A13.

Note: Absolute maximum ratings are not operating ranges. Operation at absolute maximum ratings is not guaranteed.

Symbol	Parameter		Min	Typ	Unit
TS	Storage Temperature		-20	125	℃
II/O	In/Out current for input and output		/	/	mA
VESD	ESD stress voltage	HBM(human body model)	/	/	VESD
		CDM(charged device model)	-	-	
VCC	DC Supply Voltage for I/O		2.7	3.3	V
VDD	DC Supply Voltage for Internal Digital Logic		1.0	1.3	V
VCC_ANALOG	DC Supply Voltage for Analog Part		2.7	3.3	V
VCC_DRAM	DC Supply Voltage for DRAM Part		1.3	2.0	V
VCC_USB	DC Supply Voltage for USB PHY		2.7	3.3	V
VCC_LRADC	DC Supply Voltage for LRADC		3.0	3.0	V
VCC_HP	DC Supply Voltage for Headphone		2.7	3.3	V
VDD_PLL	DC Supply Voltage for PLL		1.2	1.3	V

Table 6-1 Multiplexing Characteristics

6.2. Recommended Operating Conditions

All A13 modules are used under the operating Conditions contained in Table 6-2.

Symbol	Parameter	Min	Typ	Max	Unit
Ta	Operating Temperature[Commercial]	-25	–	+85	℃
	Operating Temperature[Extended]	-40	–	+85	℃
GND	Ground	0	0	0	V
VCC	DC Supply Voltage for I/O	/	3.3	/	V
VDD	DC Supply Voltage for Internal Digital Logic	/	1.2	/	V
VCC_ANALOG	DC Supply Voltage for Analog Part	/	3.0	/	V
VCC_DRAM	DC Supply Voltage for DRAM Part	/	1.5/1.8	/	V
VCC_USB	DC Supply Voltage for USB PHY	/	3.3	/	V

Table 6-2 Recommended Operating Conditions

6.3. DC Electrical Characteristics

Table 6-3 summarizes the DC electrical characteristics of A13.

Symbol	Parameter	Min	Typ	Max	Unit
VIH	High-level input voltage	2.4	3.0	3.3	V
VIL	Low-level input voltage	0	0.5	1.0	V
VHYS	Hysteresis voltage	/	/	/	mV
IIH	High-level input current	/	/	/	uA
IIL	Low-level input current	/	/	/	uA
VOH	High-level output voltage	3.3	3.3	3.3	V
VOL	Low-level output voltage	0	0	0	V
IOZ	Tri-State output leakage current	/	/	/	uA
CIN	Input capacitance	/	/	/	pF
COUT	Output capacitance	/	/	/	pF

Table 6-3 DC Electrical Characteristics

6.4. Oscillator Electrical Characteristics

The A13 contains a 24.000 MHz oscillator.

The A13 device operation requires the following input clock:

- The 24.000MHz frequency is used to generate the main source clock of the A13 device.

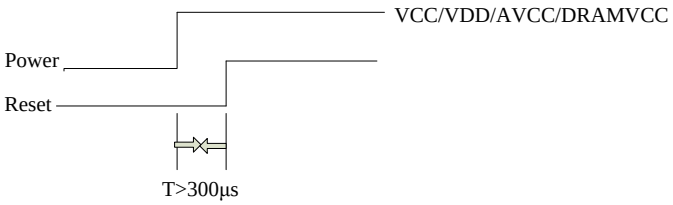
6.4.1. 24MHz Oscillator Characteristics

Table 6-4 lists the 24.MHz crystal specifications.

Symbol	Parameter	Min	Typ	Max	Unit
1/(tCPMAIN)	Crystal Oscillator Frequency Range		24.000		MHz
tST	Startup Time	–	–		ms
	Frequency Tolerance at 25 ℃	-50	–	+50	ppm
	Oscillation Mode	Fundamental			–
	Maximum change over temperature range	-50	–	+50	ppm
PON	Drive level	–	–	50	uW
CL	Equivalent Load capacitance	–		–	pF
CL1,CL2	Internal Load capacitance(CL1=CL2)	–		–	pF
RS	Series Resistance(ESR)	–		–	Ω
	Duty Cycle	30	50	70	%
CM	Motional capacitance	–	–		pF
CSHUT	Shunt capacitance	–	–		pF
RBIAS	Internal bias resistor				MΩ

Table 6-4 24MHz Oscillator Characteristics

6.5. Power up/down and Reset Specifications



6.5.1. Power-up Sequence

The external voltage regulator and other power-on devices must provide the processor with a specific sequence of power and resets to ensure proper operation. Figure 6-x shows this sequence and is detailed in Table 6-x.

6.5.2. Power-down Sequence

The sequence indicated in Figure 6-x and detailed in Table 6-x is the required timing parameters for power-down.

7. PWM

7.1. Overview

The output of the PWM is a toggling signal whose frequency and duty cycle can be modulated by its programmable registers. Each channel has a dedicated internal 16-bit up counter. If the counter reaches the value stored in the channel period register, it resets. At the beginning of a count period cycle, the PWMOUT is set to activate state and count from 0x0000.

The PWM divider divides the clock (24MHz) by 1-4096 according to the pre-scalar bits in the PWM control register.

In PWM cycle mode, the output will be a square waveform; the frequency is set to the period register. In PWM pulse mode, the output will be a positive pulse or a negative pulse.

7.2. PWM Signal Description

Signal Name	Description	Type	Pin Name
PWM	PWM output	O	PB2

Table 7. PWM Signal Description

8. Async Timer Controller

8.1. Overview

The chip implements 6 timers.

Timer 0/1/2 can take their inputs from the PLL6/6 or OSC24M. They provide the operating system's scheduler interrupt. It is designed to offer maximum accuracy and efficient management, even for systems with long or short response time. They provide 32-bit programmable overflow counter and work in auto-reload mode or no-reload mode.

The watch-dog is used to resume controller operation by generating a general reset or an interrupt request when it is disturbed by malfunctions such as noise sand system errors. It features a down counter that allows a watchdog period of up to 16 seconds.

Timer 3 is used for OS to generate a periodic interrupt.

9. Sync Timer Controller

9.1. Overview

The chip implements 2 sync timers for high-speed counter.

10. Interrupt Controller

10.1. Overview

The interrupt controller features:

- Control the nIRQ and FIQ of a RISC Processor
- 4-Level Priority Controller
- External Sources of Edge-sensitive or Level-sensitive

Since the 4-level Priority Controller allows users to define the priority of each interrupt source, so higher priority interrupts can be serviced even if a lower priority interrupt is being treated.

10.2. External Interrupt Signal Description

Signal Name	Description	Type	Pin Name
EINT0	External Interrupt source 0	I	PG0
EINT1	External Interrupt source 1	I	PG1
EINT2	External Interrupt source 2	I	PG2
EINT3	External Interrupt source 3	I	PG3
EINT4	External Interrupt source 4	I	PG4
EINT9	External Interrupt source 9	I	PG9
EINT10	External Interrupt source 10	I	PG10
EINT11	External Interrupt source 11	I	PG11
EINT12	External Interrupt source 12	I	PG12
EINT14	External Interrupt source 14	I	PE0
EINT15	External Interrupt source 15	I	PE1
EINT16	External Interrupt source 16	I	PB2

Signal Name	Description	Type	Pin Name
EINT17	External Interrupt source 17	I	PB3
EINT18	External Interrupt source 18	I	PB4
EINT24	External Interrupt source 24	I	PB10

Table 10. External Interrupt Signal Description

11. DMA Controller

11.1. Overview

There are two kinds of DMA in the chip. One is Normal DMA with 8 channels, and the other is Dedicated DMA with 8 channels.

For normal DMA, only one channel can be active and the sequence is in accordance with the priority level. As for the dedicated DMA, at most 8-channel can be active at the same time if their source or destination does not conflict.

12. SDRAM Controller

12.1. Overview

The SDRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to all industy-standard double data rate II (DDR2) ordinary SDRAM and Double data rate III (DDR3) ordinary SDRAM. It supports up to a 512MB memory address space.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type, and Extended-Mode-Register settings.

The DRAMC includes following features:

- Support DDR2 SDRAM and DDR3 SDRAM
- Support different memory device power voltage of 1.5V and 1.8V
- Support DDR2/3 SDRAM of clock frequency up to DDR1066
- Support memory capacity up to 512MB
- 15 address lines and 3 bank address lines
- Data IO size can up to 16-bit for DDR2 and DDR3
- Automatically generate initialization and refresh sequences
- Runtime-configurable parameters setting for application flexibility
- Clock frequency can be chosen for different applications
- Priority of transferring through multiple ports is programmable
- Support random read or write operation

12.2. SDRAM Signal Description

Signal Name	Description	Pin Name	Type
DDR3_D4	SDRAM Data Bus Bit 4	DDR3_D4	I/O
DDR3_D3	SDRAM Data Bus Bit3	DDR3_D3	I/O

DDR3_D1	SDRAM Data Bus Bit1	DDR3_D1	I/O
DDR3_D6	SDRAM Data Bus Bit6	DDR3_D6	I/O
DDR3_D12	SDRAM Data Bus Bit12	DDR3_D12	I/O
DDR3_D11	SDRAM Data Bus Bit11	DDR3_D11	I/O
DDR3_D9	SDRAM Data Bus Bit9	DDR3_D9	I/O
DDR3_D14	SDRAM Data Bus Bit14	DDR3_D14	I/O
DDR3_DM1	SDRAM Data Mask1	DDR3_DM1	O
DDR3_DM0	SDRAM Data Mask0	DDR3_DM0	O
DQS0	SDRAM Data Strobe0	DQS0	I/O
DQS0_N	SDRAM Data Strobe0 Invert	DQS0_N	I/O
DQS1	SDRAM Data Strobe1	DQS1	I/O
DQS1_N	SDRAM Data Strobe1 Invert	DQS1_N	I/O
DDR3_D15	SDRAM Data Bus Bit15	DDR3_D15	I/O
DDR3_D8	SDRAM Data Bus Bit8	DDR3_D8	I/O
DDR3_D10	SDRAM Data Bus Bit10	DDR3_D10	I/O
DDR3_D13	SDRAM Data Bus Bit13	DDR3_D13	I/O
DDR3_D7	SDRAM Data Bus Bit7	DDR3_D7	I/O
DDR3_D0	SDRAM Data Bus Bit0	DDR3_D0	I/O
DDR3_D2	SDRAM Data Bus Bit2	DDR3_D2	I/O
DDR3_D5	SDRAM Data Bus Bit5	DDR3_D5	I/O
DDR3_CK	SDRAM Clock	DDR3_CK	O
DDR3_CK_N	SDRAM Clock Invert	DDR3_CK_N	O
DDR3_ODT	SDRAM ODT control signal	DDR3_ODT	O
DDR3_RAS	SDRAM Row Address Strobe	DDR3_RAS	O
DDR3_CAS	SDRAM Colomn Address Strobe	DDR3_CAS	O
DDR3_A0	SDRAM Data Address Bit0	DDR3_A0	O
DDR3_A2	SDRAM Data Address Bit2	DDR3_A2	O
DDR3_A4	SDRAM Data Address Bit4	DDR3_A4	O
DDR3_A6	SDRAM Data Address Bit6	DDR3_A6	O

DDR3_A8	SDRAM Data Address Bit8	DDR3_A8	O
DDR3_A14	SDRAM Data Address Bit14	DDR3_A14	O
DDR3_A11	SDRAM Data Address Bit11	DDR3_A11	O
DDR3_A13	SDRAM Data Address Bit13	DDR3_A13	O
DDR3_CKE	SDRAM Clock Enable	DDR3_CKE	O
DDR3_WE	SDRAM Write Enable	DDR3_WE	O
DDR3_BA2	SDRAM Bank Select 2	DDR3_BA2	O
DDR3_BA1	SDRAM Bank Select 1	DDR3_BA1	O
DDR3_BA0	SDRAM Bank Select 0	DDR3_BA0	O
DDR3_A1	SDRAM Data Address Bit1	DDR3_A1	O
DDR3_A10	SDRAM Data Address Bit10	DDR3_A10	O
DDR3_A5	SDRAM Data Address Bit5	DDR3_A5	O
DDR3_A3	SDRAM Data Address Bit3	DDR3_A3	O
DDR3_A9	SDRAM Data Address Bit 9	DDR3_A9	O
DDR3_A7	SDRAM Data Address Bit7	DDR3_A7	O
DDR3_A12	SDRAM Data Address Bit 12	DDR3_A12	O
DZQ	SDRAM ZQ Calibration	DZQ	A
SVREF	SDRAM Reference Input	SVREF	P

Table 12. SDRAM Signal Description

13. NAND Flash Controller

13.1. Overview

The NFC supports all NAND/MLC flash memory available in the market and new types can be supported by software re-configuration as well. It can support 2 NAND flash with 3.3 V voltage supply. There are 2 separate chip select lines (CE#) to connect up to 2 flash chips with2 R/B signals.

The On-the-fly error correction code (ECC) is built in NFC to enhance reliability. BCH is implemented to detect and correct up to 64 bits error per 512 or 1024 bytes data. The on chip ECC and parity checking circuitry of NFC frees CPU for other tasks. The ECC function can be disabled by software.

The data can be transferred by DMA or by CPU memory-mapped IO method. The NFC provides automatic timing control to read or write external Flash. The NFC maintains the proper relativity for CLE, CE# and ALE control signal lines. Three kinds of modes are supported for serial read access: Mode 0 is the conventional serial access, Mode 1 for EDO type, and Mode 2 is for extension EDO type. In addition, NFC can monitor the status of R/B# signal line.

Block management and wear leveling management are implemented in software.

The NFC features:

- Support SLC/MLC/TLC flash and EF-NAND memory
- Software configure seed to randomize engine
- Software configure method for adaptability to a variety of system and memory types
- Support 8-bit Data Bus Width
- Support 1024, 2048, 4096, 8192, 16384 bytes size per page
- Support 3.3 V voltage supply Flash

- Up to 2 flash chips which are controlled by NFC_CEx#
- Support Conventional and EDO serial access method for serial reading Flash
- On-the-fly BCH error correction code which correcting up to 64 bits per 512 or 1024 bytes
- Corrected Error bits number information report
- ECC automatic disable function for all 0xff data
- NFC status information is reported by its registers
- Support interrupt
- One Command FIFO
- Support external DMA for data transfer
- Two 256x32-bit RAM for Pipeline Procession
- Support SDR, DDR and Toggle 1.0 NAND

13.2. NAND Flash Controller Signal Description

Signal Name	Description	Type	Pin Name
NCE[1:0]	NAND FLASH Chip Select bit	O	NCE[1:0]
NRB[1:0]	NAND FLASH Chip Ready/Busy bit	I	NRB[1:0]
NWE	NAND FLASH Chip Write Enable	O	NWE
NRE	NAND FLASH Chip Read Enable	O	NRE
NALE	NAND FLASH Chip Address Latch Enable	O	NALE
NCLE	NAND FLASH Chip Command Latch Enable	O	NCLE
NDQ[7:0]	NAND FLASH Data bit	I/O	NDQ[7:0]
NDQS	NAND FLASH Data Strobe	I/O	NDQS

Table 13. NAND Flash Controller Signal Description

14. SD3.0 Controller

14.1. Overview

The SD3.0 controller can be configured as a Secure Digital Multimedia Card controller, which simultaneously supports Secure Digital memory (SD Memo), UHS-1 Card, Secure Digital I/O (SDIO), Multimedia Cards (MMC), eMMC Card and Consumer Electronics Advanced Transport Architecture (CE-ATA).

The SD3.0 controller features:

- Support Secure Digital memory protocol commands (up to SD3.0)
- Support Secure Digital I/O protocol commands
- Support Multimedia Card protocol commands (up to MMC4.3)
- Support CE-ATA digital protocol commands
- Support eMMC boot operation and alternative boot operation
- Support Command Completion signal and interrupt to host processor and Command Completion Signal disable feature
- Support one SD (Verson1.0 to 3.0) or MMC (Verson3.3 to 4.3) or CE-ATA device
- Support hardware CRC generation and error detection
- Support programmable baud rate
- Support host pull-up control
- Support SDIO interrupts in 1-bit and 4-bit modes
- Support SDIO suspend and resume operation
- Support SDIO read wait

- Support block size of 1 to 65535 bytes
- Support descriptor-based internal DMA controller
- Internal 16x32-bit (64 bytes total) FIFO for data transfer
- Support 3.3 V IO pad

14.2. SD3.0 Controller Signal Description

SDCx=SDC[2,0]

Signal Name	Description	Type
SDCx_CLK	SDx/SDIOx/MMCx Clock	O
SDCx_CMD	SDx/SDIOx/MMCx Command Line	I/O
SDCx_D	SD Card data bit	I/O

Table 14. SD3.0 Controller Signal Description

15. Two Wire Interface

15.1. Overview

This Two Wire Controller is an interface between CPU host and the serial 2-Wire bus, which supports all standard 2-Wire transfer, including Slave and Master. The communication to the 2-Wire bus is carried out on a byte-wise basis using interrupt or polled handshaking. This 2-Wire Controller can be operated in standard mode (100K bps) or fast-mode (up to 400K bps). Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is supported in Slave mode.

The 2-Wire Controller features:

- Software-programmable for Slave or Master
- Support Repeated START signal
- Support Multi-master systems
- Support 10-bit addressing with 2-Wire bus
- Perform arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Support speed up to 400K bits/s (‘fast mode’)
- Support operation from a wide range of input clock frequencies

15.2. TWI Controller Signal Description

TWIx=TWI[2:0]

Signal Name	Description	Type
TWIx_SCK	TWI-BUS Clock for Channel x	I/O

TWIx_SDA	TWI-BUS Data for Channel x	I/O

Table 15. TWI Controller Signal Description

16. SPI Interface

16.1. Overview

The SPI is the Serial Peripheral Interface which allows rapid data communication with less software interrupts. The SPI module contains one 8x64 receiver buffer (RXFIFO) and one 8x64 transmit buffer (TXFIFO). It can work in two modes: Master mode and Slave mode.

It features:

- Full-duplex synchronous serial interface
- Configurable Master/Slave
- 8x64 FIFO for data transmit and receive
- Configurable Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK)
- Support Dedicated DMA

16.2. SPI Controller Signal Description

SPIx=SPI[2:0]

Signal Name	Description	Type
SPIx_CS[1:0]	SPIx Chip Select	I/O
SPIx_MOSI	SPIx Master data Out, Slave data In	I/O
SPIx_MISO	SPIx Master data In, Slave data Out	I/O
SPIx_CLK	SPIx Clock	I/O

Table 16. SPI Controller Signal Description

17. UART Interface

17.1. Overview

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types responsible for its assertion. Each of the interrupt types can be separately enabled/disabled with the control registers.

The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

The UART supports word lengths from five to eight bits, an optional parity bit and 1, 1.5 or 2 stop bits, and is fully programmable by an AMBA APB CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

The UART includes the following features:

- Compatible with industry-standard 16550 UARTs
- 64-Bytes Transmit and receive data FIFOs
- DMA controller interface

- Software/ Hardware Flow Control
- Programmable Transmit Holding Register Empty interrupt
- Interrupt support for FIFOs, Status Change

17.2. UART Controller Signal Description

Signal Name	Description	Type
UART1_TX	UART1 Transmit Data	O
UART1_RX	UART1 Receive Data	I
UART3_TX	UART3 Transmit Data	O
UART3_RX	UART3 Receive Data	I
UART3_CTS	UART3 Clear To Send	I
UART3_RTS	UART3 Request To Send	O

Table 17. UART Controller Signal Description

18. CIR Interface

18.1. Overview

The CIR features:

- Full physical layer implementation
- Support CIR for remote control or wireless keyboard
- Dual 8x16-bit FIFO for data transfer
- Programmable FIFO thresholds
- Support Interrupt and DMA

CIR receiver is implemented in hardware to save CPU resource. It samples the input signals on the programble frequency and records these samples into RX FIFO when one CIR signal is found on the air. The CIR receiver uses Run-Length Code (RLC) to encode pulse width, and the encoded data is buffered in a 64 levels and 8-bit width RX FIFO: the MSB bit is used to record the polarity of the receiving CIR signal (The high level is represented as 1 and the low level is represented as 0), and the rest 7 bits are used for the length of RLC. The maximum length is 128. If the duration of one level (high or low) is more than 128, another byte is used. Since there are always some noises in the air, a threshold can be set to filter the noises to reduce system loading and improve system stability.

18.2. CIR Controller Signal Description

Signal Name	Description	Type
IR_TX	CIR Transmit Data	O
IR_RX	CIR Receive Data	I

Table 18. CIR Controller Signal Description

19. USB OTG Controller

19.1. Overview

The USB OTG is dual-role controller supporting Host and device functions. It can also be configured as a Host-only or Device-only controller, full compliant with the USB 2.0 Specification. The USB OTG can support high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps) transfers in Host mode, support high-speed (HS, 480-Mbps) and full-speed (FS, 12-Mbps) in Device mode.

The USB2.0 OTG controller (SIE) features:

- 64-Byte Endpoint 0 for Control Transfer
- Support up to 5 User-Configurable Endpoints for Bulk , Isochronous**,** Control and Interrupt bi-directional transfers
- Support High-Bandwidth Isochronous & Interrupt transfers
- Support point-to-point and point-to-multipoint transfer in both Host and Peripheral mode

19.2. USB OTG Controller Signal Description

Signal Name	Description	Type
UDM0	USB0 OTG Data Negative	IO
UDP0	USB0 OTG Data Positive	IO

Table 19. USB OTG Controller Signal Description

20. USB HOST Controller

20.1. Overview

USB Host Controller is fully compliant with the USB 2.0 specification, Enhanced Host Controller Interface (EHCI) Specification, Revision 1.0, and the Open Host Controller Interface (OHCI) Specification Release 1.0a. The controller supports high-speed, 480-Mbps transfers (40 times faster than USB 1.1 full-speed mode) using an EHCI Host Controller, as well as full and low speeds through one or more integrated OHCI Host Controllers.

It features:

- Include an internal DMA Controller for data transfer with memory.
- Comply with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) Device.
- Support only one USB Root Port shared between EHCI and OHCI

20.2. USB HOST Controller Signal Description

Signal Name	Description	Type
UDM1	USB1 HOST Negative output	IO
UDP1	USB1 HOST Positive output	IO

Table 20. USB Host Controller Signal Description

21. Audio Codec

21.1. Overview

The embedded Audio Codec is a high-quality stereo audio codec with headphone amplifier.

It features:

- On-chip 24-bit DAC for play-back
- On-chip 24-bit ADC for recorder
- Support analog/ digital volume control
- Support 48K and 44.1K sample family
- Support 192K and 96K sample
- Support Microphone recorder
- Stereo headphone amplifier that can be operated in capless headphone mode
- Support Virtual Ground to automatically change to True Ground to protect headphone amplifier and make function work in normal mode

21.2. Audio Codec Signal Description

Signal Name	Description	Type
HPL	Headphone Left channel output	O
HPR	Headphone Right channel output	O
HPCOM	Headphone amplifier output	O
HPBP	Headphone Bypass output	O
MICIN1	Audio ADC Input Channel 1 of Microphone	I

Table 21. Audio Codec Signal Description

22. LRADC

22.1. Overview

LRADC is 6-bit resolution and can work up to maximum conversion rate of 250Hz.

It features:

- Support APB 32-bit bus width
- Support interrupt
- Support hold key and general key
- Support single key and continue key mode
- 6-bit resolution
- Voltage input range between 0 to 2V
- Sample rate up to 250Hz

22.2. LRADC Signal Description

Signal Name	Description	Type
LRADC	Low Resolution ADC input(6 bits)	I

Table 22. LRADC Signal Description

23. Touch Panel Controller

23.1. Overview

The controller is a 4-wire resistive touch screen controller, includes 12-bit resolution A/D converter. Especially, it provides the ability of dual touch detection. The controller through the implementation of the two A/D conversion has been identified by the location of the screen of single touch, in addition to measurable increase in pressure on the touch screen.

It features:

- 12-bit SAR type A/D converter
- 4-wire I/F
- Dual touch detect
- Touch-pressure measurement (Support program set threshold)
- Sampling frequency: 2MHz (max)
- Single-ended conversion of touch screen inputs and ratiometric conversion of touch screen inputs
- TACQ up to 262ms
- Median and averaging filter to reduce noise
- Pen down detection, with programmable sensitivity
- Support X, Y change function

23.2. Touch Panel Signal Description

Signal Name	Description	Type
X[2:1]	Touch Panel ADC input	AI
Y[2:1]	Touch Panel ADC input	AI

Table 23. Touch Panel Signal Description

24. Camera Sensor Interface

24.1. Overview

The Camera Sensor Interface (CSI) features:

- 8-bit input data
- Support CCIR656 protocol for NTSC and PAL
- 3 parallel data paths for image stream parsing
- Support Received data double buffer
- Parsing bayer data into planar R, G, B output to memory
- Parsing interlaced data into planar or MB Y, Cb, Cr output to memory
- Pass raw data direct to memory
- All data transmit timing can be adjusted by software
- Luminance statistical value

24.2. CSI Signal Description

Signal Name	Description	Type
CSI_PCLK	Camera Sensor Pixel Clock	I
CSI_MCLK	Camera Sensor Clock	O
CSI_HSYNC	Camera Sensor Horizontal Synchronization	I
CSI_VSYNC	Camera Sensor Verizontal Synchronization	I
CSI_D[7:0]	Camera Sensor Data Bit	I/O

Table 24. Camera sensor Signal Description

25. Universal LCD/TV Timing Controller

25.1. Overview

TCON in A13 is of high flexibility in timing configuration as well as LCD module compatibility.

25.2. LCD Signal Description

Signal Name	Description	Type
LCD_CLK	LCD RGB Pixel Clock	I/O
LCD_DE	LCD RGB Data Enable	I/O
LCD_HSYNC	LCD RGB Horizontal Synchronization	I/O
LCD_VSYNC	LCD RGB Verizontal Synchronization	I/O
LCD_Dx	LCD Pixel Data Bit x	I/O

Table 25. LCD Signal Description

26. Port Controller

26.1. Port Description

The chip has 7 ports for multi-functional input/out pins. They are:

- Port B(PB): 10input/output port
- Port C(PC): 17 input/output port
- Port D(PD): 22 input/output port
- Port E(PE): 12 input/output port
- Port F(PF): 6 input/output port
- Port G(PG): 9 input/output port

These ports can be easily configured by software for various system configurations.

27. Declaration

This A13 datasheet is the original work and copyrighted property of Allwinner Technology ("Allwinner"). Reproduction in whole or in part must obtain the written approval of Allwinner and give clear acknowledgement to the copyright owner.

The information furnished by Allwinner is believed to be accurate and reliable. Allwinner reserves the right to make changes in circuit design and/or specifications at any time without notice. Allwinner does not assume any responsibility and liability for its use. Nor for any infringements of patents or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Allwinner. This datasheet neither states nor implies warranty of any kind, including fitness for any particular application.