AS7000

Sensor System on Chip

General Description

The AS7000 device provides a flexible analog front end for light sensing applications. The photodiode input circuit can be configured in different ways to guarantee best tradeoff between speed and sensitivity for a large number of different sensing applications.

Key Features

- Single Device Integrated Optical Solution
- Analog optical front end
- Analog electrical front end
- Hardware Sequencer.
- Powerful 32bit Cortex-M0 processor
- 14 bit ADC
- Synchronous detector
- Integrated LED driver with current control
- VDD range: 2.6V to 3.6V

Applications

- Optical sensor platform

1 Block diagram

Figure 1: Application Schematic

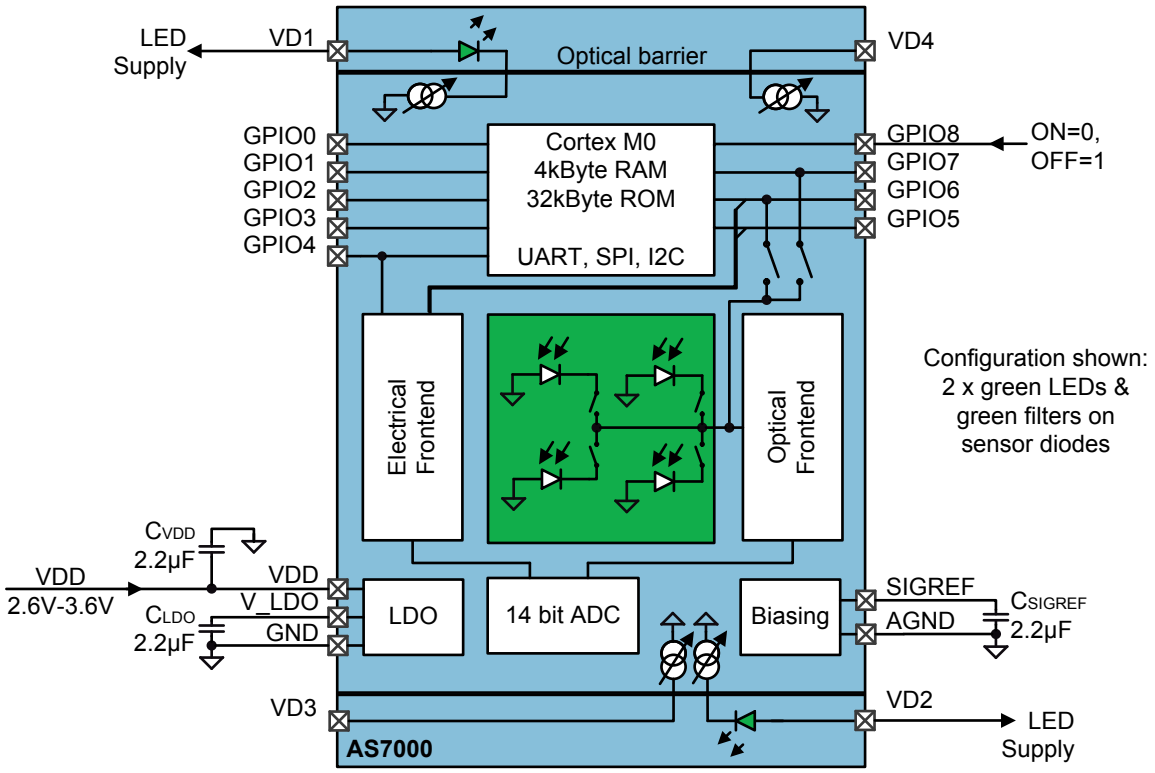


Figure 2: Cortex-M0 Block Diagram

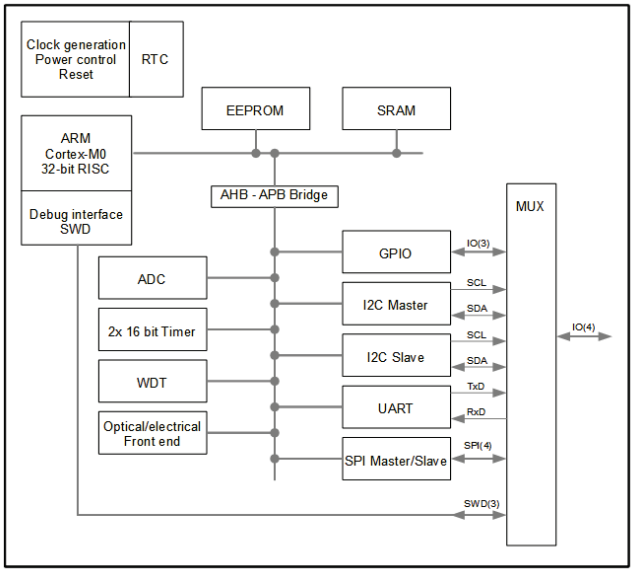


Figure 3: Measurement system with motion artefact compensation

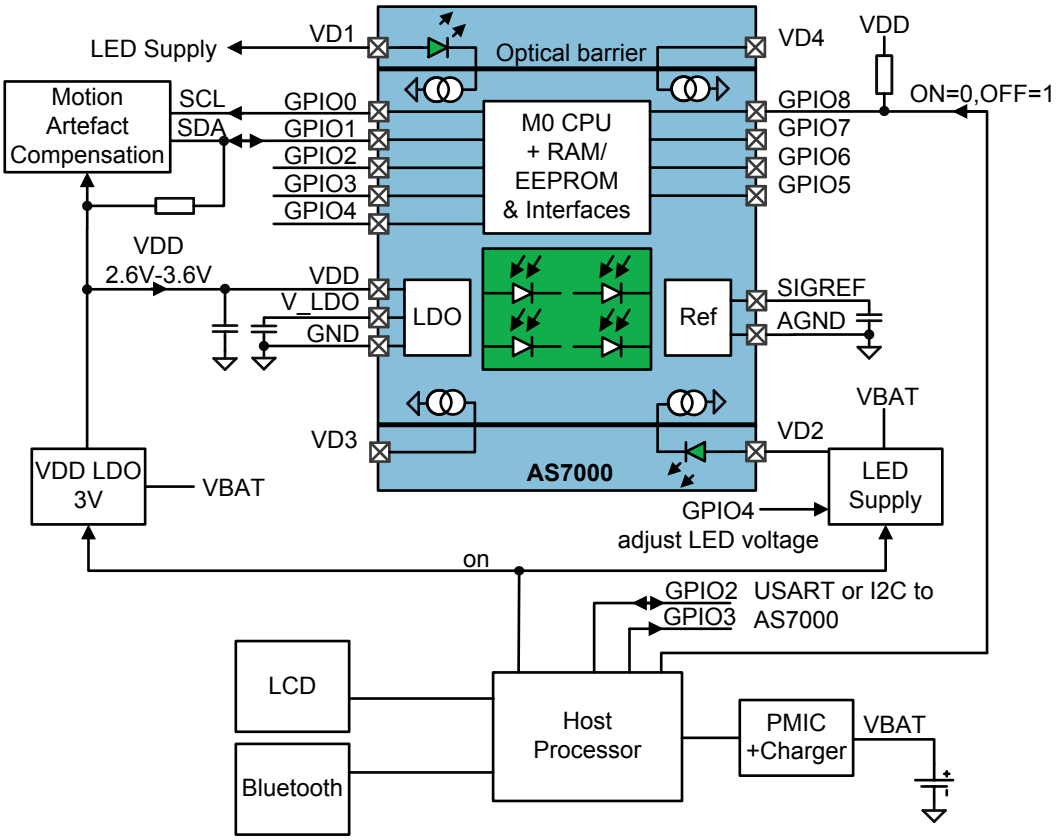


Figure 4: Typical form factor including VDD LDO

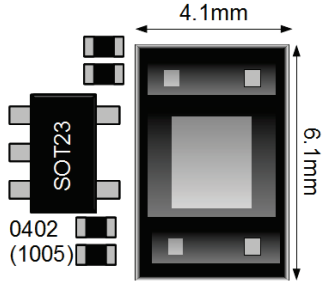
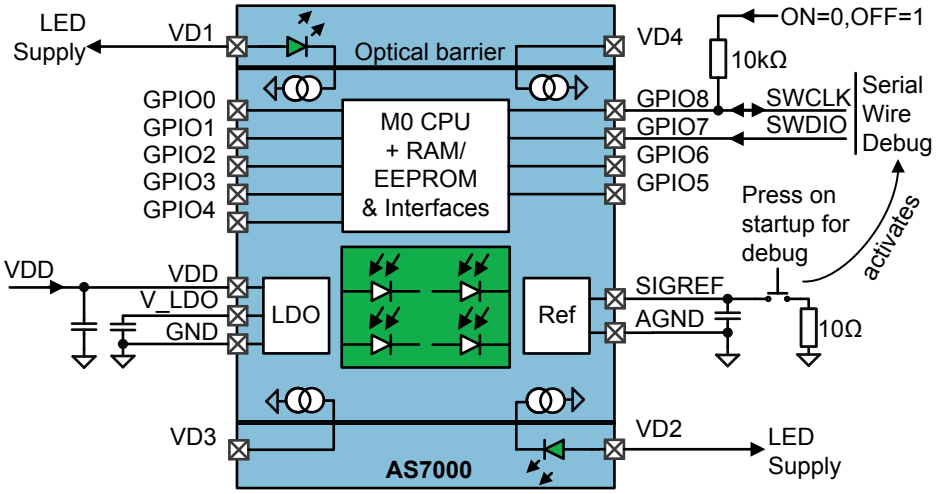


Figure 5: Program/Debug – press debug button on power-up (VDD on)



2 Pinout

Figure 6: Optical Module pinout – top view – not to scale

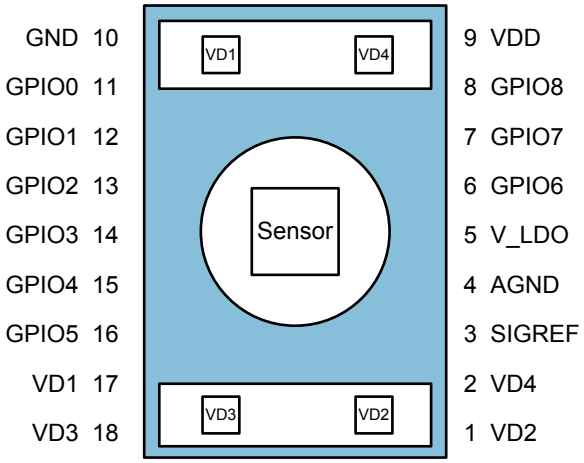


Table 1- Pin Descriptions

Pin Nr	Pin Name	Description
1	VD2	Supply voltage for LED D2
2	VD4	Supply voltage for LED D4
3	SIGREF	Analog reference output. Connect 2.2uF capacitor to GND (e.g. 0402 sized capacitor GRM153R60J225ME95 – needs to have >1uF with 1.0V voltage bias); do not load externally
4	AGND	Analog ground. Connect to low noise GND
5	V_LDO	1.8V output voltage. Connect 2.2uF capacitor to GND (e.g. 0402 sized capacitor GRM153R60J225ME95 – needs to have >1uF with 1.0V voltage bias); do not load externally
6	GPIO6	General purpose input/output
7	GPIO7	General purpose input/output
8	GPIO8	General purpose input/output
9	VDD	Supply voltage.
10	GND	Power supply ground. All voltages are referenced to GND.
11	GPIO0	General purpose input/output
12	GPIO1	General purpose input/output
13	GPIO2	General purpose input/output
14	GPIO3	General purpose input/output
15	GPIO4	General purpose input/output
16	GPIO5	General purpose input/output
17	VD1	Supply voltage for LED D1
18	VD3	Supply voltage for LED D3

3 Absolute Maximum Ratings

Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in Section “Electrical Characteristics” is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2-Absolute Maximum Ratings

Parameter	Min	Max	Unit	Note
Supply voltage, VDD		3.8 TBD	V	All voltages are with respect to GND
Input terminal voltage	−0.5	3.8 TBD	V	
Output terminal voltage	−0.5	3.8 TBD	V	
Output terminal voltage VD1, VD2,VD3,VD4	−0.5	5.5	V	
Latchup current	−100	100	mA	Norm: EIA/ JESD78
ESD tolerance, human body model	-2000	+2000	V	Norm: JEDEC JESD22-A114F, pins VDD, GND, VD3, VD4, SIGREF, AGND, V_LDO, GPIO0-8,
	-1000	+1000	V	Norm: JEDEC JESD22-A114F, Pins VD1/VD2 (LED pins)
Storage temperature range, T_{stg}	−40	85	ºC	
Moisture Sensitivity Level (MSL)	MSL 3			
Body Temperature during Soldering				See Reflow profile

4 Electrical Characteristics

VDD=2.6 to 3.6V, typ. values are at Tamb=25°C (unless otherwise specified). All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 3- General Electrical Characteristics and Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Supply voltage		2.6	3.3	3.6	V
VLED	LED Supply voltage	VD1, VD2, VD3, VD4 if a LED is used			5.0	V
T_{AMB}	Operating free-air temperature		−30		+70	°C
IDD	Supply current	CPU running at 16MHz; from 1.8V supply		2		mA
		ADC 14bit; only during conversion		2	4	mA
		Photodiode amplifier and Optical front end		420		µA
		Electrical front end		180		µA
		LED current sink per channel 25mA range		220		µA
		LED current sink per channel 50mA and 100mA range		350		µA
		LED current sink per channel 300mA range		850		µA
		Deep sleep mode[1] 512Hz oscillator running, LDO operating, processor powered		10	20	µA
		Power down[2]		0.5	1	µA
VOL	GPIO0-8 output low voltage	with 3 mA load with 6 mA load	0 0		0.4 0.8	V
VOH	GPIO0-8 output high voltage	with 6 mA load	2.4		VDD	V
VIH	GPIO0-8 input high voltage		1.25			V
VIL	GPIO0-8 input low voltage				0.54	V
ILEAK1	GPIO0-8		−1		1	µA
ILEAK2	VD1-4 pins	at TBD V	−1		1	µA
E_f16M	Tolerance of internal 16MHz oscillator		-2		+2	%
E_f3k2	Tolerance of internal 512Hz oscillator		-25		+25	%

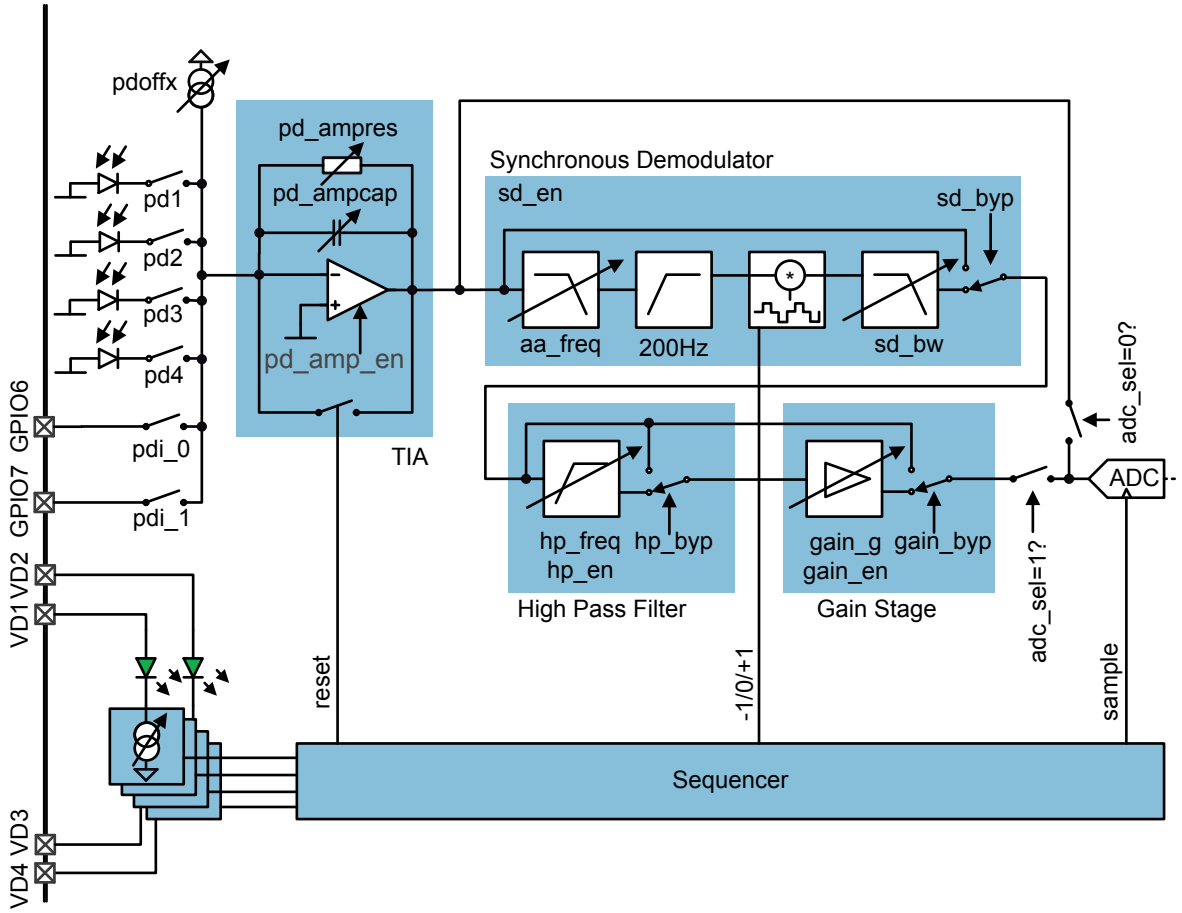
Note 1: Deep sleep mode. Entered by setting enter_sleep=1, wakeup with low on GPIO8 pin (if gpio8_wakeup_en=1) or high on GPIO7 (if gpio7_wakeup_en=1) or 512Hz oscillator sleep_timer.

Note 2: Power down mode. Entered by setting enter_powerdown=1; No oscillator running. Wakeup with low on GPIO8 pin (always) or high on GPIO7 (if gpio7_wakeup_en=1).

5 Functional description

5.1 Optical analog front end

Figure 7: Optical analog front end – dual green LED configuration shown



The number of LEDs inside the module depends on the application – above figure shows 2 LEDs. If a LED is not populated, the current sink is connected directly to the pin (VD3 and VD4 in above figure).

5.1.1 LEDs

5.1.1.1 Dual green LED configuration

Two green LEDs are used (pins VD1/VD2). The other two current sinks are available on pins VD3 and VD4.

Table 4- LED Characteristics at T_{AMB}=25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LED}	Allowed operating LED current range	continuous	0		50	mA
		1/10 duty cycle @ 1 kHz			100	mA
VF_{LED}	Forward Voltage	I_{LED}=20mA	2.9	3.2	3.9	V
λp	Dominant wavelength			527		nm
Δλ½	Spectral halfwidth			35		nm

5.1.2 LED-driver

The four LED-driver outputs can be controlled manually or by the build in sequencer. See section “Optical front end operation”

Figure 8: LED drivers – dual green LED configuration

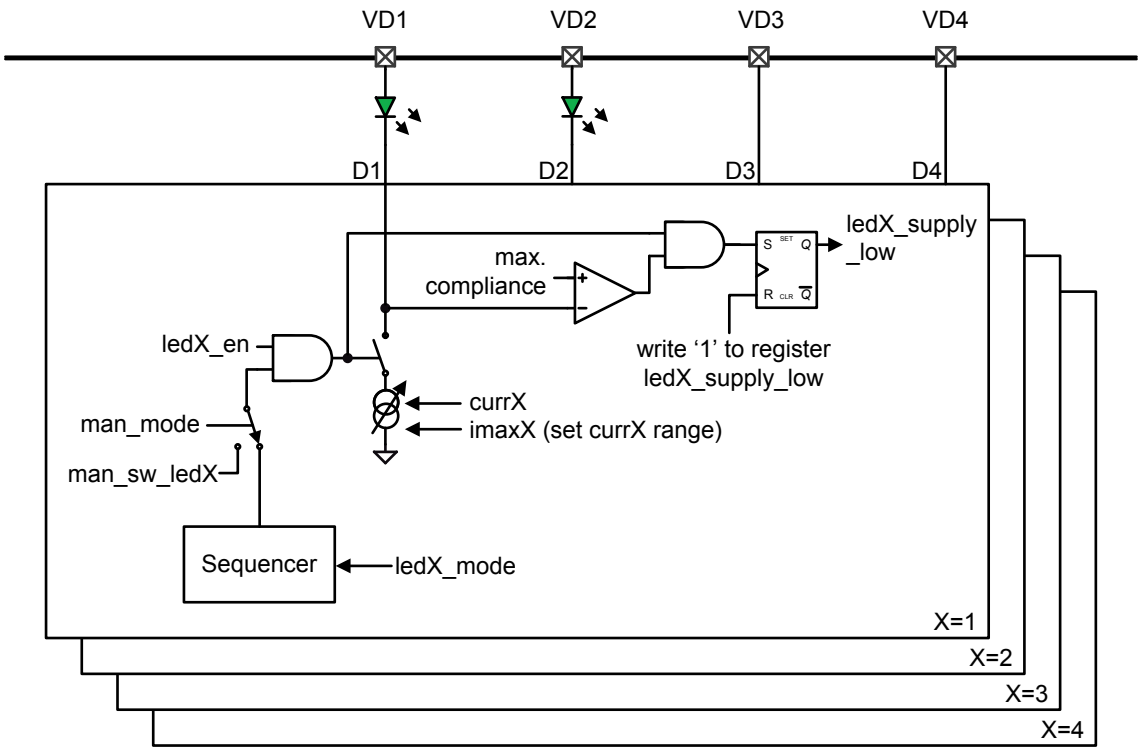


Table 5-Operating characteristics of each LED output, VDD=3V, TA=25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{LED1/2/3/4}$	LED output current range	imax1/2/3/4 = 00 imax1/2/3/4 = 01 imax1/2/3/4 = 10 imax1/2/3/4 = 11	0 0 0 0		25 50 100 300	mA mA mA mA
	tolerance		-5		5	%
V_Dmin	Output voltage compliance	D1,D2,D3,D4 @ ILED=25,50,100mA D1,D2,D3,D4 @ ILED=300mA		0.2 0.5		V V
V_Dmax	Output voltage maximum	D1,D2,D3,D4		5	5.5	V

5.1.2.1 LED Configuration Registers

0x00: AFE_LED_CFG

Field	Name	Rst	Type	Description
11	led4_en	0	RW	0...Disables LED4 output source. 1...Enables LED4 output source.
10	led3_en	0	RW	0...Disables LED3 output source. 1...Enables LED3 output source.
9	led2_en	0	RW	0...Disables LED2 output source. 1...Enables LED2 output source.
8	led1_en	0	RW	0...Disables LED1 output source. 1...Enables LED1 output source.
7:6	imax4	1	RW	Defines IMAX of LED4. Setting: 0 → IMAX: 25mA

				1 50mA 2 100mA 3 300mA
5:4	imax3	1	RW	Defines IMAX of LED3. same encoding as imax4
3:2	imax2	1	RW	Defines IMAX of LED2. same encoding as imax4
1:0	imax1	1	RW	Defines IMAX of LED1. same encoding as imax4

The LED_CFG register is used to configure the operating mode of the LED outputs.

Addr: 0x04		AFE_LED_CURR Register		
		The AFE_LED_CURR defines the LED output current.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:24	curr4	0x00	R/W	LED4 output current ILED4=curr4*imax4/255
23:16	curr3	0x00	R/W	LED3 output current ILED3=curr3*imax3/255
15:8	curr2	0x00	R/W	LED2 output current ILED2=curr2*imax2/255
7:0	curr1	0x00	R/W	LED1 output current ILED1=curr1*imax1/255

0xb0: AFE_STATUS

Field	Name	Rst	Type	Description
19	led4_supply_low	0	SS_WC[1]	If this bit is asserted, LED4 voltage has been too low.
18	led3_supply_low	0	SS_WC[1]	If this bit is asserted, LED3 voltage has been too low.
17	led2_supply_low	0	SS_WC[1]	If this bit is asserted, LED2 voltage has been too low.
16	led1_supply_low	0	SS_WC[1]	If this bit is asserted, LED1 voltage has been too low.

[1] SS_WC: Self set, write clears: These registers are set by the hardware and writing '1' to them clears them.

0x20: AFE_MAN_SEQ_CFG

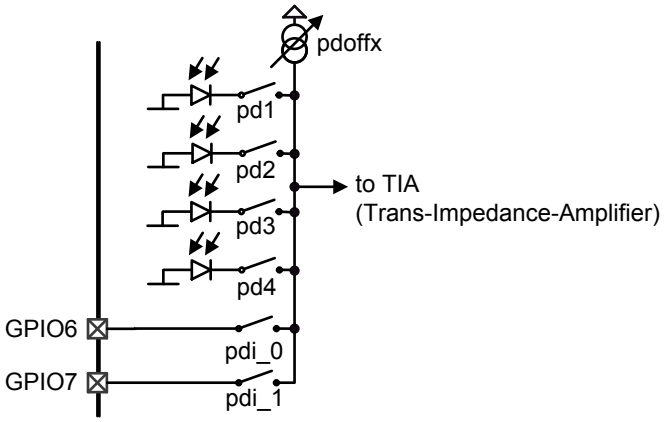
Field	Name	Rst	Type	Description
26	man_mode	0	RW	0...Enables Sequencer 1...Enables Manual control of optical front end
23	man_sw_itg	0	RW	If man_mode=1 0...All integrator capacitors are shorted. Integrator is reset 1...Integrator capacitors are charging up. Integrator is running
22	man_sw_led4	0	RW	If man_mode=1 0...LED output D4 disabled. (High impedance) 1...LED output D4 enabled
21	man_sw_led3	0	RW	If man_mode=1 0...LED output D3 disabled. (High impedance) 1...LED output D3 enabled
20	man_sw_led2	0	RW	If man_mode=1 0...LED output D2 disabled. (High impedance) 1...LED output D2 enabled
19	man_sw_led1	0	RW	If man_mode=1 0...LED output D1 disabled. (High impedance) 1...LED output D1 enabled
12:10	led4_mode	0	RW	LED4 mode

				Setting / **Behaviour** 0 Always off 1 Always on when sequencer is active 2 Controlled by sequencer 3 Controlled by sequencer, only on in even iterations: 0, 2, 4 etc. 4 Controlled by sequencer, only on in odd iterations: 1, 3, 5 etc. 5 Controlled by sequencer, only on in every fourth iteration, starting at 3: 3, 7, 11 etc.
9:7	led3_mode	0	RW	LED3 mode **Setting** / **Behaviour** 0 Always off 1 Always on when sequencer is active 2 Controlled by sequencer 3 Controlled by sequencer, only on in even iterations: 0, 2, 4 etc. 4 Controlled by sequencer, only on in odd iterations: 1, 3, 5 etc. 5 Controlled by sequencer, only on in every fourth iteration, starting at 2: 2, 6, 10 etc.
6:4	led2_mode	0	RW	LED2 mode **Setting** / **Behaviour** 0 Always off 1 Always on when sequencer is active 2 Controlled by sequencer 3 Controlled by sequencer, only on in even iterations: 0, 2, 4 etc. 4 Controlled by sequencer, only on in odd iterations: 1, 3, 5 etc. 5 Controlled by sequencer, only on in every fourth iteration, starting at 1: 1, 5, 9 etc.
3:1	led1_mode	0	RW	LED1 mode **Setting** / **Behaviour** 0 Always off 1 Always on when sequencer is active 2 Controlled by sequencer 3 Controlled by sequencer, only on in even iterations: 0, 2, 4 etc. 4 Controlled by sequencer, only on in odd iterations: 1, 3, 5 etc. 5 Controlled by sequencer, only on in every fourth iteration, starting at 1: 0, 4, 8 etc.

5.1.3 Photodiode Selection

In order to have flexible arrangement of the use photodiodes, PD1-PD4 can be individually connected to the photodiode amplifier input. The optional offset current allows cancellation of constant light sources like sunlight. In case of an external photodiode or any other sensor with (low) current output, the pins GPIO6 and GPIO7 can be used as input.

Figure 9: Photodiode selection



5.1.3.1 AFE_PD_CFG Register

Addr: 0x08		AFE_PD_CFG Register		
		The AFE_PD_CFG register is used to configure the input to the photo amplifier.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
15:8	pdoffx	0x00	R/W	Input offset current Ioffset = pdoffx*.10nA 00000000…Offset source is turned off
5	pd4	0	R/W	0…Photodiode PD4 is disconnected from photo amplifier 1…Photodiode PD4 is connected to photo amplifier
4	pd3	0	R/W	0…Photodiode PD3 is disconnected from photo amplifier 1…Photodiode PD3 is connected to photo amplifier
3	pd2	0	R/W	0…Photodiode PD2 is disconnected from photo amplifier 1…Photodiode PD2 is connected to photo amplifier
2	pd1	0	R/W	0…Photodiode PD1 is disconnected from photo amplifier 1…Photodiode PD1 is connected to photo amplifier
1	pdi_1	0	R/W	0…GPIO7-input is disconnected from photo amplifier 1…GPIO7-input is connected to photo amplifier
0	pdi_0	0	R/W	0…GPIO7-input is disconnected from photo amplifier 1…GPIO7-input is connected to photo amplifier

5.1.4 Photodiode Characteristics

Figure 10: Photodiode arrangement – orientation as in Figure 1 or Figure 6

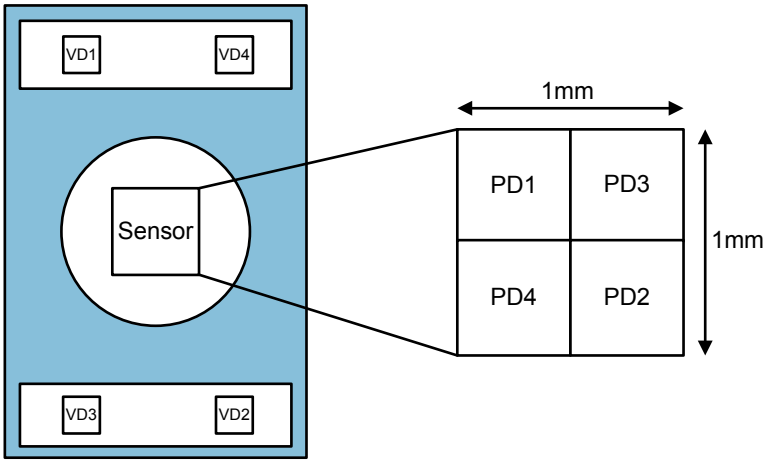
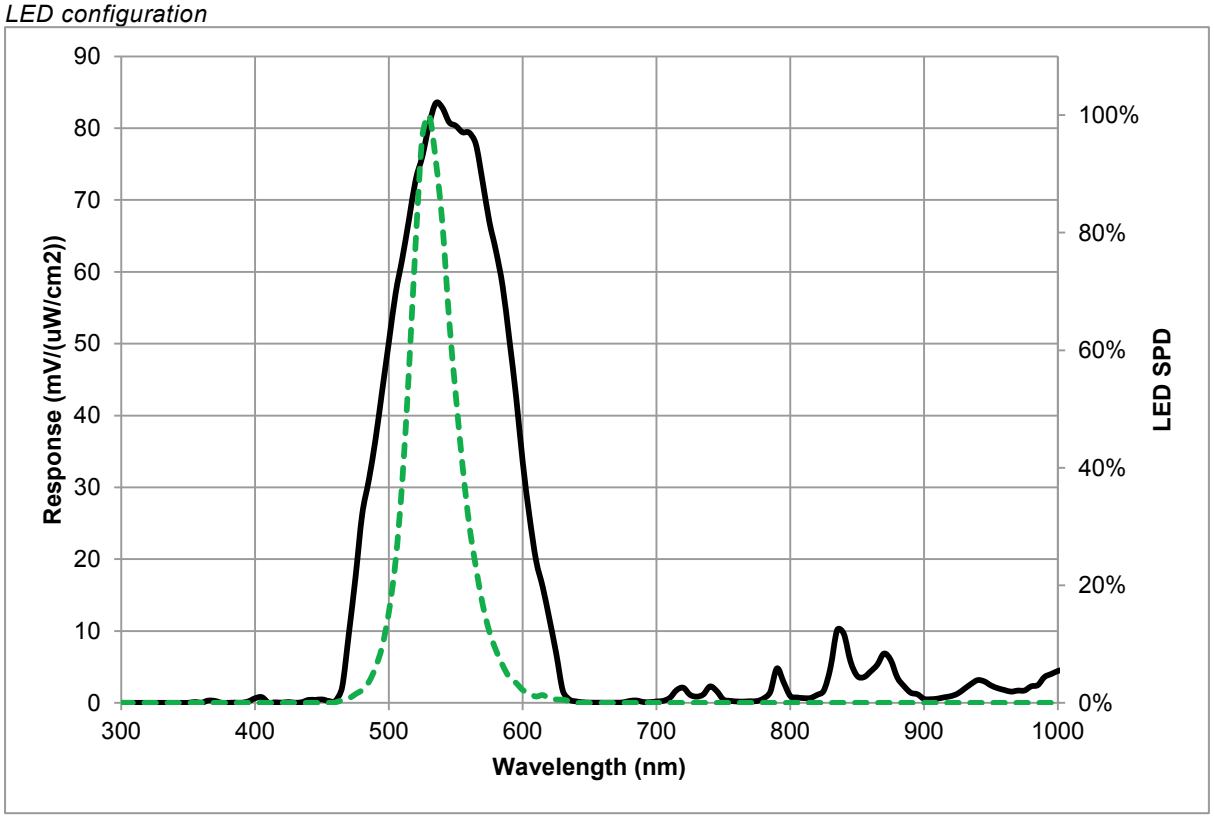


Figure 11: Photodiode sensitivity and LED emission spectrum – LEDs and filters shown for dual green LED configuration



Note: All 4 photodiodes used pd1/2/3/4=1; pd_amp_res=7MΩ, gain_g=4x, gain_en=1 measured at ADC input

Table 6-Operating characteristics of each photodiode, VDD=3V, TA=25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Re	Irradiance responsivity	λ_P=525nm, 4 photodiodes used pd1/2/3/4=1, gain_g=4x, gain_en=1, pd_ampres=7MΩ dual green LED configuration filters		76		mV/(µW /cm^2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Id	Dark current	E_e=0	0		1	nA
Ios	Extrapolated offset current		−1		1	nA

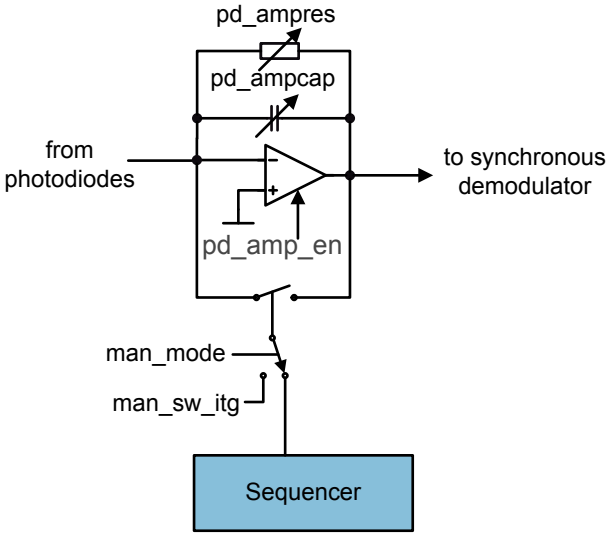
(Note: For monochromatic light *of 555nm*, one lux corresponds to 0.146 µW/cm^2. That is, one obtains 6.5 lux per µW/cm^2)

5.1.5 Photodiode Trans-Impedance Amplifier (TIA)

The photodiode amplifier can be configured in three different modes:

- Photocurrent to frequency converter
- Photocurrent to voltage converter
- Photocurrent integrator

Figure 12: Trans-Impedance-Amplifier (TIA)



The integration time t_{INT} is defined either by the sequencer (man_mode=0) of manually through the bit sw_itg if man_mode=1.

5.1.5.1 AFE_PD_AMPCFG register

Addr: 0x0c		AFE_PD_AMPCFG Register		
		The AFE_PD_AMPCFG register is used to configure the operating mode of the photo-amplifier		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31	pd_amp_en	0	R/W	0…activates power down mode of photo-amplifier 1…Enables photo-amplifier
13:10	pd_amp_vo	15	R/W	Opamp offset. Use ams device drivers – these automatically configure this register.
9:8	pd_ampcomp	3	R/W	Opamp compensation. Use ams device drivers – these automatically configure this register.

7:5	pd_ampres	0x0	R/W	Feedback resistor 000…no resistor in feedback of amplifier 001…1MΩ 010…2MΩ 011…3MΩ 100…4MΩ 101…5MΩ 110…6MΩ 111…7MΩ
4:0	pd_ampcap	0x0	R/W	Feedback capacitor – automatically set by ams device drivers for modes using pd_ampres not 000b. Capacitor = pd_ampcap*0.1pF

0x20: AFE_MAN_SEQ_CFG

Field	Name	Rst	Type	Description
26	man_mode	0	RW	0...Enables Sequencer 1...Enables Manual control of optical front end
23	man_sw_itg	0	RW	If man_mode=1 0...All integrator capacitors are shorted. Integrator is reset 1...Integrator capacitors are charging up. Integrator is running

5.1.6 Voltage mode of the photodiode amplifier

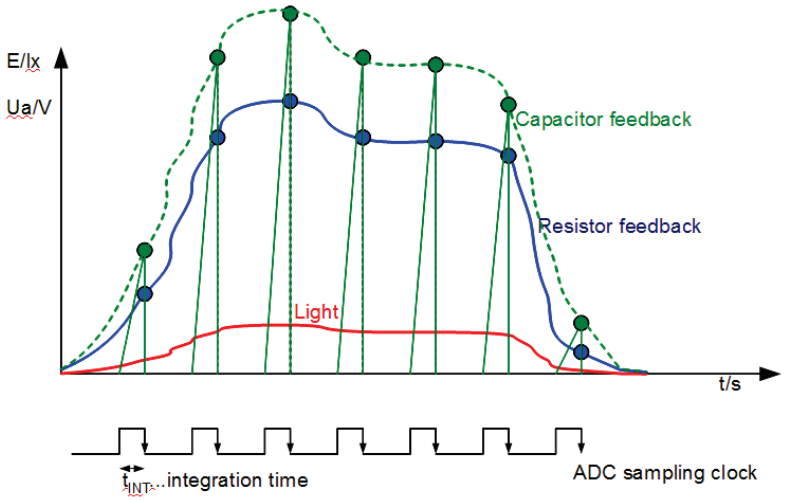
The output voltage of the photodiode amplifier is depending on the feedback component:

Feedback resistor: $$U_{out} = I_{photo} * R_{fb}$$

Feedback capacitor: $$U_{out} = I_{photo} * \frac{t_{INT}}{C_{fb}}$$

Note: The integration time t_{INT} is defined either by the sequencer (man_mode=0) of manually through the bit sw_itg if man_mode=1.
For the synchronous demodulator only use the resistive feedback.

Figure 13: Difference between resistive and capacitive feedback)

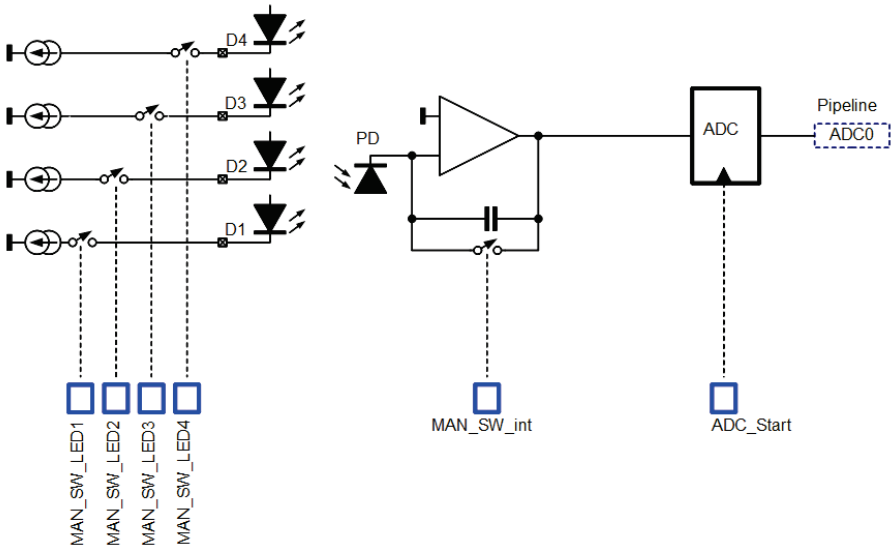


5.2 Optical front end operating modes

Once the photodiode amplifier is configured the measurement can be done in two different ways. Either the LED-outputs, the photodiode amplifier and the ADC are controlled manually by means of register bits, or they are controlled by a build in sequencer.

5.2.1 Manual operation of the optical frontend:

The optical front end can be controller via the MAN_Cfg register.



The optical front end can be controller via the MAN_Cfg register.

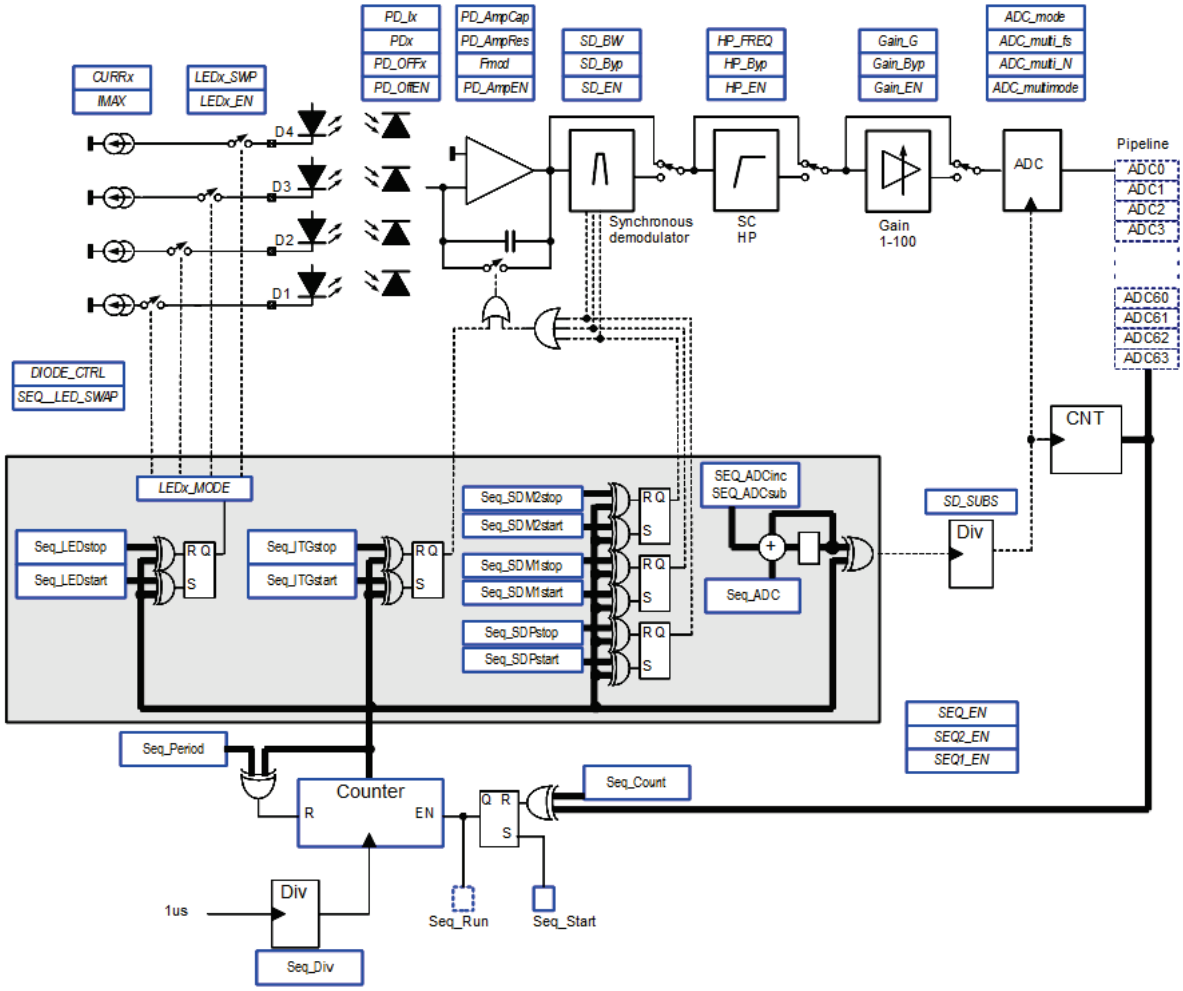
5.2.2 Sampling-sequencer:

In order to synchronize the LED-currents, the integration time and the ADC-sampling time, a build in sampling Sequencers can be used. The sequencer generates the 16 bit-timings based on the input clock t_clk. The results of the analog to digital conversion are automatically stored in a pipeline buffer.

The timings that can be programmed are:

Seq_Div:	Divider of the input clock
Seq_Count,:	Number of measurements in one sequence
Seq_Period:	Time of one measurement cycle
Seq_LEDstart:	Start time of the LED drivers
Seq_LEDstop:	Stop time of the LED drivers
Seq_ITGstart:	Start time of the integrator
Seq_ITGstop:	Stop time of the integrator
Seq_SDPstart:	Start time of the synchronous demodulators positive multiplication
Seq_SDPstop:	Stop time of the synchronous demodulators positive multiplication
Seq_SDM1start:	Start time of the synchronous demodulators negative multiplication1
Seq_SDM1stop:	Stop time of the synchronous demodulators negative multiplication1
Seq_SDM2start:	Start time of the synchronous demodulators negative multiplication2
Seq_SDM2stop:	Stop time of the synchronous demodulators negative multiplication2
Seq_ADC:	Sampling position of the ADC
Seq_ADCinc:	Increment of the sampling position of the ADC after each measurement

Note: The lowest data value of all registers except *Seq_Count* is 1



Block diagram of Sequencer

5.2.2.1 MAN_SEQ_Cfg Register

Addr: xx		MAN_SEQ_Cfg Register		
		The MAN_SEQ_Cfg register is used to configure the operation of the optical front end.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:27				Not used
26	MAN_MODE	0	R/W	0…Enables Sequencer 1… Enables Manual control of optical front end
25	MAN_SW_SDMULT(1)	0	R/W	0…disables sync.- demodulator multiplication 1…enables sync.- demodulator multiplication
24	MAN_SW_SDPOL(1)	0	R/W	0…negative polarity in sync.- demodulator multiplication 1…positive polarity in sync.- demodulator multiplication

23	MAN_SW_ITG(1)	0	R/W	0…All integrator capacitors are shorted. Integrator is reset 1…Integrator capacitors are charging up. Integrator is running
22	MAN_SW_LED4(1)	0	R/W	0…LED output D4 disabled. (High impedance) 1…LED output D4 enabled
21	MAN_SW_LED3(1)	0	R/W	0…LED output D3 disabled. (High impedance) 1…LED output D3 enabled
20	MAN_SW_LED2(1)	0	R/W	0…LED output D2 disabled. (High impedance) 1…LED output D2 enabled
19	MAN_SW_LED1(1)	0	R/W	0…LED output D1 disabled. (High impedance) 1…LED output D1 enabled
18:17	DIODE_CTRL	00		Connection of Photodiodes PD1, PD2, PD3, PD4 to the Photodiode amplifier. 00…PD1-PD4 are connected according to PD_Cfg register 01…PD1 synchronous to LED1 PD2 synchronous to LED2 PD3 synchronous to LED3 PD4 synchronous to LED4 10…PD1 synchronous to LED1 PD2 synchronous to LED1 PD3 synchronous to LED2 PD4 synchronous to LED2 11…PD1 synchronous to LED1 PD2 synchronous to LED1 PD3 synchronous to LED4 PD4 synchronous to LED4
16:15	ADC_multi_N	0	R/W	Defines number of samples that are taken in multimode (ADC_multimode =1) 00… 2 Samples 01… 4 Samples 10… 8 Samples 11…16 Samples
14	ADC_multimode	0	R/W	0…If ADC is started one sample is measured 1…If ADC is started multiple samples are measured with “ADC_multi_fs” interval and stored to memory by the DMA-controller. The number of samples is defined with “ADC_multiple”. In interleaved mode, the sampling time is 4x higher than in non-interleave mode. In non-interleave mode, if adc_multimode=0, only 1 sample is taken. In interleave mode, if adc_multimode=0, then ADC conversions are executed until the end of the sequencer period. If adc_multimode=1, then adc_multi_n is always taken into account.

13	dma_disable	0	R/W	0…ADC result(s) is/are written to memory 1…ADC result has to be read from ADC_DATA
12:10	LED4_MODE	000	R/W	000…Always OFF 001…Always ON when sequencer is active 010…Controlled by sequencer 011…Controlled by sequencer, only ON in even iterations: 0,2,4 etc. 100…Controlled by sequencer, only ON in odd iterations: 1,3,5 etc. 101…Controlled by sequencer, only ON in every fourth iteration, starting at 3: 3,7,11 etc. 110…tbd 111…tbd
9:7	LED3_MODE	000	R/W	000…Always OFF 001…Always ON when sequencer is active 010…Controlled by sequencer 011…Controlled by sequencer, only ON in even iterations: 0,2,4 etc. 100…Controlled by sequencer, only ON in odd iterations: 1,3,5 etc. 101…Controlled by sequencer, only ON in every fourth iteration, starting at 3: 3,7,11 etc. 110…tbd 111…tbd
6:4	LED2_MODE	000	R/W	000…Always OFF 001…Always ON when sequencer is active 010…Controlled by sequencer 011…Controlled by sequencer, only ON in even iterations: 0,2,4 etc. 100…Controlled by sequencer, only ON in odd iterations: 1,3,5 etc. 101…Controlled by sequencer, only ON in every fourth iteration, starting at 3: 3,7,11 etc. 110…tbd 111…tbd
3:1	LED1_MODE	000	R/W	000…Always OFF 001…Always ON when sequencer is active 010…Controlled by sequencer 011…Controlled by sequencer, only ON in even iterations: 0,2,4 etc. 100…Controlled by sequencer, only ON in odd iterations: 1,3,5 etc. 101…Controlled by sequencer, only ON in every fourth iteration, starting at 3: 3,7,11 etc. 110…tbd 111…tbd
0	SEQ_EN	0	R	0…Sequencer disabled 1…Sequencer enabled. Can be started with SEQ_Start

Note(1): function enabled only in manual mode

5.2.2.2 SEQ_Div_CNT Register

Addr: xx		Seq_Div_CNT Register		
		The SEQ_Div_CNT register sets the input divider for the main clock.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:24				Not used
23:8	SEQ_Div	0x0000	R/W	Divider value

7:0	SEQ_Count	0x00	R/W	Number of measurements in one sequence. **IF SEQ_Count = 0x00 the sequencer is running continuously.**

Sequencer time increment $t_{clk} = SEQ\_Div * 1\mu s$

5.2.2.3 SEQ_START Register

Addr: xx		Seq_START Register		
		In SEQ START register the configured sequencer can be started.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:1				Not used
0	SEQ_Start	0	R/W	1…Starts the sequencer. Sequencer is running according to the configurations in the sequencer registers

5.2.2.4 SEQ_Per Register

Addr: xx		Seq_Per Register		
		The Seq_Per register sets one measurement cycle of the sequencer.		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:16				
15:0	SEQ_Period	0x0000	R/W	T_Period

Sequencer period $T = T\_Period * SEQ\_Div * 1\mu s$

5.2.2.5 SEQ_LED Register

Addr: xx		SEQ_LED Register		
		The SEQ_LED register sets the LED drive timing. Data is stored as 16-bit value		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:16	SEQ_LEDstart	0x0000	R/W	LED start time
15:0	SEQ_LEDstop	0x0000	R/W	LED stop time

5.2.2.6 SEQ_ITG Register

Addr: xx		SEQ_ITG Register		
		The SEQ_ITG register sets the photoamplifier integration time. Data is stored as 16-bit value		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:16	SEQ_ITGstart	0x0000	R/W	Integrator start time
15:0	SEQ_ITGstop	0x0000	R/W	Integrator stop time

5.2.2.7 SEQ_SDP Register

Addr: xx		SEQ_SDP Register		
		The SEQ_SDP register sets the synchronous demodulator positive multiplication time. Data is stored as 16-bit value		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:16	SEQ_SDPstart	0x0000	R/W	multiplication start time
15:0	SEQ_SPDstop	0x0000	R/W	multiplication stop time

5.2.2.8 SEQ_SDM1 Register

Addr: xx		SEQ_SDM1 Register		
		The SEQ_SDM1 register sets the synchronous demodulator negative multiplication time1. Data is stored as 16-bit value		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:16	SEQ_SDM1start	0x0000	R/W	multiplication start time
15:0	SEQ_SPM1stop	0x0000	R/W	multiplication stop time

5.2.2.9 SEQ_SDM2 Register

Addr: xx		SEQ_SDM2 Register		
		The SEQ_SDM2 register sets the synchronous demodulator negative multiplication time2. Data is stored as 16-bit value		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:16	SEQ_SDM2start	0x0000	R/W	multiplication start time
15:0	SEQ_SPM1stop	0x0000	R/W	multiplication stop time

5.2.2.10 SEQ_ADC Register

Addr: xx	SEQ_ADC Register

		The SEQ_ADC register defines the time when the ADC starts sampling during each measurement cycle. The fraction setting permits a definition of the sampling point as a 1/16 fraction of a sequencer cycle. If seq_div=0 (1us sequencer clock), then one unit is equivalent to 62.5ns. If, e.g. seq_div=4 (5us) then the resolution of the fract register is 62.5ns*5=312.5ns		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:28	SEQ_ADC_inc_fract	0x0	R/W	ADC delay increment : SEQ_ADC_inc_fract/16 fractional
27:24	SEQ_ADC_fract	0x0	R/W	ADC start delay: SEQ_ADC_fract/16 fractional
23:16	SEQ_ADC_inc	0x00	R/W	ADC increment to the adc sample time after each conversion.
15:0	SEQ_ADC	0x0000	R/W	ADC Sampling time high

5.2.2.11 SEQ_COUNTER_ Register

Addr: xx/xx		SEQ2_COUNTER Register		
		The SEQ2_COUNTER register shows the counter value of the sequence counter and period counter		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:24	Subs_counter	0x00	R	Current subsampling counter value
23:16	Sequence_counter	0x00	R	Current sequence counter value
15:0	SEQ_COUNTER	0x0000	R	Current cycle counter value

5.2.2.12 ADC_COUNTER_ Register

Addr: xx/xx		ADC_COUNTER _Register		
		The ADC_Counter register shows the current value of the ADC counter		
Bit	**Bit Name**	**Default**	**Access**	**Description**
7:0	ADC_COUNTER	0x00	R	Current ADC counter value

5.2.2.13 ADC_DATA_ Register

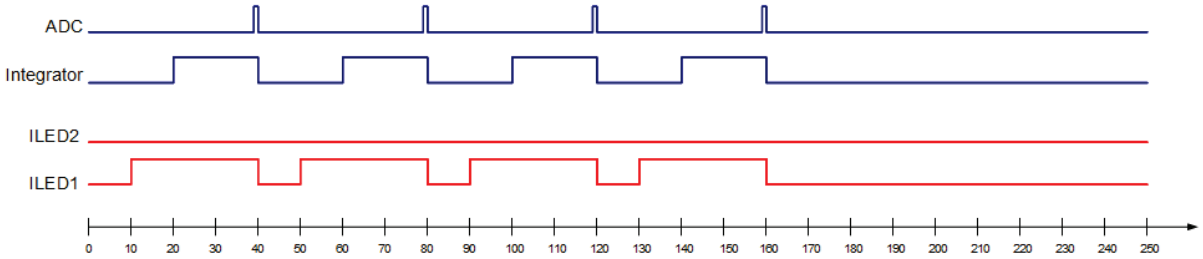
Addr: xx/xx		ADC_DATA_ Register		
		The ADC_DATA register shows the current raw output of the ADC		
Bit	**Bit Name**	**Default**	**Access**	**Description**

13:0	ADC_DATA	0x000	R	Current ADC output signals

5.2.3 Example sequencer configurations:

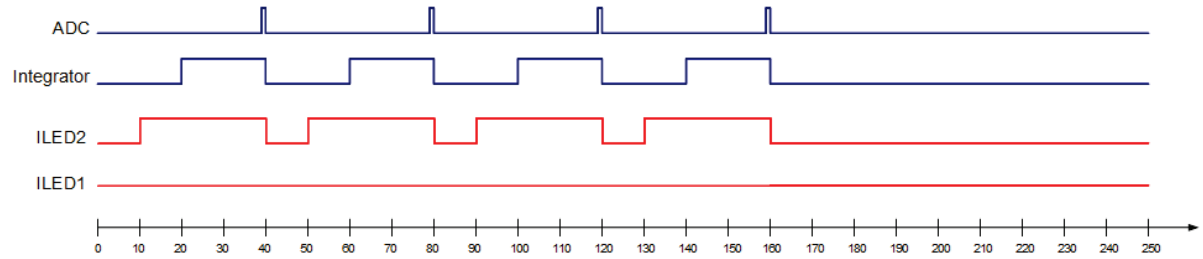
Making 4 measurements with LED1 only.
Integration time is 20 cycles. LED is turned on 10 cycles before integration starts to avoid current bouncing errors.

SEQ Period	SEQ Div	SEQ Count	SEQ LEDstart	SEQ LEDstop	SEQ ITGstart	SEQ ITGstop	SEQ ADC	SEQ ADCinc	SEQ Lmod
40	**1**	**4**	**10**	**40**	**20**	**40**	**39**	**0**	001



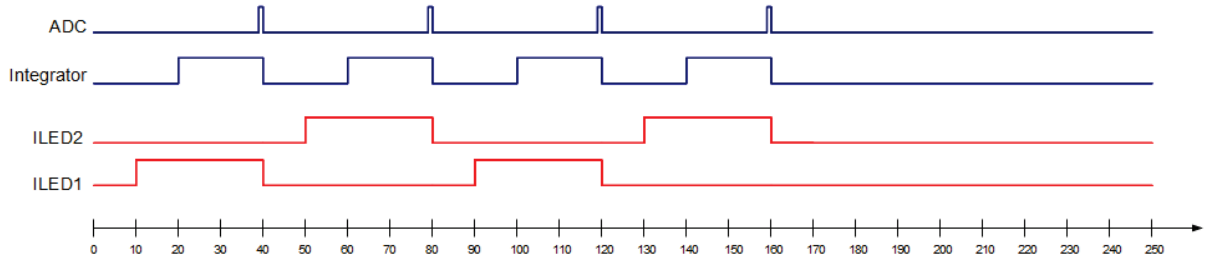
Making 4 measurements with LED2 only.
Integration time is 20 cycles. LED is turned on 10 cycles before integration starts to avoid current bouncing errors.

SEQ Period	SEQ Div	SEQ Count	SEQ LEDstart	SEQ LEDstop	SEQ ITGstart	SEQ ITGstop	SEQ ADC	SEQ ADCinc	SEQ Lmod
40	**1**	**4**	**10**	**40**	**20**	**40**	**39**	**0**	010



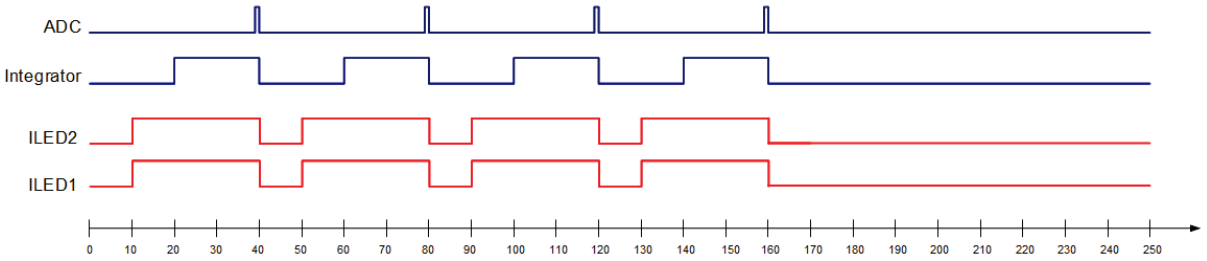
Making 4 measurements, switching between LED1 and LED2.
Integration time is 20 cycles. LED is turned on 10 cycles before integration starts to avoid current bouncing errors.

SEQ Period	SEQ Div	SEQ Count	SEQ LEDstart	SEQ LEDstop	SEQ ITGstart	SEQ ITGstop	SEQ ADC	SEQ ADCinc	SEQ Lmod
40	**1**	**4**	**10**	**40**	**20**	**40**	**39**	**0**	011



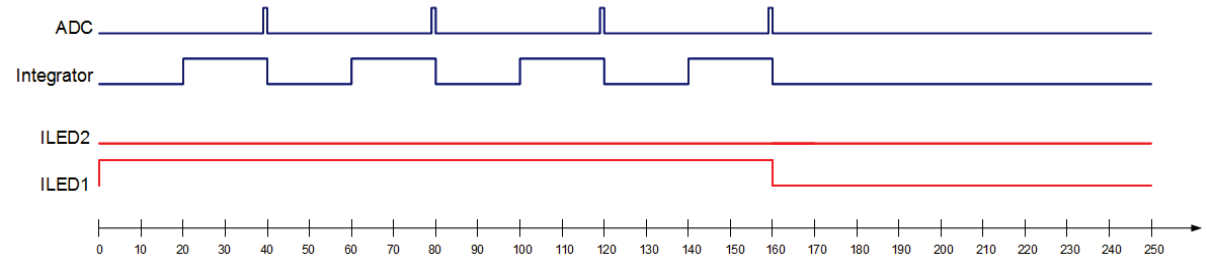
Making 4 measurements, switching LED1 and LED2 simultaneously.
Integration time is 20 cycles. LED is turned on 10 cycles before integration starts to avoid current bouncing errors.

SEQ Period	SEQ Div	SEQ Count	SEQ LEDstart	SEQ LEDstop	SEQ ITGstart	SEQ ITGstop	SEQ ADC	SEQ ADCinc	SEQ Lmod
40	**1**	**4**	**10**	**40**	**20**	**40**	**39**	**0**	100



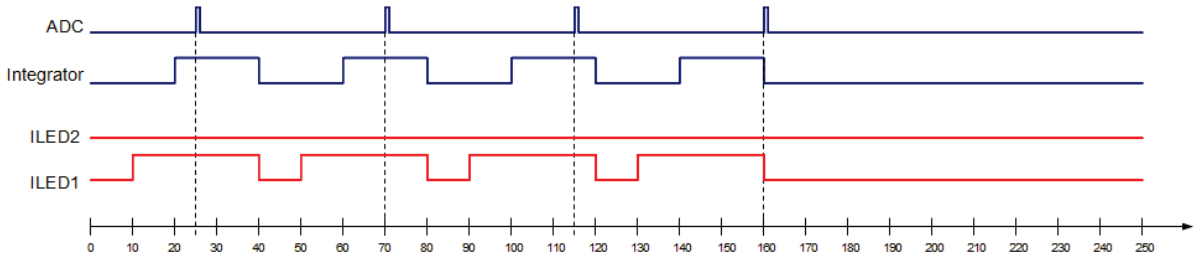
Making 4 measurements with LED1constantly on.
Integration time is 20 cycles. LED is turned on 10 cycles before integration starts to avoid current bouncing errors.

SEQ Period	SEQ Div	SEQ Count	SEQ LEDstart	SEQ LEDstop	SEQ ITGstart	SEQ ITGstop	SEQ ADC	SEQ ADCinc	SEQ Lmod
40	**1**	**4**	**10**	**40**	**20**	**40**	**39**	**0**	101



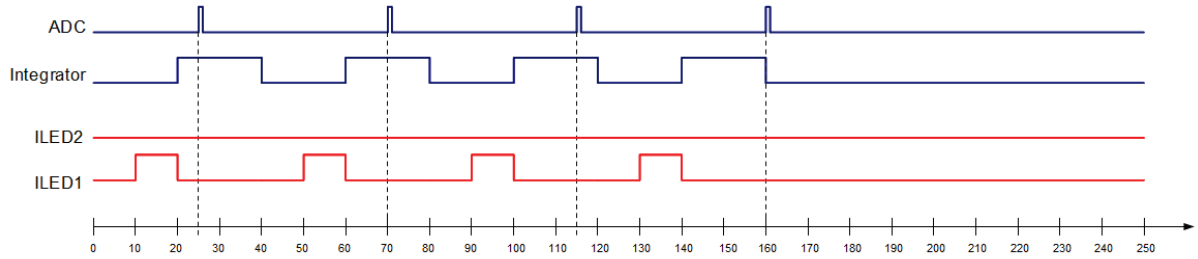
Making 4 measurements with LED1 only and subsampling.
Integration time is 20 cycles. LED is turned on 10 cycles before integration starts to avoid current bouncing errors. ADC sampling starts 5 cycles delayed every measurement.

SEQ Period	SEQ Div	SEQ Count	SEQ LEDstart	SEQ LEDstop	SEQ ITGstart	SEQ ITGstop	SEQ ADC	SEQ ADCinc	SEQ Lmod
40	**1**	**4**	**10**	**40**	**20**	**40**	**25**	**5**	001



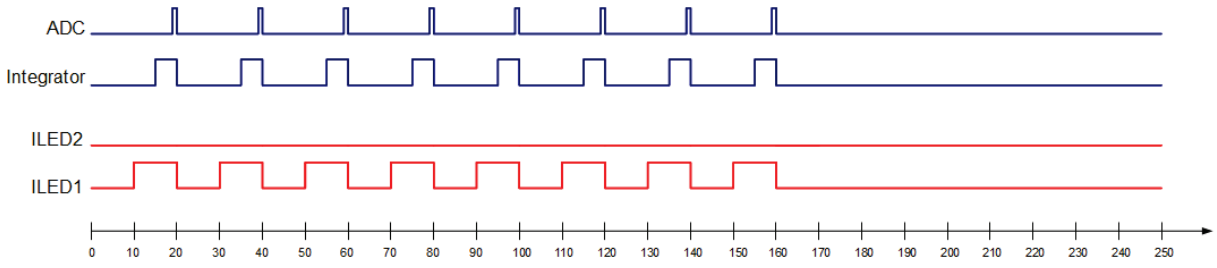
Making 4 measurements with LED1 only and subsampling.
Integration time is 20 cycles. LED is turned off 10 cycles before integration starts to measure fluorescent response of a sensor. ADC sampling starts 5 cycles delayed every measurement.

SEQ Period	SEQ Div	SEQ Count	SEQ LEDstart	SEQ LEDstop	SEQ ITGstart	SEQ ITGstop	SEQ ADC	SEQ ADCinc	SEQ Lmod
40	**1**	**4**	**10**	**20**	**20**	**40**	**25**	**5**	001



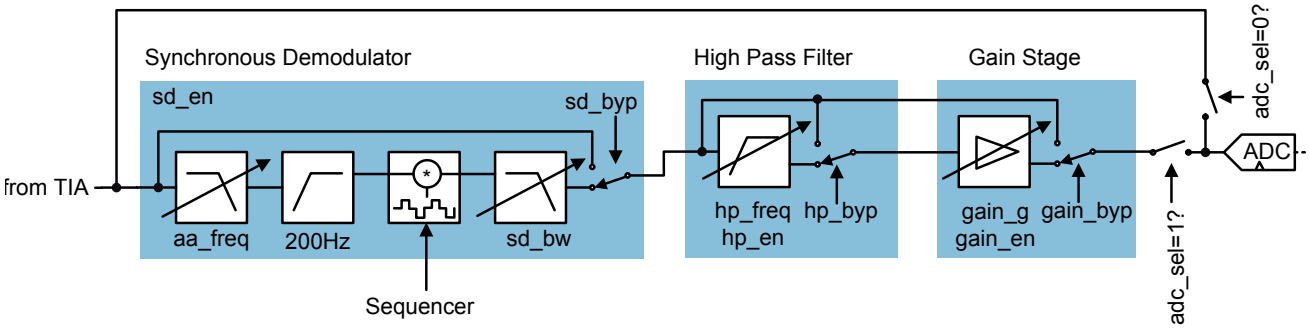
Making 8 measurements with LED1 only.
Integration time is 5 cycles. LED is turned on 5 cycles before integration starts to avoid current bouncing errors.

SEQ Period	SEQ Div	SEQ Count	SEQ LEDstart	SEQ LEDstop	SEQ ITGstart	SEQ ITGstop	SEQ ADC	SEQ ADCinc	SEQ Lmod
20	**1**	**8**	**10**	**20**	**15**	**20**	**19**	**0**	001



5.3 Optical signal conditioning

Figure 14: Optical signal conditioning



5.3.1 Synchronous demodulator:

An optional synchronous demodulator can be used to detect small optical signals in the presence of large unwanted noise (ambient light). Since the detector synchronizes to the LED frequency, the demodulator can only be used of the measurement sequencer is running.
It includes input filer (high pass at 200Hz, adjustable low pass) and an 2nd order adjustable output low pass. The demodulator itself multiplies the signal by +1 / 0 / -1 with a timing which is controlled by the sequencer.

Note: The optical signal conditioning stage need sigref_en=1 for operation.

5.3.2 High pass filter:

An optional high pass filter can be used to remove unwanted DC-components from the signal and allows further amplification. In order to guarantee fast settling times of the filter, four cutoff frequencies can be chosen.

5.3.3 Gain stage:

An optional gain stage can be used to amplify the signal after the DC-component has been removed.

5.3.4 AFE_SC_CFG Register

0x00: AFE_LED_CFG

Field	Name	Rst	Type	Description
18	sigref_en	0	RW	Signal reference: Is required for all analog blocks 0...disable signal reference 1...enable signal reference

0x70: AFE_SC_CFG

Field	Name	Rst	Type	Description
25	sd_pol_init	0	RW	The low level driver shall ensure that this register is 0 if one of the seq_sdm pulses is first, and is 1 if the seq_sdp is first within a sequence.
24:23	aa_freq	0	RW	Anti-aliasing filter cut-off frequency Setting: Signal 0: 10kHz 1: 20kHz 2: 40kHz 3: 60kHz
12:11	sd_bw	0	RW	Synchronous demodulator low pass filter. Setting: frequency 0: 10Hz 1: 20Hz 2: 40Hz 3: 80Hz

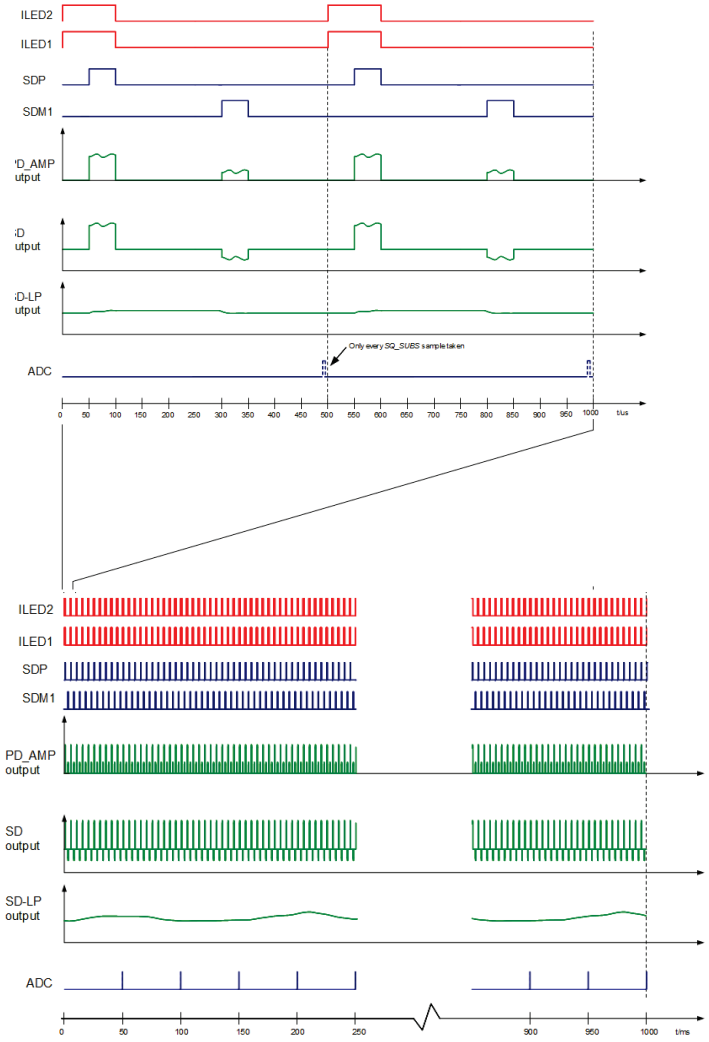
10	hp_en	0	RW	0...Power down of the high pass filter 1...Enable high pass filter
9	hp_byp	0	RW	0...HP filter is used 1...HP filter is bypassed
8:7	hp_freq	0	RW	High pass filter cutoff frequency **Setting** / **cut off frequency** 0 / 0.33Hz 1 / 1.32Hz 2 / 5.28Hz 3 / 10.56Hz
6	sd_en	0	RW	0...Power down of the Synchronous demodulator 1...Enable Synchronous demodulator
5	sd_byp	0	RW	0...Synchronous demodulator is used 1...Synchronous demodulator is bypassed
4	gain_en	0	RW	0...Power down of the Gain stage 1...Enable Gain stage
3	gain_byp	0	RW	0...Gain stage is used 1...Gain stage is bypassed
2:0	gain_g	0	RW	Gain **Setting** / **gain** 0 / 1 1 / 2 2 / 4 3 / 8 4 / 16 5 / 32 6 / 64 7 / 128

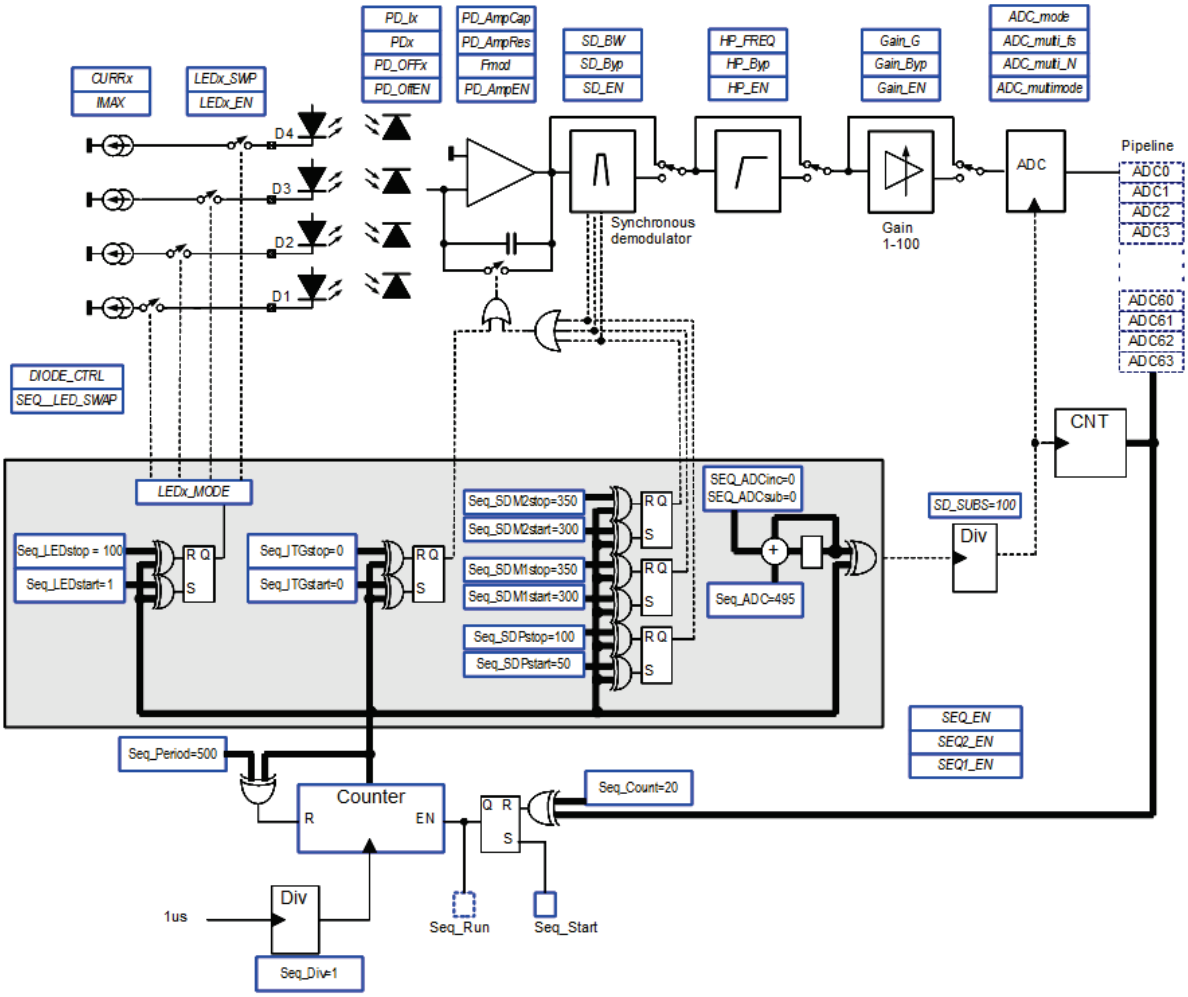
5.3.5 Sync demodulator example

LED1 and LED2 should be modulated with 2kHz
Demodulated signal should be sampled with 20Hz for 1 second.

Calculation of sequencer values:

1. Modulation Frequency = 2kHz. Period = 500us.
2. Set sequencer period to 250us.
   -> SEQ_DIV=1, SEQ_Period=500
3. Operation of LEDs beween 0us and 100us (depends on LED and Amp-settings)
   -> SEQ_LEDstart=1, SEQ_LEDstop=100
4. Operation of photo-amplifier and synchronous demodulator multipl. by +1 between 50us and 100us
   -> SEQ_SDPstart=50, SEQ_SDPstop=100
5. Operation of photo-amplifier and synchronous demodulator multipl. by -1 between 300us and 350us
   -> SEQ_SDM1start=300, SEQ_SDM2start=300, SEQ_SDM1stop=350, SEQ_SDM1stop=350
6. Sampling position at 495us
   -> SEQ_ADC=495
7. ADC should only sample at 20Hz (50ms). This means sampling at every 50ms/500us = 100th sequencer run.
   SD_SUBS=100
8. ADC values should be stored for 1 second. This means 1s/50ms = 20 samples must be stored.
   ->SEQ_Count=20

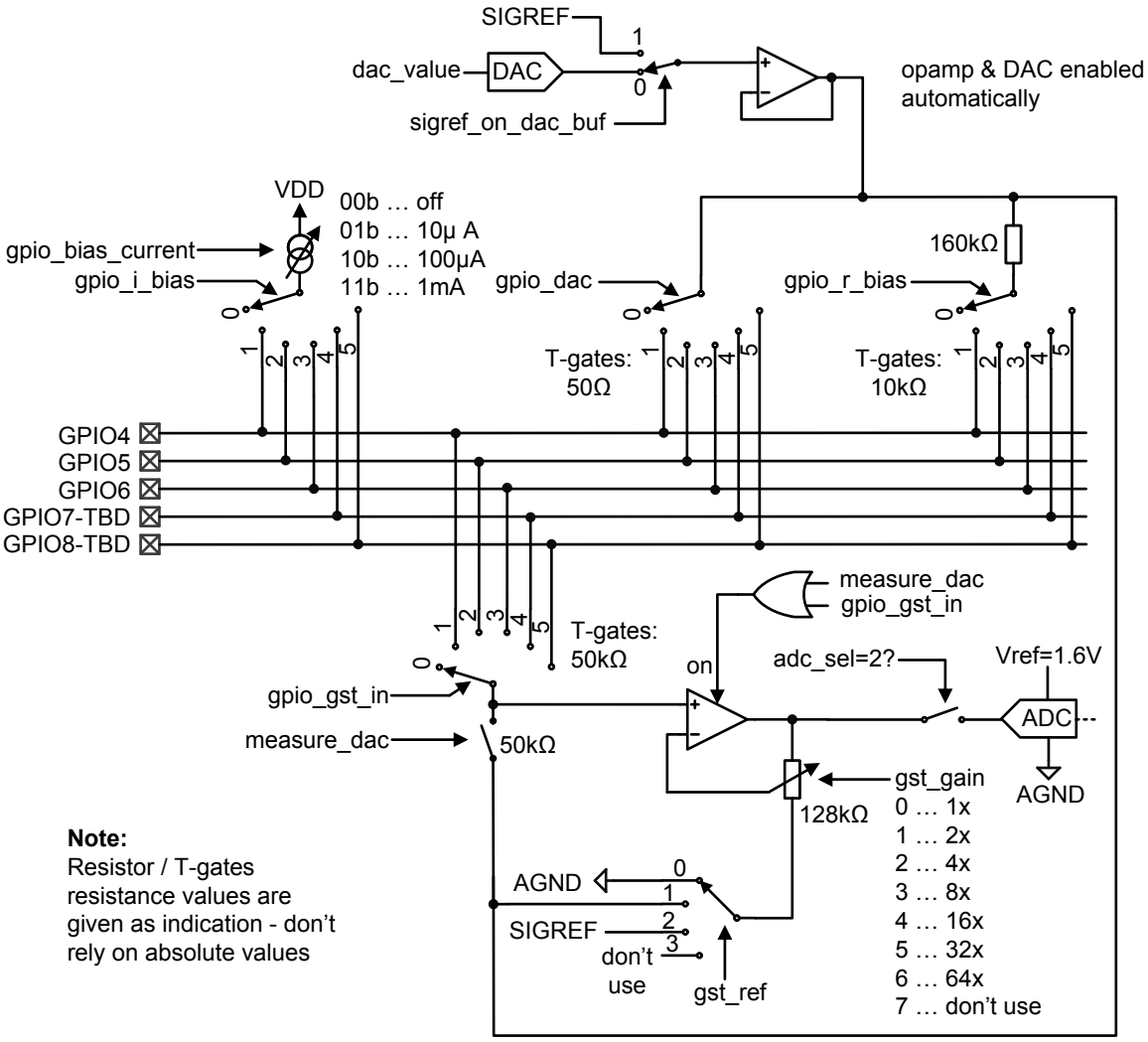

ILED2
ILED1
SDP
SDM1
'D_AMP
utput
;D
utput
;D-LP
utput
ADC
Only every SQ_SUBS sample taken
0 50 100 150 200 250 300 350 400 450 500 550 600 650 700 750 800 850 900 950 1000 t/us
ILED2
ILED1
SDP
SDM1
PD_AMP
output
SD
output
SD-LP
output
ADC
0 50 100 150 200 250 900 950 1000 t/ms


PD_Ix
PDx
PD_OFFx
PD_OffEN
PD_AmpCap
PD_AmpRes
Fmod
PD_AmpEN
SD_BW
SD_Byp
SD_EN
HP_FREQ
HP_Byp
HP_EN
Gain_G
Gain_Byp
Gain_EN
ADC_mode
ADC_muti_fs
ADC_muti_N
ADC_mutimode
CURRx
IMAX
LEDx_SWP
LEDx_EN
D4
D3
D2
D1
Synchronous demodulator
Gain 1-100
ADC
Pipeline
ADC0
ADC1
ADC2
ADC3
ADC60
ADC61
ADC62
ADC63
DIODE_CTRL
SEQ__LED_SWAP
CNT
LEDx_MODE
Seq_LEDstop = 100
Seq_LEDstart=1
Seq_JTGstop=0
Seq_JTGstart=0
Seq_SDM2stop=350
Seq_SDM2start=300
Seq_SDM1stop=350
Seq_SDM1start=300
Seq_SDPstop=100
Seq_SDPstart=50
SEQ_ADCinc=0
SEQ_ADCsub=0
Seq_ADC=495
SD_SUBS=100
Div
SEQ_EN
SEQ2_EN
SEQ1_EN
Seq_Period=500
Counter
R
EN
Seq_Count=20
1us
Div
Seq_Div=1
Seq_Run
Seq_Start

5.4 Electrical analog front end

The electrical analog front end consists of three identical signal paths with independent settings of bias condition, gain and offset.

Figure 15: Electrical analog front end internal circuit



5.4.1 Input pins

Five general purpose pins can be used either as configurable GPIO for the processor or as analog input pins for the electrical analog front end. The analog inputs can be configured to setup different amplifier topologies.

5.4.2 AFE Registers

0x00: AFE_LED_CFG

Field	Name	Rst	Type	Description
18	sigref_en	0	RW	Signal reference: Is required for all analog blocks 0...disable signal reference 1...enable signal reference

0x90: AFE_EAF

Field	Name	Rst	Type	Description
25	sigref_on_dac_buf	0	RW	If asserted, connect SIGREF to DAC buffer.

<table>
<tr><td>24</td><td>measure_dac</td><td>0</td><td>RW</td><td>If this bit is asserted, the DAC output is connected to the gain stage input (independent of gpio_gst_in selection, therefore the DAC output is measureable on the GPIO pin)</td></tr>
<tr><td>18:16</td><td>gpio_dac</td><td>0</td><td>RW</td><td>DAC on GPIO<table><tr><th>Setting</th><th>Meaning</th></tr><tr><td>0</td><td>No DAC biasing</td></tr><tr><td>1</td><td>DAC on GPIO4</td></tr><tr><td>2</td><td>DAC on GPIO5</td></tr><tr><td>3</td><td>DAC on GPIO6</td></tr><tr><td>4</td><td>DAC on GPIO7-TBD</td></tr><tr><td>5</td><td>DAC on GPIO8-TBD</td></tr></table></td></tr>
<tr><td>15:13</td><td>gpio_r_bias</td><td>0</td><td>RW</td><td>Resistive biasing<table><tr><th>Setting</th><th>Meaning</th></tr><tr><td>0</td><td>No resistive biasing</td></tr><tr><td>1</td><td>Resistive biasing on GPIO4</td></tr><tr><td>2</td><td>Resistive biasing on GPIO5</td></tr><tr><td>3</td><td>Resistive biasing on GPIO6</td></tr><tr><td>4</td><td>Resistive biasing on GPIO7-TBD</td></tr><tr><td>5</td><td>Resistive biasing on GPIO8-TBD</td></tr></table></td></tr>
<tr><td>12:10</td><td>gpio_i_bias</td><td>0</td><td>RW</td><td>Current biasing<table><tr><th>Setting</th><th>Meaning</th></tr><tr><td>0</td><td>No current biasing</td></tr><tr><td>1</td><td>Current biasing on GPIO4</td></tr><tr><td>2</td><td>Current biasing on GPIO5</td></tr><tr><td>3</td><td>Current biasing on GPIO6</td></tr><tr><td>4</td><td>Current biasing on GPIO7-TBD</td></tr><tr><td>5</td><td>Current biasing on GPIO8-TBD</td></tr></table></td></tr>
<tr><td>9:8</td><td>gpio_bias_current</td><td>0</td><td>RW</td><td>Current setting of gpio current bias<table><tr><th>Setting</th><th>Current</th></tr><tr><td>0</td><td>off</td></tr><tr><td>1</td><td>10uA</td></tr><tr><td>2</td><td>100uA</td></tr><tr><td>3</td><td>1mA</td></tr></table></td></tr>
<tr><td>7:5</td><td>gpio_gst_in</td><td>0</td><td>RW</td><td>Gain stage input selection<table><tr><th>Setting</th><th>Meaning</th></tr><tr><td>0</td><td>Not connected</td></tr><tr><td>1</td><td>GPIO4</td></tr><tr><td>2</td><td>GPIO5</td></tr><tr><td>3</td><td>GPIO6</td></tr><tr><td>4</td><td>GPIO7-TBD</td></tr><tr><td>5</td><td>GPIO8-TBD</td></tr></table></td></tr>
<tr><td>4:3</td><td>gst_ref</td><td>0</td><td>RW</td><td>Gain stage reference voltage<table><tr><th>Setting</th><th>Meaning</th></tr><tr><td>0</td><td>AGND</td></tr><tr><td>1</td><td>DAC buffer</td></tr><tr><td>2</td><td>SIGREF</td></tr><tr><td>3</td><td>Reserved – don’t use</td></tr></table></td></tr>
<tr><td>2:0</td><td>gst_gain</td><td>0</td><td>RW</td><td>Gain stage gain<table><tr><th>Setting</th><th>Meaning</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>2</td></tr><tr><td>2</td><td>4</td></tr><tr><td>3</td><td>8</td></tr><tr><td>4</td><td>16</td></tr><tr><td>5</td><td>32</td></tr></table></td></tr>
</table>

				6	64
				7	Reserved – don't use

The AFE_EAF register is used to configure the electrical frontend

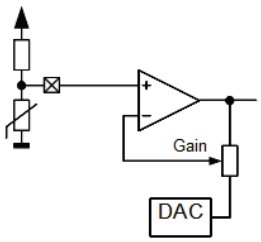
0x94: AFE_EAF_DAC

Field	Name	Rst	Type	Description
9:0	dac_value	0	RW	DAC value (10 bit)

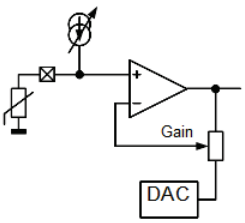
The AFE_EAF_DAC register is used to configure the dac value

5.4.3 Possible configurations of every amplifier stage:

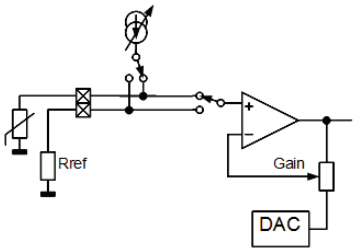
5.4.3.1 Non inverting amplifier with offset and input voltage divider. (Temperature sensor)



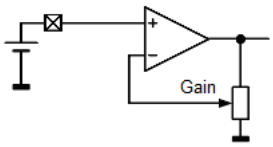
5.4.3.2 Non inverting amplifier with current source and offset. (Temperature sensor)



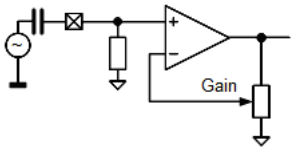
5.4.3.3 Non inverting amplifier with current source and reference path. (Temperature sensor)



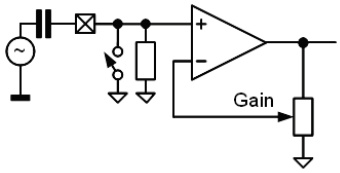
5.4.3.4 Non inverting amplifier high impedance, GND referenced.



5.4.3.5 Non inverting amplifier with DC-blocking. Referenced to V_ADCRef/2.



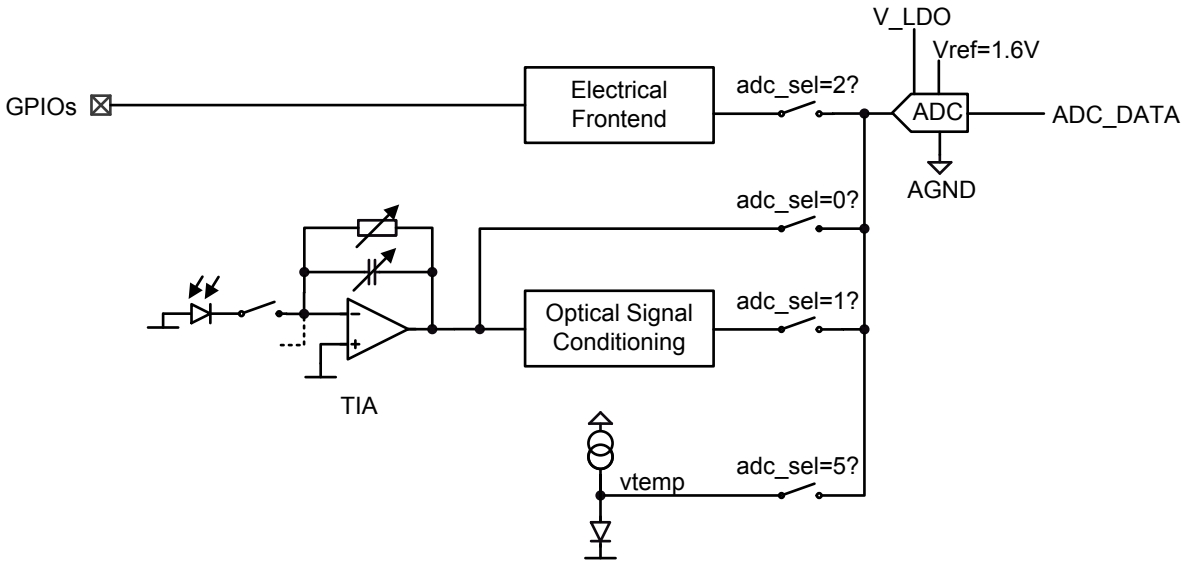
5.4.3.6 Non inverting amplifier with DC-blocking and fast settling time. Referenced to ADCRef /2.



5.5 ADC

The ADC is a 14bit successive-approximation register (SAR) type. It supports 12 bit with very fast conversion time up to 1Msps and 12bit with moderate conversion time up to 10ksps.

Figure 16: ADC Internal Circuit and multiplexer

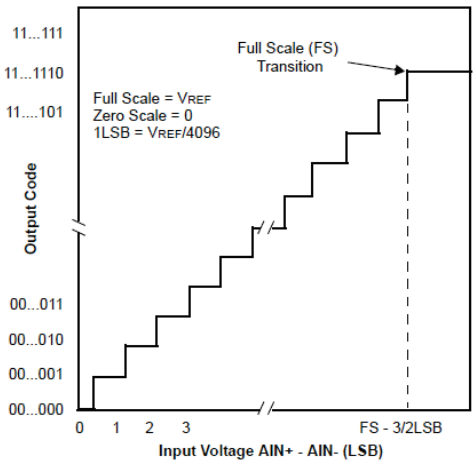


For best accuracy the ADC needs to recalibrate itself – use ams SDK to initiate the calibration procedure.

Table 7-Operating characteristics of the ADC, VDD=3V, TA=25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vref	Reference voltage V_ADCRef		TBD	1.6	TBD	V
TCvref	Reference voltage temperature coefficient			±50		ppm/°C
	Resolution	Fsample < 250kHz Fsample >= 250kHz	14 12			Bit Bit
INL	Relative accuracy		-8		8	LSB
DNL	Differential Nonlinearity		-2		2	LSB
	Offset error		-8		8	LSB
	Gain error		-8		8	LSB
SNR	Signal-to-noise ratio	Fsample = 1kHz, Fsignal=100Hz		80		dB
THD	Total harmonic distortion	Fsample = 1kHz, Fsignal=100Hz		-70		dB
Tconv	Conversion rate	12 bit resolution	1			µs
Vin	Input voltage range		0		Vref	V

Figure 17: ADC output codes



5.5.1 ADC Registers

0x88: AFE_ADC_DATA

Field	Name	Rst	Type	Description
13:0	adc_data	0	RO	current ADC output signals

The ADC_DATA register shows the current raw output of the ADC.

0xa4: AFE_ADC_CFG

Field	Name	Rst	Type	Description
19:17	adc_settling_time	5	RW	ADC settling time: Use with synchronous demodulator, and not in interleaved mode. It defines the number of ADC clock cycles the sampling window is kept open additionally. If the gain stage in the optical frontend is used (gain_byp=0), set this to minimum 8us. If adc_selfpd=1, set this to minimum 64us.

setting	periods	us (@4MHz)	us (@2MHz)	us (@1MHz)
0	0	0	0	0

				1 4 1 2 4 2 8 2 4 8 3 16 4 8 16 4 32 8 16 32 5 64 16 32 64 6 128 32 64 128 7 256 64 128 256
15:12	adc_clock	7	RW	ADC clock divider: The ADC clock is freely configurable. Note that values other 4MHz, 2MHz, 1MHz and 500kHz will make the resulting timing very confusing for the human observer. **setting Periods ns kHz** 0 2 125 8000 1 4 250 4000 2 6 375 2666 3 8 500 2000 4 10 625 1600 5 12 750 1333 6 14 875 1142 7 16 1000 1000 8 18 1125 888 9 20 1250 800 10 22 1375 727 11 24 1500 666 12 26 1625 615 13 28 1750 571 14 30 1875 533 15 32 2000 500
11	adc_calibration	0	RW	to activate self calibration, this bit must be asserted, and an ADC "conversion" has to be started in manual mode (man_mode=1) by asserting seq_start. It is suggested to let the CPU sleep and wait for the ADC interrupt. Also, a slow ADC clock should be used.
10	adc_interleave	0	RW	interleave mode
9	adc_en	0	RW	0...reset ADC 1...enable ADC Warning: In reset state the ADC clears its calibration data. Re-calibration is necessary next time it is enabled again.
8:6	adc_sel	0	RW	ADC Input Select 0… trans impedance amplifier – see Figure 7 1… optical frontend – see Figure 7 2… electrical front end – see Figure 14 3… don't use 4… don't use 5… temperature sensor (diode with approx. -2mV/K) 6… don't use 7… don't use
4	adc_highres	1	RW	ADC resolution depending on the Sampling speed **setting selection** 0 12 bit 1 14 bit
3:1	adc_multi_n	0	RW	Defines number of samples that are taken in multimode (adc_multimode =1) **Setting sample period** 0 2 1 4

				2 8 3 16 4 32 5 48 6 64 7 96
0	adc_multimode	0	RW	0...If ADC is started one sample is measured 1...If ADC is started multiple samples are measured with "adc_multi_fs" interval and stored to memory by the DMA controller. The number of samples is defined with adc_multi_n. In interleaved mode, the sampling time is 4x higher than in non-interleave mode. In non-interleave mode, if adc_multimode=0, only 1 sample is taken. In interleave mode, if adc_multimode=0, then ADC conversions are executed until the end of the sequencer period. If adc_multimode=1, then adc_multi_n is always taken into account.

5.6 Power management and operating modes

After the supply (VDD) is asserted the AS7000 automatically starts up. It is up to the application software into which operating mode the AS7000 is changed (e.g. to power down mode).
The AS7000 can operate in following modes:

Table 8 - AS7000 operating modes

Mode	Internal LDO (V_LDO)	512Hz oscillator	16MHz oscillator	CPU	Wake up CPU to active mode by	Entered by
Active	✓	✓	✓	Running	-	-
Sleep mode	✓	✓	✓	Idle	Any Interrupt (any. timer, GPIO)	__WFI() command of CPU
Deep sleep mode	✓	✓	✗	✗ = reset	512Hz sleep_counter, GPIO7[1] and GPIO8[2]	enter_sleep=1
Power down	✗	✗	✗	✗ = reset	GPIO7[1] and GPIO8[3]	enter_powerdown=1

Notes:

1) Wakeup by GPIO7=high if gpio7_wakeup_en=1; applies for power down and deep sleep mode.
2) Wakeup by GPIO8=low if gpio8_wakeup_en=1.
3) In power down mode the AS7000 will always wakeup if GPIO8=low independent of previous setting of gpio8_wakeup_en.

For operation of the sequencer the 16MHz oscillator is required, therefore the sequencer only operates in active or wait for interrupt mode.

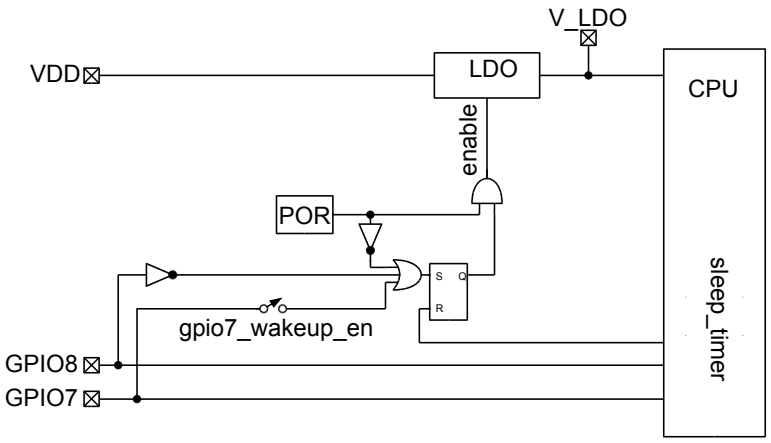
5.6.1 Clock Control Unit (CCU) for peripheral blocks

All peripheral block have a reset bit and a clock enable bit. The purpose of these register bits is to disable clock to them when they are not used and therefore reduce power consumption.

Note: Access to the register is not possible if the clock to the peripheral is disabled or reset is asserted.
e.g. to access any register of AFE (like optical analog front end) set the register bits afe_resetn=1 and afe_enable=1.

5.6.2 Wake up from power down mode

Figure 18: Wakeup logic from power down mode



5.6.3 Power management and operating modes registers

0x00: CCU_DEVICEID

Field	Name	Rst	Type	Description
31:16	device_id	0	RO	reads back 0x1b58 (decimal 7000) ("AS7000")
3:0	revision	0	RO	reads back the silicon revision

0x20: CCU_GPIO

Field	Name	Rst	Type	Description
0	gpio_resetn	0	RW	0=reset 1=running
1	gpio_enable	0	RW	0=clock off 1=clock on

0x24: CCU_SPIM

Field	Name	Rst	Type	Description
0	spim_resetn	0	RW	0=reset 1=running
1	spim_enable	0	RW	0=clock off 1=clock on

0x28: CCU_SPIS

Field	Name	Rst	Type	Description
0	spis_resetn	0	RW	0=reset 1=running
1	spis_enable	0	RW	0=clock off 1=clock on

0x2c: CCU_I2CM

Field	Name	Rst	Type	Description
0	i2cm_resetn	0	RW	0=reset 1=running
1	i2cm_enable	0	RW	0=clock off 1=clock on

0x30: CCU_I2CS

Field	Name	Rst	Type	Description
0	i2cs_resetn	0	RW	0=reset 1=running
1	i2cs_enable	0	RW	0=clock off 1=clock on

0x34: CCU_UART

Field	Name	Rst	Type	Description
0	uart_resetn	0	RW	0=reset 1=running
1	uart_enable	0	RW	0=clock off 1=clock on

0x38: CCU_TMR

Field	Name	Rst	Type	Description
0	tmr_resetn	0	RW	0=reset 1=running
1	tmr_enable	0	RW	0=clock off 1=clock on

0x3c: CCU_AFE

Field	Name	Rst	Type	Description
0	afe_resetn	0	RW	0=reset 1=running
1	afe_enable	0	RW	0=clock off 1=clock on

0x40: CCU_WD_CTRL

Field	Name	Rst	Type	Description
0	wd_en	0	RW	enable watchdog timer
1	wd_irq_msk	0	RW	if 1, pass wd_irq to system NMI input
2	wd_reset_msk	0	RW	if 1, then reset system in case of wd_reset

0x44: CCU_WD_STATUS

Field	Name	Rst	Type	Description
0	wd_irq	0	SS_WC	watchdog timer has reached interrupt level
1	wd_reset	0	SS_WC	watchdog has reached zero
2	wd_irq_intr	0	RO	NMI is currently asserted by watchdog

0x48: CCU_WD_VAL

Field	Name	Rst	Type	Description
23:0	wd_value	0	R_PUSH	Reload the watchdog counter with this value. The watchdog counter counts down, and it triggers a system reset as soon as it reaches zero.

0x4c: CCU_WD_IRQVAL

Field	Name	Rst	Type	Description
23:0	wd_irq_value	0	RW	If the watchdog counter reached this value, it will trigger an NMI as an early warning, if wd_irq_msk is set.

0x60: CCU_LP_CFG

Field	Name	Rst	Type	Description
15:0	sleep_counter	0	RW	when going into low power sleep, this the sleep counter start value. As soon as it reaches zero, the CPU will wake up (if wakeup_by_counter is set)
16	gpio7_wakeup_en	0	RW	if asserted, setting GPIO7 to high can wake up the chip as well (from both sleep and powerdown)
17	gpio8_wakeup_en	0	RW	if asserted, setting GPIO8 to low can wake up the chip from deep sleep (GPIO8=low always wakes up from powerdown)

The CCU_LP registers controls the low power modes

0x64: CCU_LP_CTRL

Field	Name	Rst	Type	Description
0	enter_sleep	0	W	writing a 1 here makes the system enter sleep mode (wakeup by counter reaching zero)
1	enter_powerdown	0	W	writing a 1 here makes the system enter power down mode (wakeup by GPIO)

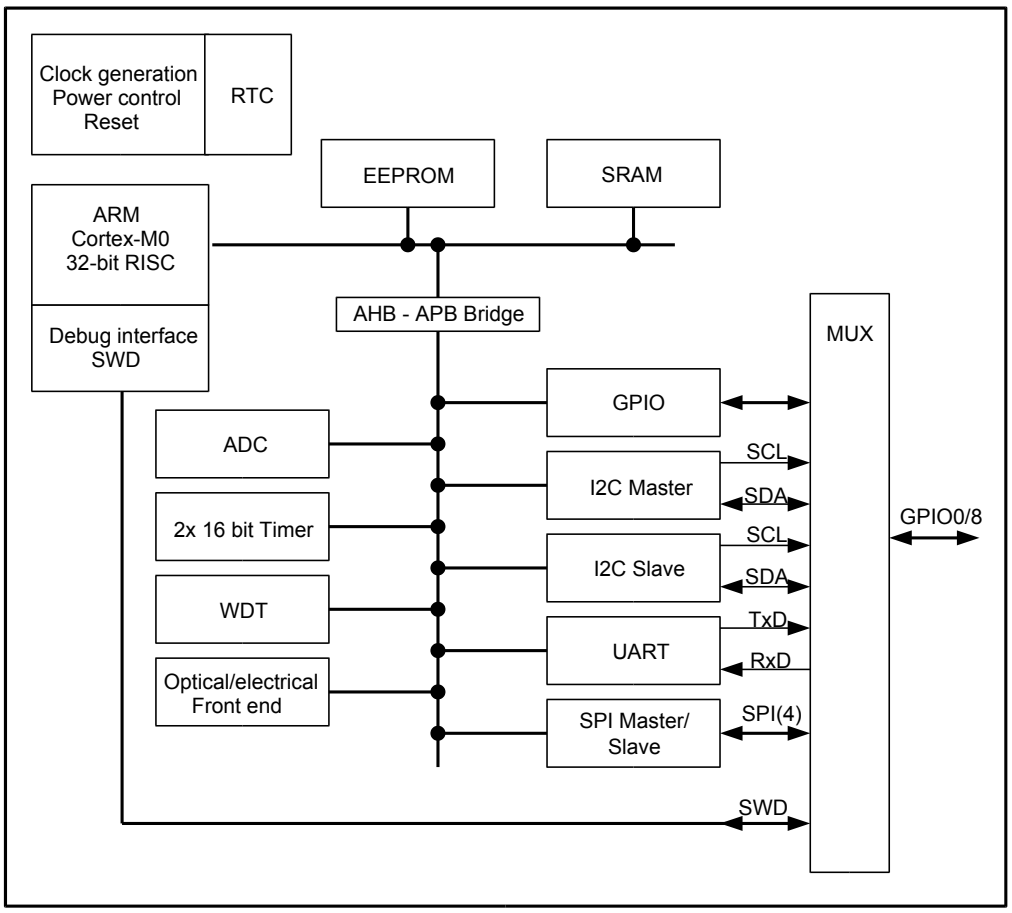
5.7 MCU

The MCU is a 32-bit ARM Cortex-M0-based RISC processor with 32kB of EEPROM memory and 4kB of RAM data memory. Details of the core processor can be found under http://infocenter.arm.com .

The MCU offers the following features:

- System:
  - ARM Cortex M0 processor
  - System tick timer
  - Hardware protection to disable the read or read/write of the internal EEPROM and SRAM
  - Unique ID for every device delivered
- Memory:
  - 32kByte EEPROM memory
  - 4kByte RAM
- Peripherals:
  - 9 general-purpose (GPIO) pins with configurable output structure
  - SPI Master/Slave
  - UART
  - I2C Master
  - I2C Slave
  - 14 bit ADC
  - Watchdog timer
  - 2 general purpose 16 bit timer
- Clock:
  - Internal 16MHz RC oscillator
  - Internal 512Hz watchdog oscillator and timer
- Debug:
  - Serial wire Debug
- Power control:
  - Reduced power modes Sleep, Stop
  - Power on reset

Figure 19: CPU internal block diagram



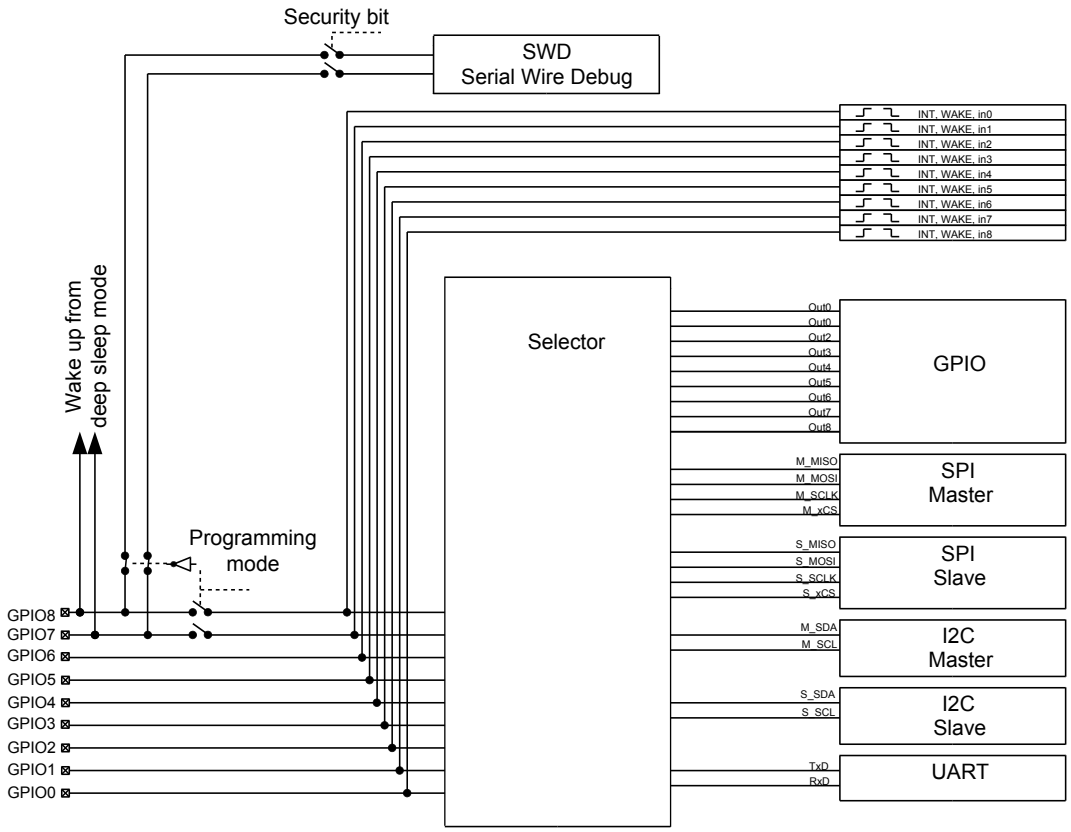
ams delivers a SDK (Software Development Kit) for easy access of the internal digital and analog blocks. The SDK includes detailed documentation of the hardware (like SPI, I2C) and includes low level drivers.

5.7.1 Debug – SWD

During power up of the AS7000 the device checks if the pin SIGREF is shorted to GND (e.g. by a resistance of 10Ω) – see Figure 5. If this condition is detected and the security bit is not set, a monitor mode is entered.
In this monitor mode the AS7000 waits 5s where a debugger can be connected. If the 5s expire without a debugger connected, the AS7000 continues startup.
If a debugger is connected, the debugger can control AS7000 as required.

5.7.2 Output switch matrix

Figure 20: Output switch matrix



Interface	GPIO Input only	GPIO output	SPI Master	SPI Slave	I2C Master	I2C Slave	UART	Analog
GPIOx_SEL	*000*	*001*	*010*	*011*	*100*	*101*	*110*	*111*
GPIO0	In0	Out0	M_MISO	S_MISO	M_SDA	S_SDA	TxD	Ana0
GPIO1	In1	Out1	M_MOSI	S_MOSI	M_SCL	S_SCL	RxD	Ana1
GPIO2	In2	Out2	M_SCK	S_SCK	M_SDA	S_SDA	TxD	Ana2
GPIO3	In3	Out3	M_xCS	S_xCS	M_SCL	S_SCL	RxD	Ana3
GPIO4	In4	Out4	M_MISO	S_MISO	M_SDA	S_SDA	TxD	Ana4
GPIO5	In5	Out5	M_MOSI	S_MOSI	M_SCL	S_SCL	RxD	Ana5
GPIO6	In6	Out6	M_SCK	S_SCK	M_SDA	S_SDA	TxD	Ana6
GPIO7	In7	Out7	M_xCS	S_xCS	M_SCL	S_SCL	RxD	Ana7
GPIO8	In8	Out8	M_MISO	S_MISO	M_SDA	S_SDA	TxD	Ana8

Configuration of interface selector

5.7.3 CPU_Cfg Register

Addr: xx		CPU_Cfg Register		
		The CPU_Cfg register is used to configure the CPU and its periphery		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:29			R/W	Not used
28:27	OTP_SEL	00	R/W	Select OTP configuration 00…normal configuration. Front ends are controlled by CPU 01…Direct access to Analog front end 10…Access to analog front end via SPI interface 11…
26:24	GPIO8_SEL	000	R/W	Configuration of the selector block for GPIO8 according to table "*Configuration of interface selector*".
23:21	GPIO7_SEL	000	R/W	Configuration of the selector block for GPIO7 according to table "*Configuration of interface selector*".
20:18	GPIO6_SEL	000	R/W	Configuration of the selector block for GPIO6 according to table "*Configuration of interface selector*".
17:15	GPIO5_SEL	000	R/W	Configuration of the selector block for GPIO5 according to table "*Configuration of interface selector*".
14:12	GPIO4_SEL	000	R/W	Configuration of the selector block for GPIO4 according to table "*Configuration of interface selector*".
11:9	GPIO3_SEL	000	R/W	Configuration of the selector block for GPIO3 according to table "*Configuration of interface selector*".
8:6	GPIO2_SEL	000	R/W	Configuration of the selector block for GPIO2 according to table "*Configuration of interface selector*".
5:3	GPIO1_SEL	000	R/W	Configuration of the selector block for GPIO1 according to table "*Configuration of interface selector*".
2:0	GPIO0_SEL	000	R/W	Configuration of the selector block for GPIO0 according to table "*Configuration of interface selector*".

5.7.3.1 GPIO_Cfg Register

Addr: xx		GPIO_Cfg Register		
		The PIO_Cfg register is used to configure the inputs of the GPIO ports		
Bit	**Bit Name**	**Default**	**Access**	**Description**
31:9			R/W	Not used
8	INT_SLOPE8	0	R/W	GPIO8 interrupt on 0… falling edge 1…rising edge
7	INT_SLOPE7	0	R/W	GPIO7 interrupt on 0… falling edge 1…rising edge
6	INT_SLOPE6	0	R/W	GPIO6 interrupt on 0… falling edge 1…rising edge
5	INT_SLOPE5	0	R/W	GPIO5 interrupt on 0… falling edge 1…rising edge

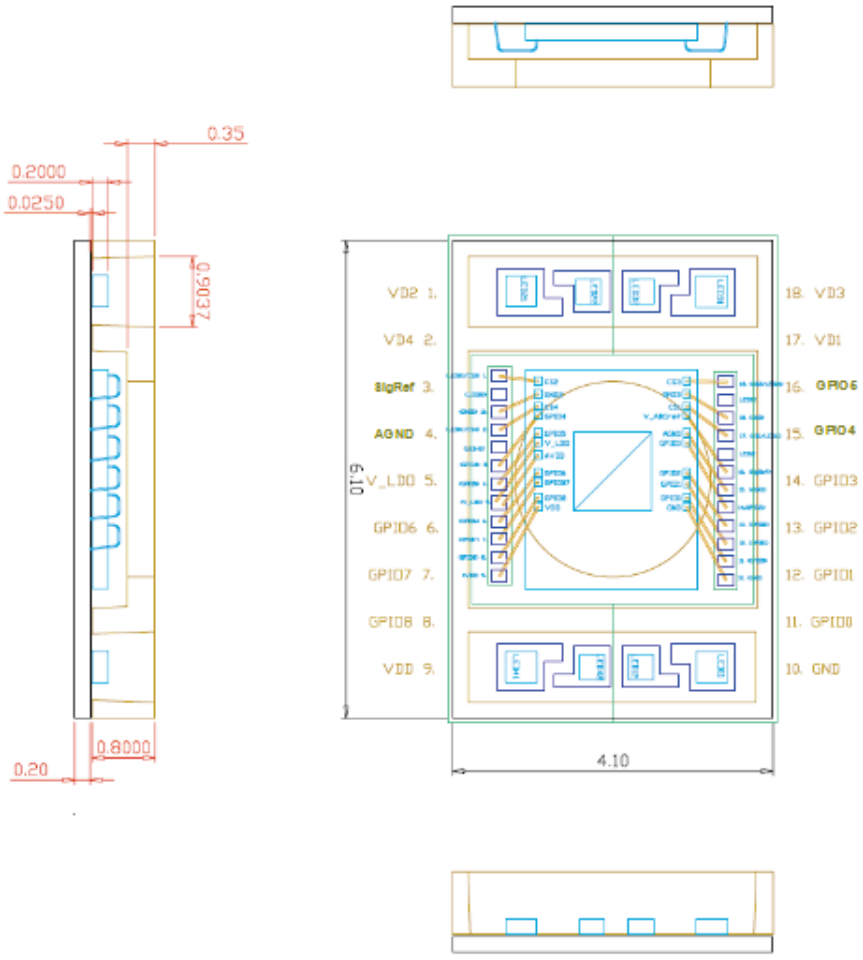
4	INT_SLOPE4	0	R/W	GPIO4 interrupt on 0… falling edge 1…rising edge
3	INT_SLOPE3	0	R/W	GPIO3 interrupt on 0… falling edge 1…rising edge
2	INT_SLOPE2	0	R/W	GPIO2 interrupt on 0… falling edge 1…rising edge
1	INT_SLOPE1	0	R/W	GPIO1 interrupt on 0… falling edge 1…rising edge
0	INT_SLOPE0	0	R/W	GPIO0 interrupt on 0… falling edge 1…rising edge

6 Ordering Information

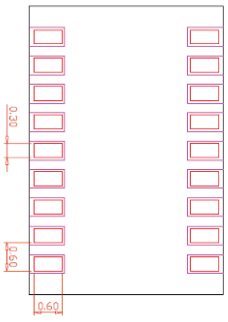
Figure X - X: Ordering Information

Ordering Code	Address	Interface	Delivery Form

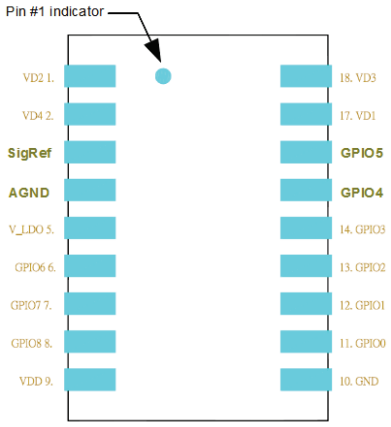
7 Package drawing



Bonding inside module (TOP VIEW)



Bottom Layer of substrate (TOP VIEW)



Bottom solder mask layer of substrate (TOP VIEW)

8 Register Map

tbd

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