ANY1630

Ultra-Low Power, Ultra-Small 32.768 kHz Oscillator

AnyCLK
Service depends on time

Features

- <20 ppm initial tolerance
- <100 ppm stability over -40°C to +85°C
- Small SMD package: 2.0 x 1.2 mm (2012)[1]
- Ultra-low power: 1.0 µA typ
- Vdd supply range: 1.5V to 3.63V
- Operating temperature ranges:
  - -10°C to +70°C
  - -40°C to +85°C
  - -40°C to +105°C[1]
- Internal filtering eliminates external Vdd bypass capacitors
- Pb-free, RoHS and REACH compliant

Applications

- Industrial timekeeping
- Industrial battery management
- Multi-drop 32 kHz clock distribution
- Bluetooth modules
- WiFi modules
- RTC Reference Clock

TempFlat MEMS™

Note: 1. For the smallest 32 kHz XO in CSP (1.2mm^2), consider the ANY1532. Contact Factory for -40°C to +105°C availability.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency and Stability						
Output Frequency	Fout		32.768		kHz	
Frequency Stability						
Initial Tolerance [2]	F_init			20	ppm	T_A = 25°C, post reflow, Vdd: 1.5V – 3.63V.
Frequency Stability Over Temperature [3]	F_stab			75	ppm	T_A = -10°C to +70°C, Vdd: 1.5V – 3.63V.
				100		T_A = -40°C to +85°C, Vdd: 1.5V – 3.63V.
				150		T_A = -40°C to +105°C, Vdd: 1.5V – 3.63V.
25°C Aging		-1		1	ppm	1st Year
Supply Voltage and Current Consumption						
Operating Supply Voltage	Vdd	1.5		3.63	V	T_A = over temperature
Operating Current	Idd		1.0		µA	T_A = 25°C, Vdd: 1.5V – 3.3V. No load
				1.90		T_A = -10°C to +70°C, Vdd max: 3.63V. No load
				2.20		T_A = -40°C to +85°C, Vdd max: 3.63V. No load
				2.80		T_A = -40°C to +105°C, Vdd max: 3.63V. No load
Power-Supply Ramp	t_Vdd_Ramp			100	ms	Over temperature, 0 to 90% Vdd
Start-up Time at Power-up	T_start		180	300	ms	T_A = 25°C ±10°C
				450		T_A = -40°C to +70°C
				500		T_A = +85°C
			800			T_A = +105°C
Operating Temperature Range						
Commercial Temperature	T_use	-10		70	°C	Temp code "C" in part number ordering
Industrial Temperature		-40		85		Temp code "I" in part number ordering
Extended Industrial Temperature		-40		105		Temp code "E" in part number ordering. Contact Factory for Availability.
LVCMOS Output, T_A = Over Temperature, typical values are at T_A = 25°C						
Output Rise/Fall Time	tr, tf		100	200	ns	10-90%, 15 pF load, Vdd = 1.5V to 3.63V
Output Clock Duty Cycle	DC	48		52	%	
Output Voltage High	VOH	90%			V	Vdd: 1.5V – 3.63V. I_{OH} = -10 µA, 15 pF
Output Voltage Low	VOL			10%	V	Vdd: 1.5V – 3.63V. I_{OL} = 10 µA, 15 pF
Maximum Output Drive				50	pF	≥80% LVCMOS swing, T_A = over temperature, Vdd = 1.5V to 3.3V
Period Jitter	T_jitt		35		ns_{RMS}	Cycles = 10,000, T_A = 25°C

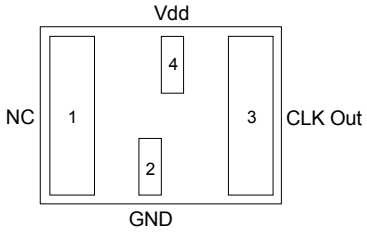
Notes:

2. Measured peak-to-peak. Tested with Agilent 53132A frequency counter. Due to the low operating frequency, the gate time must be ≥100 ms to ensure an accurate frequency measurement.
3. Measured peak-to-peak. Inclusive of Initial Tolerance at 25°C, and variations over operating temperature, rated power supply voltage and load.

Pin Configuration

SMD Pin	Symbol	I/O	Functionality
1	NC	No Connect	No Connect. Will not respond to any input signal.
2	GND	Power Supply Ground	Connect to ground. All GND pins must be connected to power supply ground.
3	CLK Out	OUT	Oscillator clock output. When interfacing to an MCU's XTAL input, the CLK Out is typically connected to the receiving IC's X IN pin.
4	Vdd	Power Supply	Connect to power supply 1.5V ≤ Vdd ≤ 3.63V. Under normal operating conditions, Vdd does not require external bypass/decoupling capacitor(s). Internal power supply filtering will reject more than ±150 mVpp with frequency components through 10 MHz.

SMD Package (Top View)



System Block Diagram

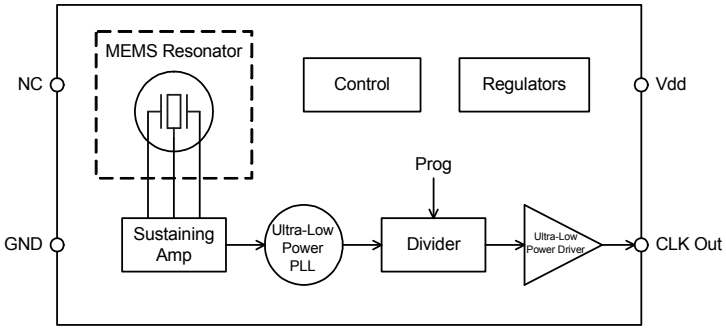


Figure 1.

Absolute Maximum

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Condition	Value	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 3.63	V
Short Duration Maximum Power Supply Voltage (Vdd)	≤30 minutes, over -40°C to +85°C	4.0	V
Short Duration Maximum Operating Temperature Range	Vdd = 1.5V - 3.63V, ≤30 mins	125	°C
Human Body Model ESD Protection	HBM, JESD22-A114	3000	V
Charge-Device Model (CDM) ESD Protection	JESD220C101	750	V
Machine Model (MM) ESD Protection	T_A = 25°C	300	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	Mil 883, Method 2002	10,000	g
Mechanical Vibration Resistance	Mil 883, Method 2007	70	g
2012 SMD Junction Temperature		150	°C
Storage Temperature		-65°C to 150°C	

Description

The ANY1630 is an ultra-small and ultra-low power 32.768 kHz oscillator optimized for battery-powered applications.

Anyclk's MEMS oscillators consist of MEMS resonators and a programmable analog circuit. Our MEMS resonators are built with Anyclk's unique MEMS First™ process. A key manufacturing step is EpiSeal™ during which the MEMS resonator is annealed with temperatures over 1000°C. EpiSeal creates an extremely strong, clean, vacuum chamber that encapsulates the MEMS resonator and ensures the best performance and reliability. During EpiSeal, a poly silicon cap is grown on top of the resonator cavity, which eliminates the need for additional cap wafers or other exotic packaging. As a result, Anyclk's MEMS resonator die can be used like any other semiconductor die. One unique result of Anyclk's MEMS First and EpiSeal manufacturing processes is the capability to integrate Anyclk's MEMS die with a SOC, ASIC, microprocessor or analog die within a package to eliminate external timing components and provide a highly integrated, smaller, cheaper solution to the customer.

Frequency Stability

The ANY1630 is factory calibrated (trimmed) to guarantee frequency stability to be less than 20 ppm at room temperature and very tight stability over temperature. Unlike quartz crystals that have a classic tuning fork parabola temperature curve with a 25°C turnover point, the ANY1630 temperature coefficient is extremely flat across temperature.

When measuring the ANY1630 output frequency with a frequency counter, it is important to make sure the counter's gate time is ≥100 ms. The slow frequency of a 32 kHz clock will give false readings with faster gate times.

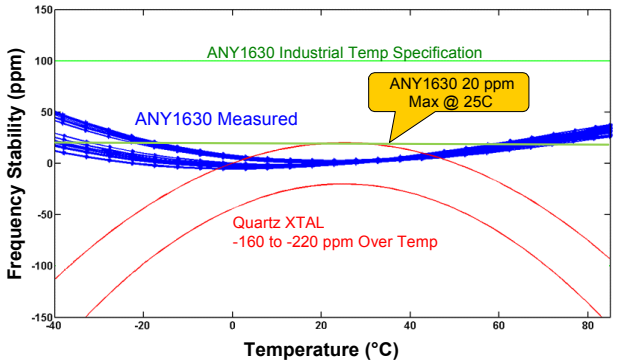


Figure 2. Anyclk vs. Quartz

Power Supply Noise Immunity

The ANY1630 is an ultra-small 32 kHz oscillator. In addition to eliminating external output load capacitors common with standard XTALs, this device includes special power supply filtering and thus, eliminates the need for an external Vdd bypass-decoupling capacitor. This feature further simplifies the design and keeps the footprint as small as possible. Internal power supply filtering is designed to reject AC-noise greater than ±150 mVpp magnitude and beyond 10 MHz frequency component.

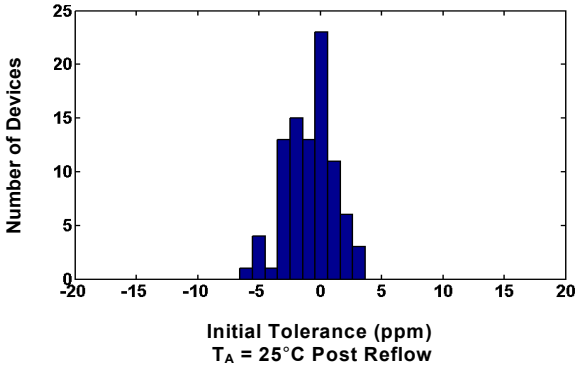
Power-up

The ANY1630 starts-up to a valid output frequency within 300 ms (180 ms typ). To ensure the device starts-up within the specified limit, make sure the power-supply ramps-up in approximately 10 - 20 ms (to within 90% of Vdd).

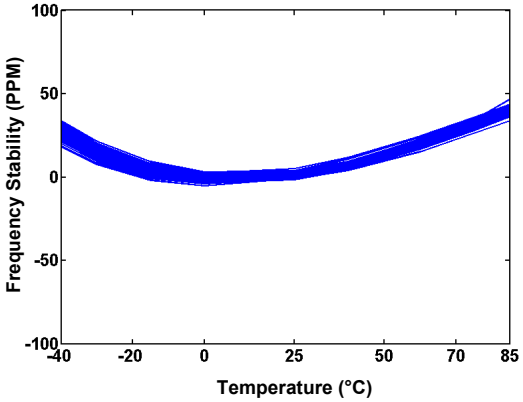
Typical Operating Curves

(T_A = 25°C, Vdd = 1.8V, unless otherwise stated)

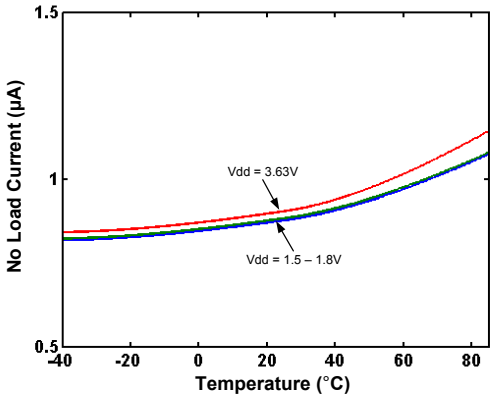
Initial Tolerance Histogram



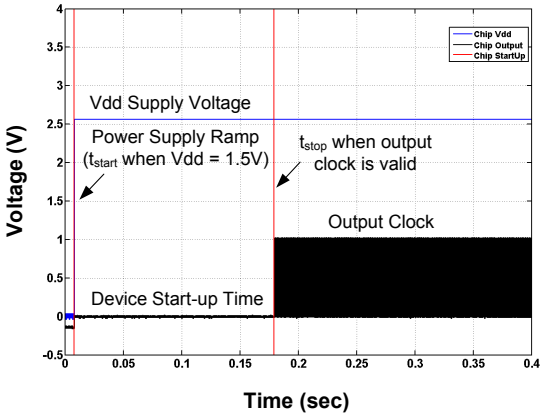
Frequency Stability Over Temperature



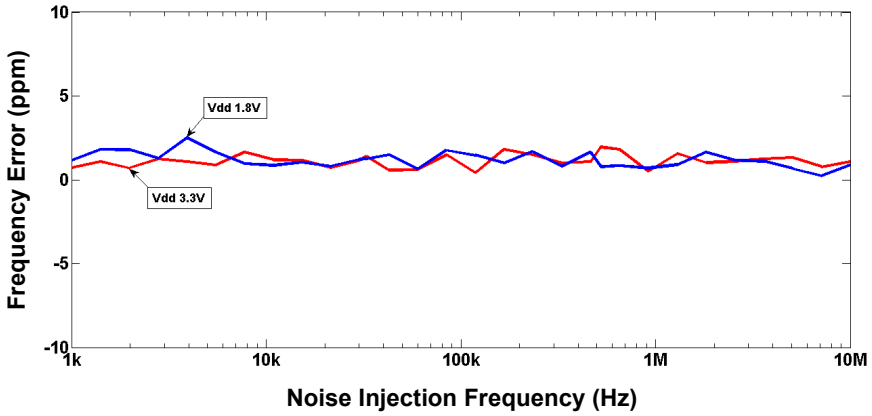
Supply Current Over Temperature (No Load)



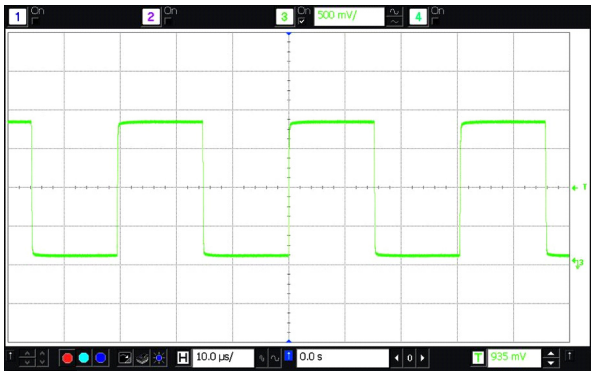
Start-up Time



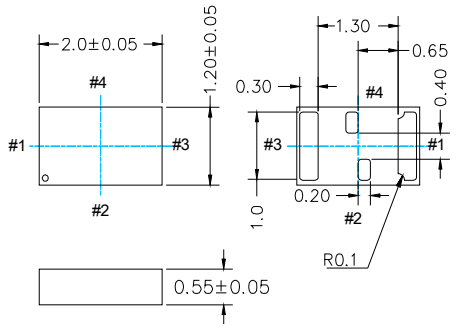
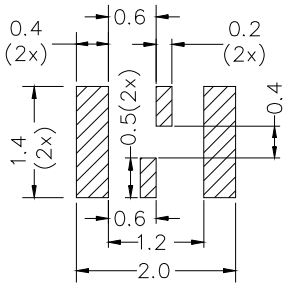
Power Supply Noise Rejection
(±150mV Noise)



LVCMOS Output Waveform
(V_{swing} = 1.8V, ANY1630AI-H4-DCC-32.768)



Dimensions and Patterns

Package Size – Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)
2.0 x 1.2 mm SMD 	

Manufacturing Guidelines

1)No Ultrasonic Cleaning: Do not subject the ANY1630 to an ultrasonic cleaning environment. Permanent damage or long term reliability issues to the MEMS structure may occur.

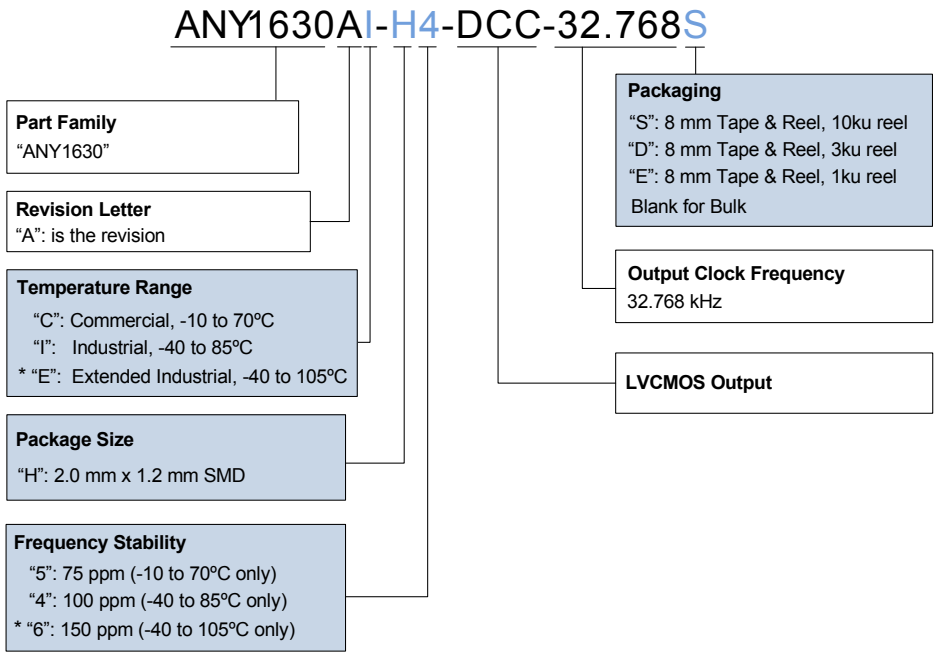
2) For Noisy, high EM environments, we recommend the following design guidelines:

- Place oscillator as far away from EM noise sources as possible (e.g., high-voltage switching regulators, motor drive control).
- Route noisy PCB traces, such as digital data lines or high di/dt power supply lines, away from the Anyclk oscillator.
- Add a low ESR/ESL, 0.1uF to 1.0uF ceramic capacitor (X7R) to help filter high frequency noise on the Vdd power-supply line. Place it as close to the Anyclk oscillator Vdd pin as posible.
- Place a solid GND plane underneath the Anyclk oscillator to shield the oscillator from noisy traces on the other board layers

3) For additional manufacturing guidelines and marking/tape-reel instructions, click on the following link:
http://www.anyclk.com

Ordering Information

Part number characters in blue represent the customer specific options. The other characters in the part number are fixed. Here are guidelines to select the correct output voltage.



* **Note:** Contact Factory for availability "E" temp range.

Revision History

Version	Release Date	Change Summary
1.0	9/3/14	Rev 0.85 Preliminary to Rev 1.0 Production Release • Updated start-up time specification • Deleted SOT23 package option • Added typical operating plots • Added maximum output drive specification • Added *Manufacturing Guidelines* section
1.1	9/3/14	• Updated start-up time plot in *Typical Operating Curves* section • Updated start-up time specification
1.2	11/25/14	• Added additional design-in/mfg guidelines