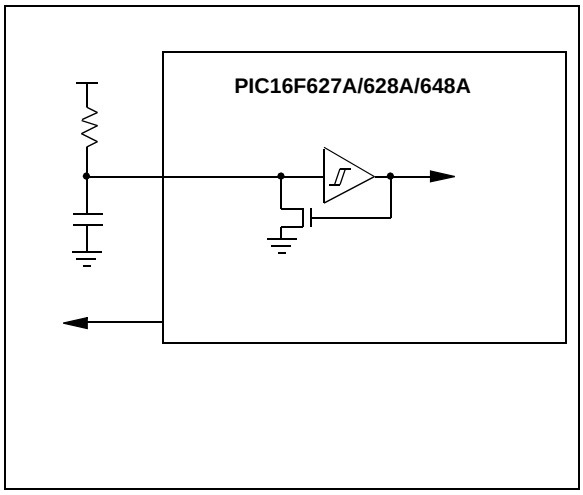
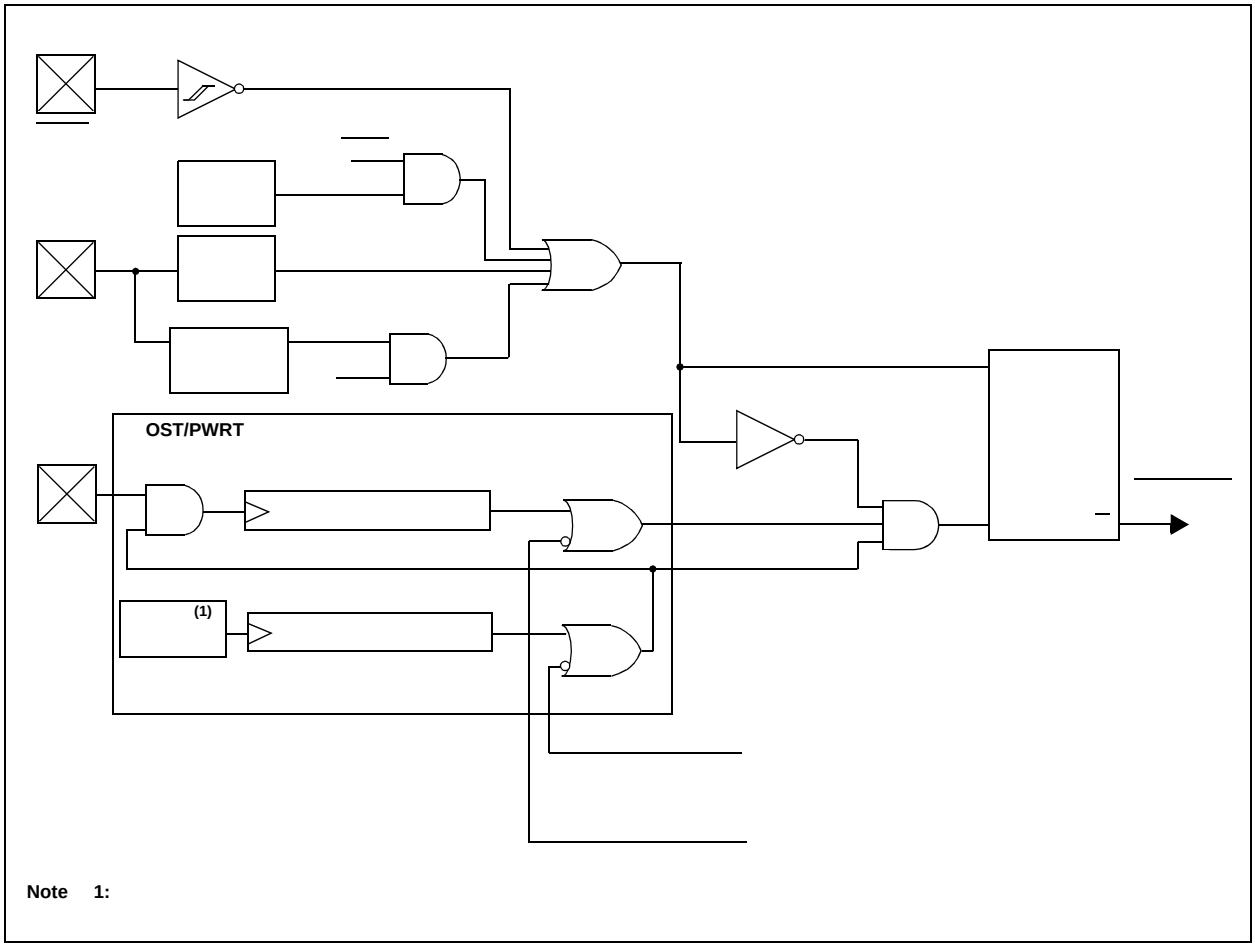
FIGURE 14-5: RC OSCILLATOR MODE



Section 4.2.2.6 “PCON Register”

14.3 Reset

FIGURE 14-6: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1:

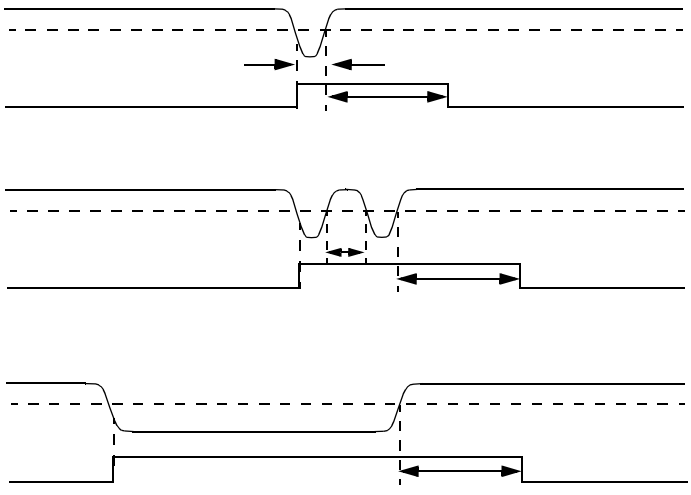
14.4 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST) and Brown-out Reset (BOR)

Section 17.0

“Electrical Specifications”

Power-up Trouble Shooting

FIGURE 14-7: BROWN-OUT SITUATIONS WITH PWRT ENABLED



Note: 0

0

0

0

1

0

TABLE 14-3: TIME OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up Timer		Brown-out Reset		Wake-up from Sleep
	$\overline{PWRTE}$ = 0	$\overline{PWRTE}$ = 1	$\overline{PWRTE}$ = 0	$\overline{PWRTE}$ = 1	

TABLE 14-4: STATUS/PCON BITS AND THEIR SIGNIFICANCE

$\overline{POR}$	$\overline{BOR}$	$\overline{TO}$	$\overline{PD}$	Condition
0	X	1	1	
0	X	0	X	
0	X	X	0	
1	0	X	X	
1	1	0	u	
1	1	0	0	
1	1	u	u	
1	1	1	0	

Legend: u x

TABLE 14-5: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT RESET

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other Resets(1)
					—	—				0001 1xxx	000q quuu
								—	—	---- 1-0x	---- u-uq

Legend: x u - 0 q

Note 1: —

TABLE 14-6: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	Status Register	PCON Register
		0001 1xxx	---- 1-0x
—		000u uuuu	---- 1-uu
—		0001 0uuu	---- 1-uu
		0000 uuuu	---- 1-uu
		uuu0 0uuu	---- u-uu
		000x xuuu	---- 1-u0
	(1)	uuu1 0uuu	---- u-uu

Legend: u x - 0
Note 1:

TABLE 14-7: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset	• MCLR Reset during normal operation • MCLR Reset during Sleep • WDT Reset • Brown-out Reset (1)	• Wake-up from Sleep(7) through interrupt • Wake-up from Sleep(7) through WDT time out
		xxxx xxxx	uuuu uuuu	uuuu uuuu
		xxxx xxxx	uuuu uuuu	uuuu uuuu
		0000 0000	0000 0000	PC + 1 (3)
		0001 1xxx	000q quuu (4)	uuuq 0uuu (4)
		xxxx xxxx	uuuu uuuu	uuuu uuuu
		xxxx 0000	xxxx 0000	uuuu uuuu
		xxxx xxxx	uuuu uuuu	uuuu uuuu
		---0 0000	---0 0000	---u uuuu
		0000 000x	0000 000u	uuuu uqqq (2)
		0000 -000	0000 -000	qqqq -qqq (2)
		xxxx xxxx	uuuu uuuu	uuuu uuuu
		xxxx xxxx	uuuu uuuu	uuuu uuuu
		--00 0000	--uu uuuu (6)	--uu uuuu
		0000 0000	0000 0000	uuuu uuuu
		-000 0000	-000 0000	-uuu uuuu
		xxxx xxxx	uuuu uuuu	uuuu uuuu
		xxxx xxxx	uuuu uuuu	uuuu uuuu
		--00 0000	--00 0000	--uu uuuu
		0000 000x	0000 000x	uuuu uuuu
		0000 0000	0000 0000	uuuu uuuu
		0000 0000	0000 0000	uuuu uuuu
		0000 0000	0000 0000	uu-- uuuu
		1111 1111	1111 1111	uuuu uuuu
		1111 1111	1111 1111	uuuu uuuu
		1111 1111	1111 1111	uuuu uuuu
		0000 -000	0000 -000	uuuu -uuu
		---- 1-0x	---- 1-uq (1,5)	---- u-uu
		1111 1111	1111 1111	uuuu uuuu
		0000 -010	0000 -010	uuuu -uuu
		0000 0000	0000 0000	uuuu uuuu
		xxxx xxxx	uuuu uuuu	uuuu uuuu
		xxxx xxxx	uuuu uuuu	uuuu uuuu
		---- x000	---- q000	---- uuuu
		000- 0000	000- 0000	uuu- uuuu

Legend: u x - 0 q

Note 1:
2:
3:
4:
5: 0 u
6: --00 0000
7:

FIGURE 14-8: TIME OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE

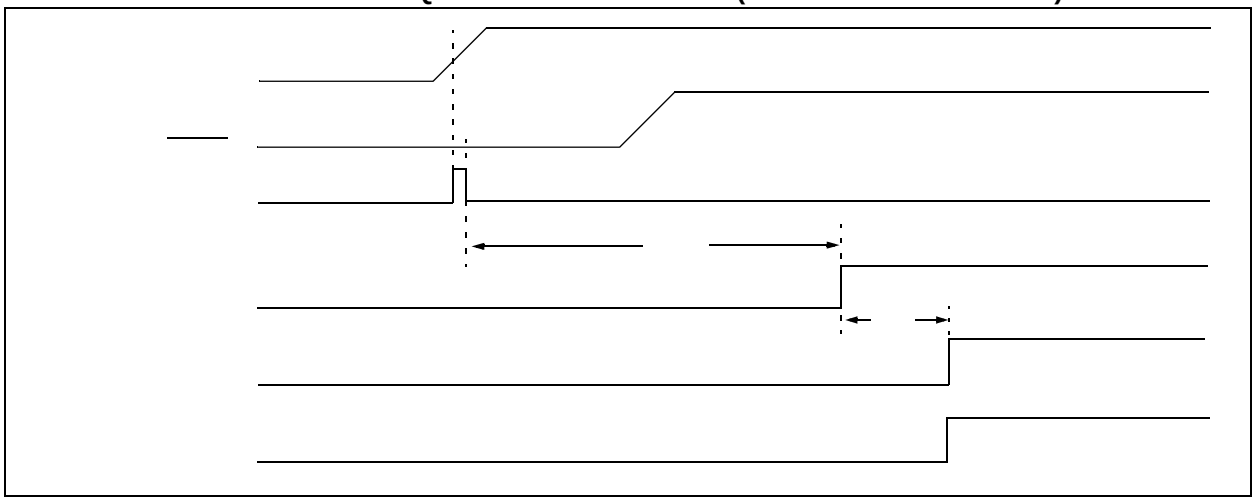


FIGURE 14-9: TIME OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD}): CASE 2

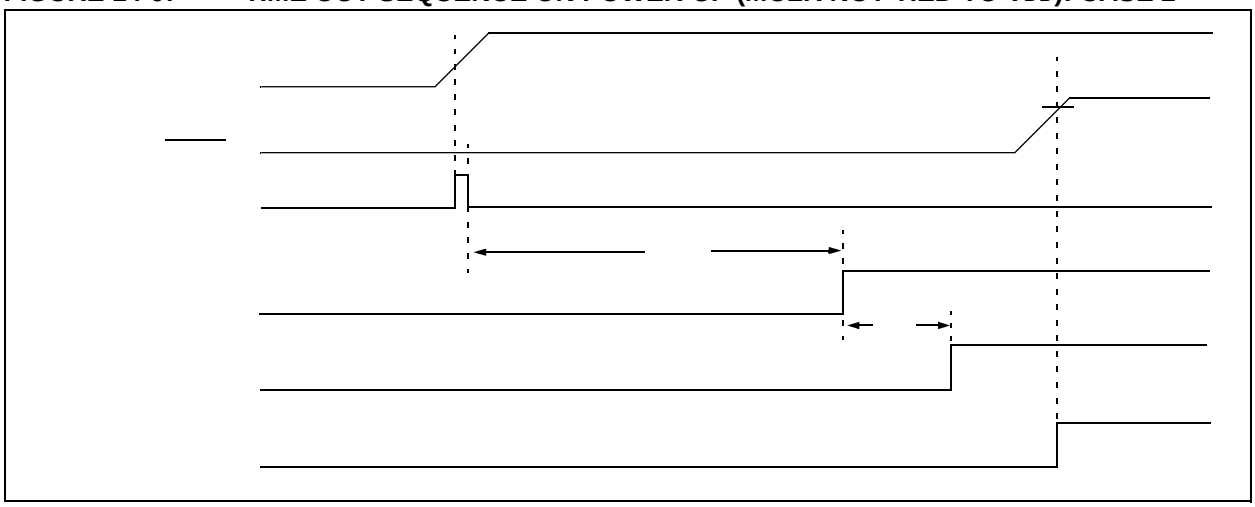


FIGURE 14-10: TIME OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD})

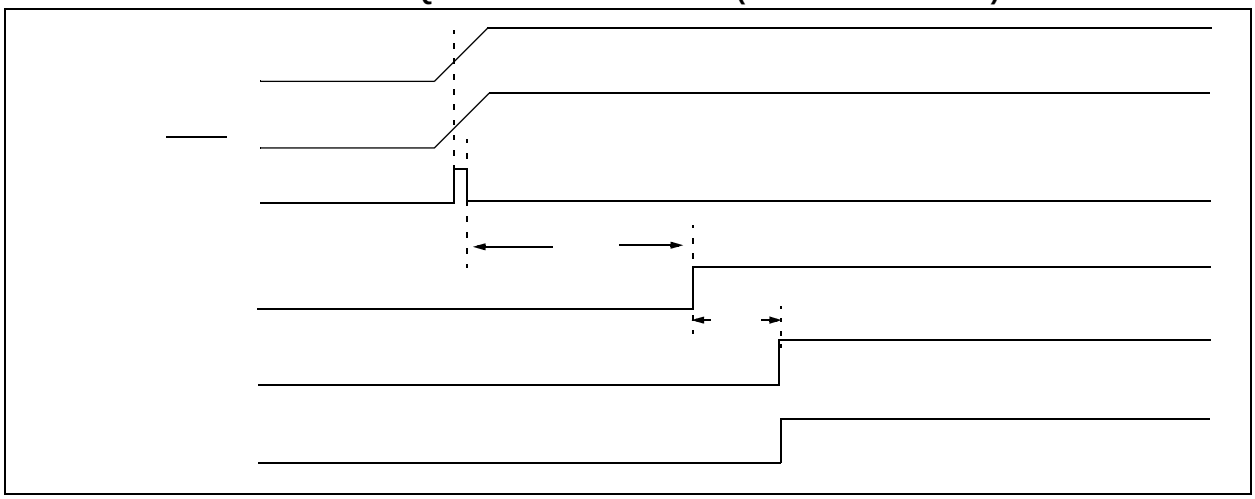
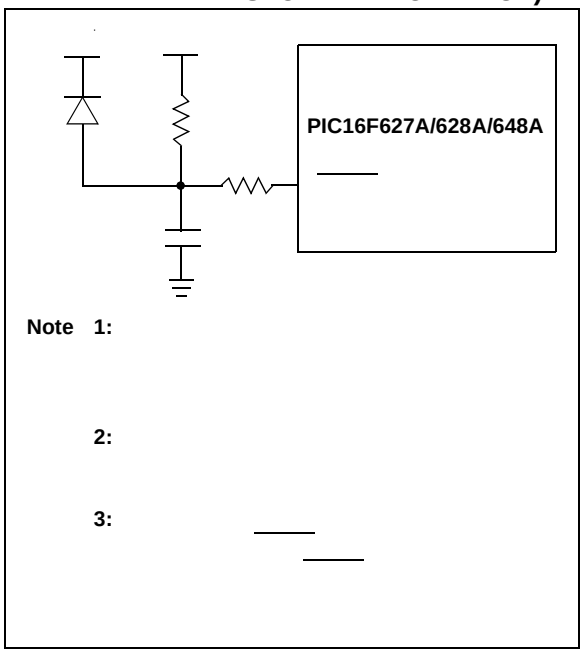


FIGURE 14-11: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)

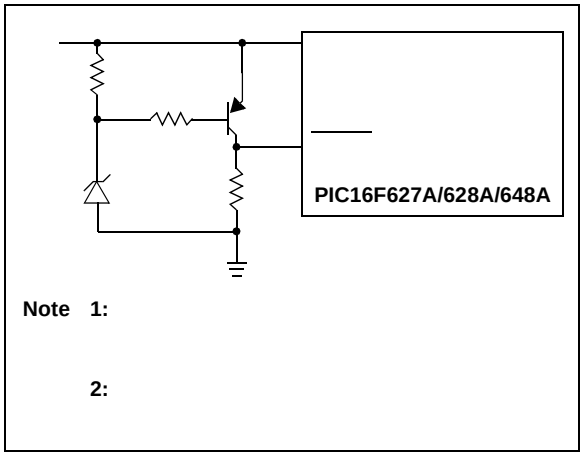


Note 1:

2:

3:

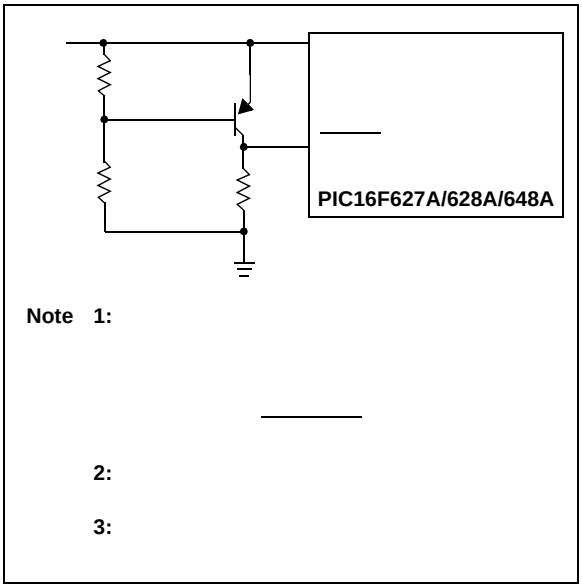
FIGURE 14-12: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



Note 1:

2:

FIGURE 14-13: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



Note 1:

2:

3:

14.5 Interrupts

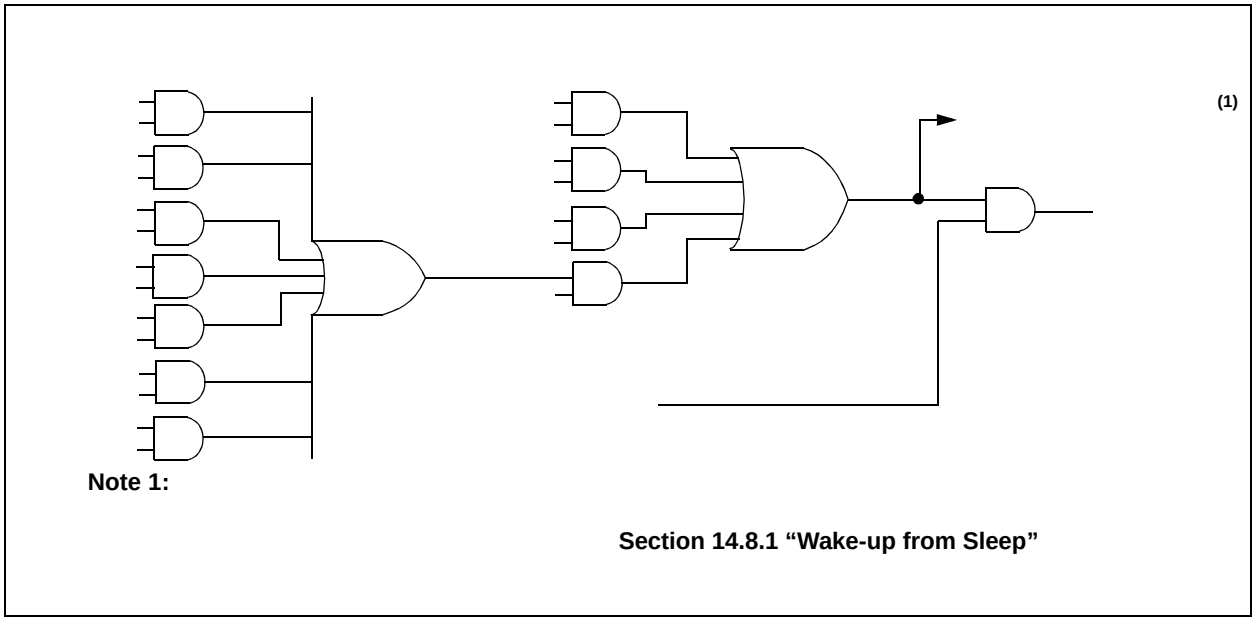
Note 1:

2:

RETFIE

NOP

FIGURE 14-14: INTERRUPT LOGIC



Section 5.2 “PORTB and TRISB Registers”

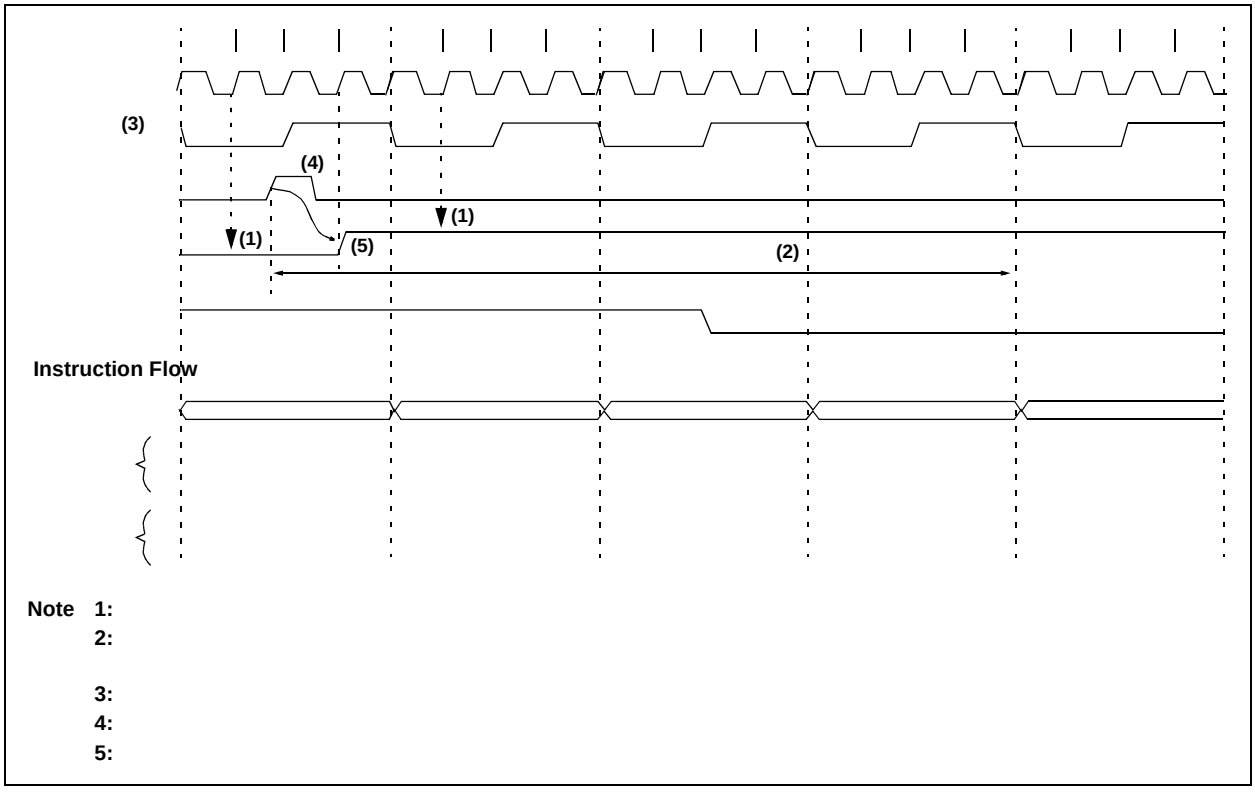
Note:

Section 14.8 “Power-Down Mode (Sleep)”

Section 10.6 “Comparator Interrupts”

Section 6.0 “Timer0 Module”

FIGURE 14-15: INT PIN INTERRUPT TIMING



Note 1:
2:
3:
4:
5:

TABLE 14-8: SUMMARY OF INTERRUPT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other Resets(1)
										0000 000x	0000 000u
										0000 -000	0000 -000
										0000 -000	0000 -000

Note 1:

14.6 Context Saving During Interrupts

14.7 Watchdog Timer (WDT)

SLEEP

Section 14.1 “Configuration Bits”

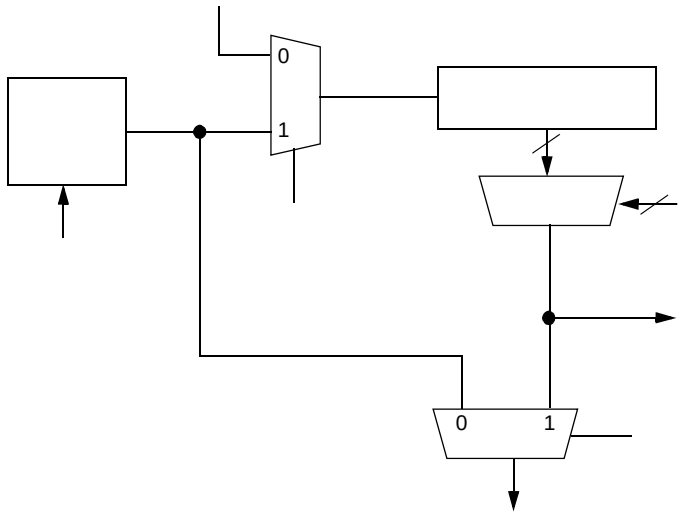
EXAMPLE 14-1: SAVING THE STATUS AND W REGISTERS IN RAM

```
MOVWF     W_TEMP          ;copy W to temp register,
                          ;could be in any bank
SWAPF     STATUS,W        ;swap status to be saved
                          ;into W
BCF       STATUS,RP0      ;change to bank 0
                          ;regardless of current
                          ;bank
MOVWF     STATUS_TEMP ;save status to bank 0
                          ;register
      :
      :(ISR)
      :

SWAPF     STATUS_TEMP,W;swap STATUS_TEMP
register
                          ;into W, sets bank to
original
                          ;state
MOVWF     STATUS          ;move W into STATUS
                          ;register
SWAPF     W_TEMP,F        ;swap W_TEMP
SWAPF     W_TEMP,W        ;swap W_TEMP into W
```

CLRWDT SLEEP

FIGURE 14-16: WATCHDOG TIMER BLOCK DIAGRAM



Note:

TABLE 14-9: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other Resets
										uuuu uuuu	uuuu uuuu
										1111 1111	1111 1111

Legend: x u - 0 q

Note:

14.8 Power-Down Mode (Sleep)

SLEEP

SLEEP

Note:

SLEEP

SLEEP

SLEEP

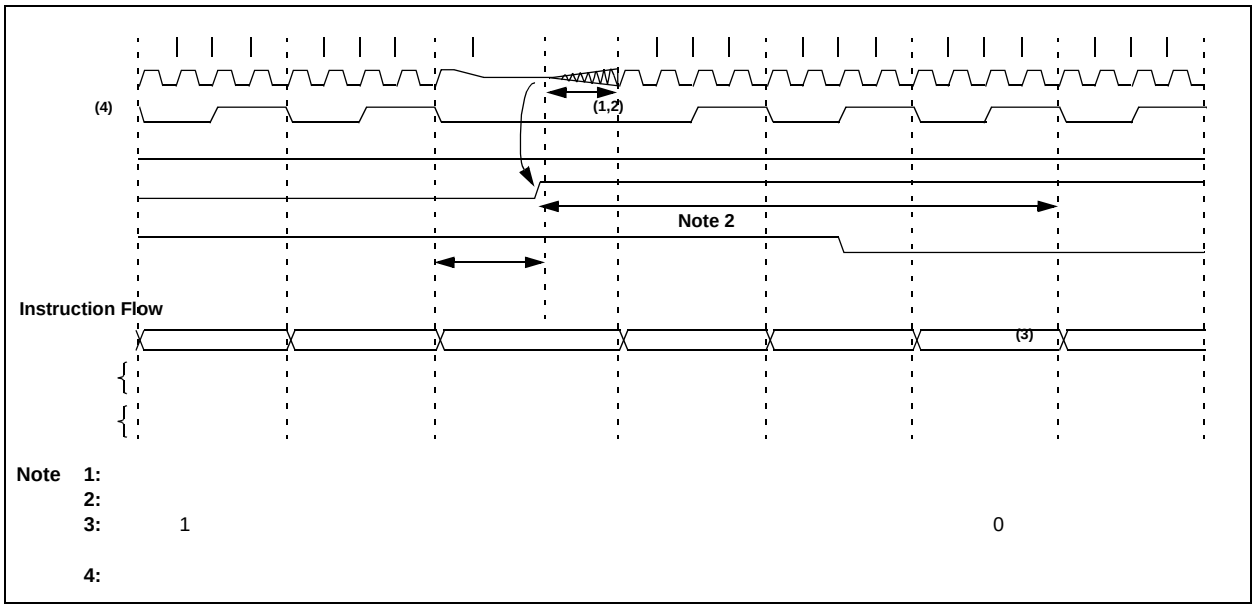
SLEEP

SLEEP
NOP SLEEP

Note:

SLEEP
NOP

FIGURE 14-17: WAKE-UP FROM SLEEP THROUGH INTERRUPT



14.9 Code Protection

14.10 User ID Locations

0 PIC16F627A/628A/
648A EEPROM Memory Programming Specification

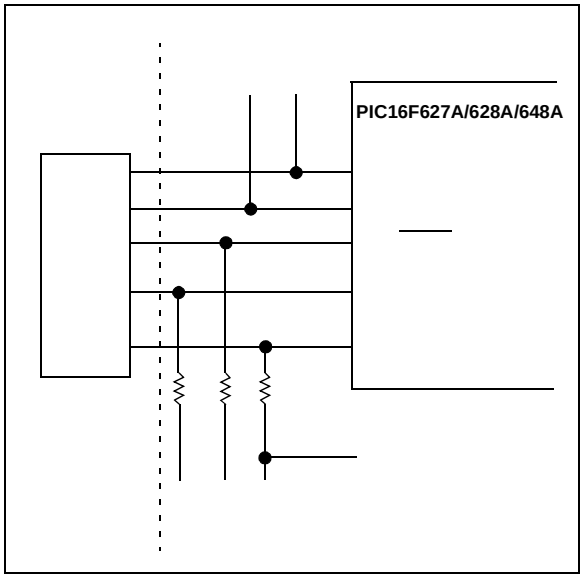
Note:

14.11 In-Circuit Serial Programming™ (ICSP™)

PIC16F627A/628A/648A EEPROM Memory Programming Specification

PIC16F627A/628A/648A EEPROM Memory Programming Specification

FIGURE 14-18: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



14.12 Low-Voltage Programming

1

1

Note 1:

2:

0

0

14.13 In-Circuit Debugger

TABLE 14-19: DEBUGGER RESOURCES

I/O pins	ICDCLK, ICDDATA
	NOP

NOTES:

15.0 INSTRUCTION SET SUMMARY

Byte-oriented
Bit-oriented
Literal and control

byte-oriented bit-oriented
literal and control

byte-oriented

NOP

bit-oriented

literal and control

Note 1:

2:

OPTION TRIS

15.1 Read-Modify-Write Operations

clrf PORTB

FIGURE 15-1: GENERAL FORMAT FOR INSTRUCTIONS

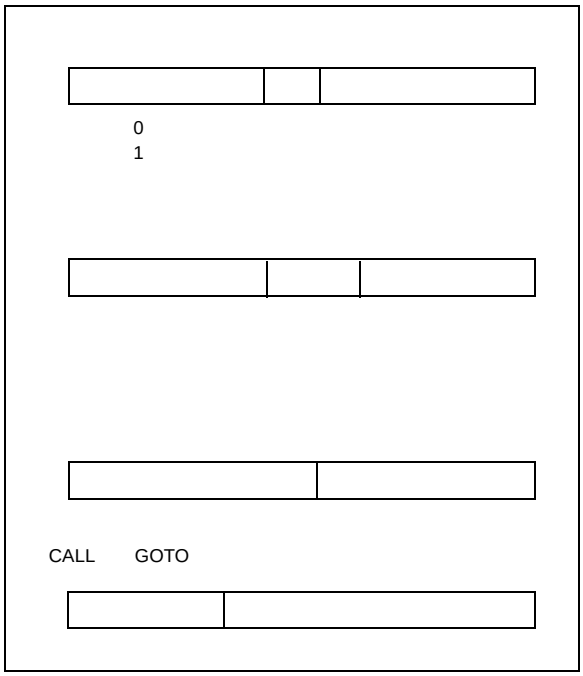


TABLE 15-1: OPCODE FIELD DESCRIPTIONS

Field	Description
	0 1 0
	0 1 1
—	
—	

TABLE 15-2: PIC16F627A/628A/648A INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	14-Bit Opcode				Status Affected	Notes
			MSb			LSb		
ADDWF			00	0111	dfff	ffff		**1, 2**
ANDWF			00	0101	dfff	ffff		**1, 2**
CLRF			00	0001	lfff	ffff		**2**
CLRW			00	0001	0xxx	xxxx		
COMF			00	1001	dfff	ffff		**1, 2**
DECF			00	0011	dfff	ffff		**1, 2**
DECFSZ		**(2)**	00	1011	dfff	ffff		**1, 2, 3**
INCF			00	1010	dfff	ffff		**1, 2**
INCFSZ		**(2)**	00	1111	dfff	ffff		**1, 2, 3**
IORWF			00	0100	dfff	ffff		**1, 2**
MOVF			00	1000	dfff	ffff		**1, 2**
MOVWF			00	0000	lfff	ffff		
NOP			00	0000	0xx0	0000		
RLF			00	1101	dfff	ffff		**1, 2**
RRF			00	1100	dfff	ffff		**1, 2**
SUBWF			00	0010	dfff	ffff		**1, 2**
SWAPF			00	1110	dfff	ffff		**1, 2**
XORWF			00	0110	dfff	ffff		**1, 2**
BCF			01	00bb	bfff	ffff		**1, 2**
BSF			01	01bb	bfff	ffff		**1, 2**
BTFSC		**(2)**	01	10bb	bfff	ffff		**3**
BTFSS		**(2)**	01	11bb	bfff	ffff		**3**
ADDLW			11	111x	kkkk	kkkk		
ANDLW			11	1001	kkkk	kkkk		
CALL			10	0kkk	kkkk	kkkk		
CLRWDT			00	0000	0110	0100		
GOTO			10	1kkk	kkkk	kkkk		
IORLW			11	1000	kkkk	kkkk		
MOVLW			11	00xx	kkkk	kkkk		
RETFIE			00	0000	0000	1001		
RETLW			11	01xx	kkkk	kkkk		
RETURN			00	0000	0000	1000		
SLEEP			00	0000	0110	0011		
SUBLW			11	110x	kkkk	kkkk		
XORLW			11	1010	kkkk	kkkk		

Note 1: MOVF PORTB, 1

1

0

2: 1

3:

NOP

15.2 Instruction Descriptions

ADDLW **Add Literal and W**

label

11	111x	kkkk	kkkk

ADDLW 0x15

ANDLW **AND Literal with W**

label

11	1001	kkkk	kkkk

ANDLW 0x5F

ADDWF **Add W and f**

label

00	0111	dfff	ffff

0

1

ADDWF REG1, 0

ANDWF **AND W with f**

label

00	0101	dfff	ffff

0

1

ANDWF REG1, 1

BCF **Bit Clear f**

label

01	00bb	bfff	ffff

BCF REG1, 7

BSF **Bit Set f**

label

01	01bb	bfff	ffff

BSF REG1, 7

BTFSC **Bit Test f, Skip if Clear**

label

0

01	10bb	bfff	ffff

0

0

HERE BTFSC REG1
FALSE GOTO PROCESS_CODE
TRUE •
•
•

HERE

0
TRUE
1
FALSE

BTFSS **Bit Test f, Skip if Set**

label

1

01	11bb	bfff	ffff

1

1

NOP

HERE BTFSS REG1
FALSE GOTO PROCESS_CODE
TRUE •
•
•

HERE

0

FALSE

1

TRUE

CALL **Call Subroutine**

label

10	0kkk	kkkk	kkkk

CALL

HERE CALL THERE

HERE

THERE
HERE+1

CLRF **Clear f**

label

00	0001	1fff	ffff

CLRF REG1

1

CLRW **Clear W**

label

00	0001	0000	0011

CLRW

1

CLRWDT **Clear Watchdog Timer**

label

00	0000	0110	0100

CLRWDT

CLRWDT

0
1
1

COMF **Complement f**

label

-

00	1001	dfff	ffff

0
1

COMF REG1, 0

DECF **Decrement f**

label

00	0011	dfff	ffff

0
1

DECF CNT, 1

0
1

DECFSZ **Decrement f, Skip if 0**

label

00	1011	dfff	ffff

0

1

0

NOP

HERE DECFSZ REG1, 1
GOTO LOOP
CONTINUE •
•
•

HERE

0

CONTINUE

0

HERE+1

GOTO **Unconditional Branch**

label

10	1kkk	kkkk	kkkk

GOTO

GOTO

GOTO THERE

THERE

INCF **Increment f**

label

00	1010	dfff	ffff

0

1

INCF REG1, 1

0

1

INCFSZ **Increment f, Skip if 0**

label

0

00	1111	dfff	ffff

0

1

0

NOP

```
HERE    INCFSZ  REG1, 1
        GOTO    LOOP
CONTINUE •
         •
         •
```

HERE

0

CONTINUE

0

HERE +1

IORLW **Inclusive OR Literal with W**

label

11	1000	kkkk	kkkk

IORLW 0x35

0

IORWF **Inclusive OR W with f**

label

00	0100	dfff	ffff

0

1

IORWF REG1, 0

1

MOVLW **Move Literal to W**

label

11	00xx	kkkk	kkkk

0

MOVLW 0x5A

MOVF **Move f**

label

00	1000	dfff	ffff

0

1

1

MOVF REG1, 0

1

MOVWF **Move W to f**

label

00	0000	1fff	ffff

_____ MOVWF REG1

OPTION **Load Option Register**

label

00	0000	0110	0010

MOVWF.

_____

To maintain upward compatibility with future PIC® MCU products, do not use this instruction.

NOP **No Operation**

label

00	0000	0xx0	0000

_____ NOP

RETFIE **Return from Interrupt**

label

00	0000	0000	1001

_____ RETFIE

RETLW **Return with Literal in W**

Syntax: label

11	01xx	kkkk	kkkk

Example:

```
CALL TABLE;W contains table
      ;offset value
•     ;W now has table value
•
•
TABLE ADDWF PC;W = offset
      RETLW k1;Begin table
      RETLW k2;
      •
      •
      •
      RETLW kn; End of table
```

RETURN **Return from Subroutine**

Syntax: label

00	0000	0000	1000

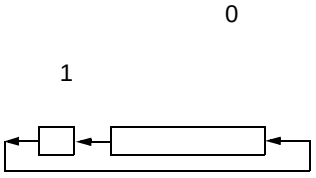
Example:

```
RETURN
```

RLF **Rotate Left f through Carry**

Syntax: label

00	1101	dfff	ffff



Example:

```
RLF   REG1, 0
```

Before Instruction
REG1 =1110 0110
C = 0

After Instruction
REG1 =1110 0110
W = 1100 1100
C = 1

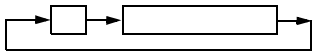
RRF **Rotate Right f through Carry**

label

00	1100	dfff	ffff

0

1



RRF REG1, 0

= 1110 0110
= 0

= 1110 0110
= 0111 0011
= 0

SLEEP

labe

00	0000	0110	0011

Section 14.8
“Power-Down Mode (Sleep)”

SLEEP

SUBLW **Subtract W from Literal**

label

11	110x	kkkk	kkkk

SUBLW 0x02

1

1
1

0
1

0

SUBWF **Subtract W from f**

label

00	0010	dfff	ffff

0

1

SUBWF REG1, 1

1

1
1
0

0

1

1

1

0

0

SWAPF **Swap Nibbles in f**

label

00	1110	dfff	ffff

0

1

SWAPF REG1, 0

TRIS **Load TRIS Register**

label

00	0000	0110	0fff

To maintain upward compatibility with future PIC® MCU products, do not use this instruction.

XORLW **Exclusive OR Literal with W**

label

11	1010	kkkk	kkkk

XORLW 0xAF

XORWF **Exclusive OR W with f**

label

00	0110	dfff	ffff

0

1

XORWF REG1, 1

16.0 DEVELOPMENT SUPPORT

16.1 MPLAB Integrated Development Environment Software

16.2 MPLAB C Compilers for Various Device Families

16.3 HI-TECH C for Various Device Families

16.4 MPASM Assembler

16.5 MPLINK Object Linker/ MPLIB Object Librarian

16.6 MPLAB Assembler, Linker and Librarian for Various Device Families

16.7 MPLAB SIM Software Simulator

16.8 MPLAB REAL ICE In-Circuit Emulator System

16.9 MPLAB ICD 3 In-Circuit Debugger System

16.10 PICkit 3 In-Circuit Debugger/ Programmer and PICkit 3 Debug Express

16.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

16.12 MPLAB PM3 Device Programmer

16.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

17.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings(†)

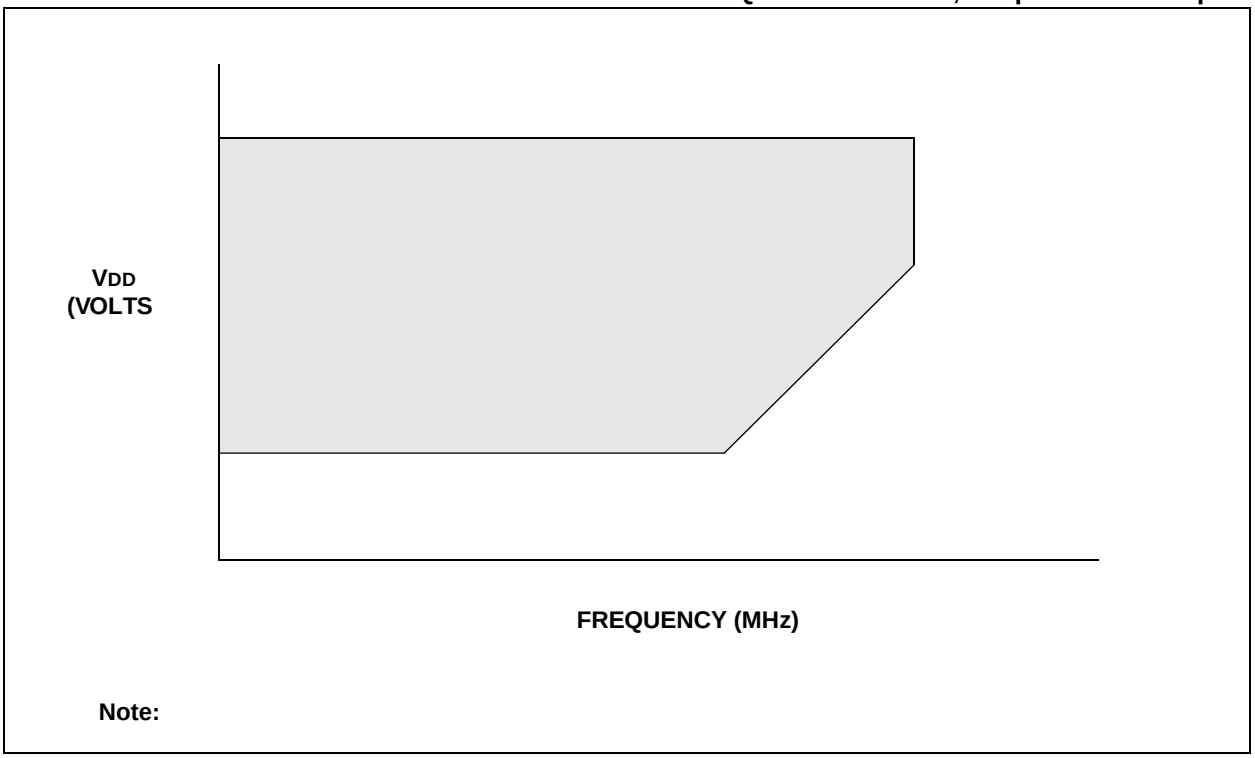
(1)

Note 1:

† NOTICE

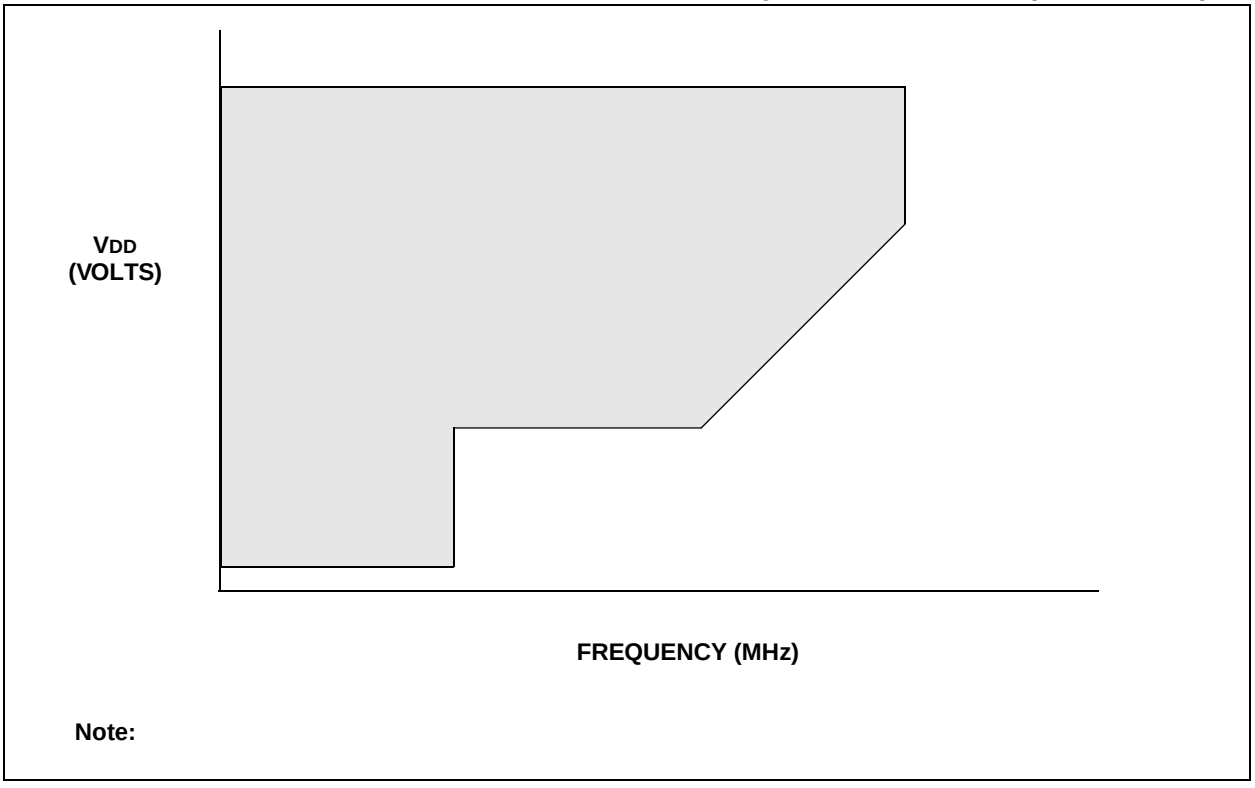
Note:

FIGURE 17-1: PIC16F627A/628A/648A VOLTAGE-FREQUENCY GRAPH, -40qC d TA d +125qC



Note:

FIGURE 17-2: PIC16LF627A/628A/648A VOLTAGE-FREQUENCY GRAPH, -40qC d TA d +85qC



Note:

17.1 DC Characteristics: PIC16F627A/628A/648A (Industrial, Extended) PIC16LF627A/628A/648A (Industrial)

PIC16LF627A/628A/648A			Standard Operating Conditions (unless otherwise stated)				
PIC16F627A/628A/648A			Standard Operating Conditions (unless otherwise stated)				
Param No.	Sym	Characteristic/Device	Min	Typ†	Max	Units	Conditions
		Supply Voltage					
		RAM Data Retention Voltage(1)					
		VDD Start Voltage					Section 14.4 “Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST) and Brown-out Reset (BOR)”
		VDD Rise Rate					Section 14.4 “Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST) and Brown-out Reset (BOR)”
		Brown-out Reset Voltage					

Legend:

Note 1:

17.2 DC Characteristics: PIC16F627A/628A/648A (Industrial) PIC16LF627A/628A/648A (Industrial)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)					
Param No.	LF and F Device Characteristics	Min†	Typ	Max	Units	Conditions	
						V_{DD}	Note
Supply Voltage (V_{DD})							
Power-down Base Current (I_{PD})							
Peripheral Module Current (' I_{MOD})[1]							
Supply Current (I_{DD})							

17.3 DC Characteristics: PIC16F627A/628A/648A (Extended)

DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated)					
Param No.	Device Characteristics	Min†	Typ	Max	Units	Conditions	
						V_{DD}	Note
Supply Voltage (V_{DD})							
Power-down Base Current (I_{PD})							
Peripheral Module Current (' I_{MOD})[1]							
Supply Current (I_{DD})							

Note 1:

17.4 DC Characteristics: PIC16F627A/628A/648A (Industrial, Extended) PIC16LF627A/628A/648A (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
Param. No.	Sym	Characteristic/Device	Min	Typ†	Max	Unit	Conditions
		Input Low Voltage					
		_____ (4)					(Note1)
		Input High Voltage					
		_____ (4)					(Note1)
		PORTB weak pull-up current					
		Input Leakage Current(2), (3)					
		(4) _____					
		Output Low Voltage					
		(4)					
		Output High Voltage(3)					
		(4)					
		Open-Drain High Voltage					
		Capacitive Loading Specs on Output Pins					

Note 1:

_____

2:

3:

4:

**TABLE 17-1: DC Characteristics: PIC16F627A/628A/648A (Industrial, Extended)
PIC16LF627A/628A/648A (Industrial)**

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
		Data EEPROM Memory					
		(1)					
		Program Flash Memory					

Note 1: Section 13.7 “Using the Data EEPROM”

TABLE 17-2: COMPARATOR SPECIFICATIONS

Operating Conditions: 2.0V VDD 5.5V, -40°C < TA < +125°C, unless otherwise stated.							
Param No.	**Characteristics**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Comments**
	(1)						

Note 1:

TABLE 17-3: VOLTAGE REFERENCE SPECIFICATIONS

Operating Conditions: 2.0V < VDD < 5.5V, -40qC < TA < +125qC, unless otherwise stated.							
Spec No.	**Characteristics**	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Comments**
							1 0
							1 0
	(1)						

Note 1: 1 0000 1111
2:

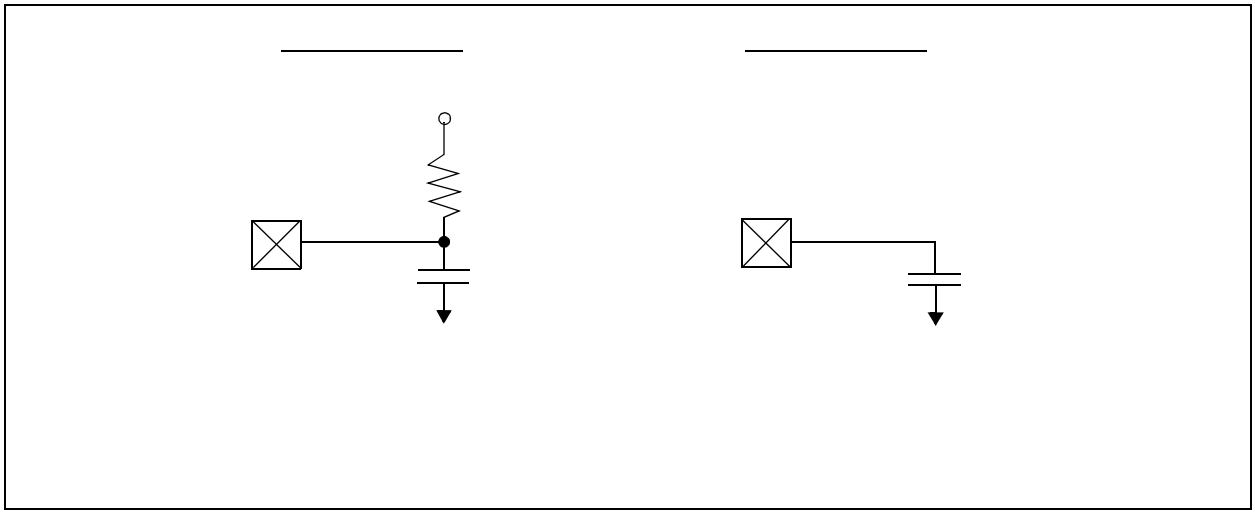
17.5 Timing Parameter Symbology

T	

pp	

S	

FIGURE 17-3: LOAD CONDITIONS



17.6 Timing Diagrams and Specifications

FIGURE 17-4: EXTERNAL CLOCK TIMING

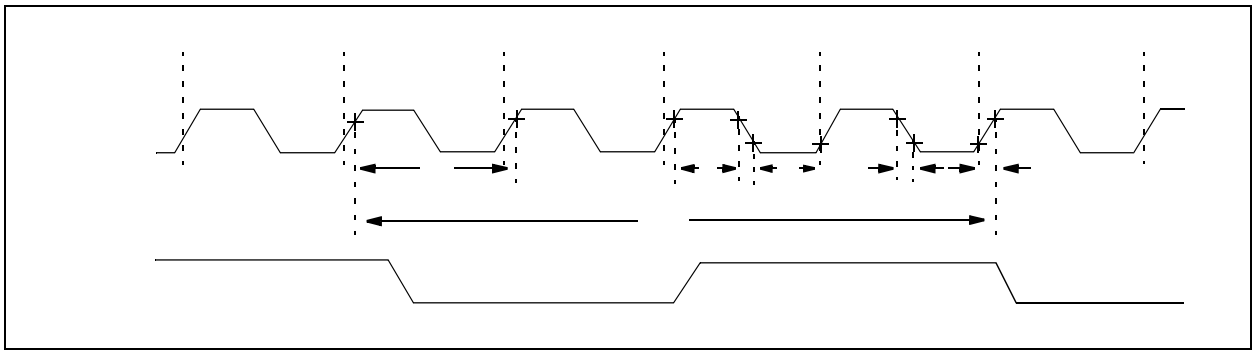


TABLE 17-4: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
		(1)					
		(1)					
		(1)					
		(1)					

Note 1:

TABLE 17-5: PRECISION INTERNAL OSCILLATOR PARAMETERS

Parameter No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions

Legend:

FIGURE 17-5: CLKOUT AND I/O TIMING

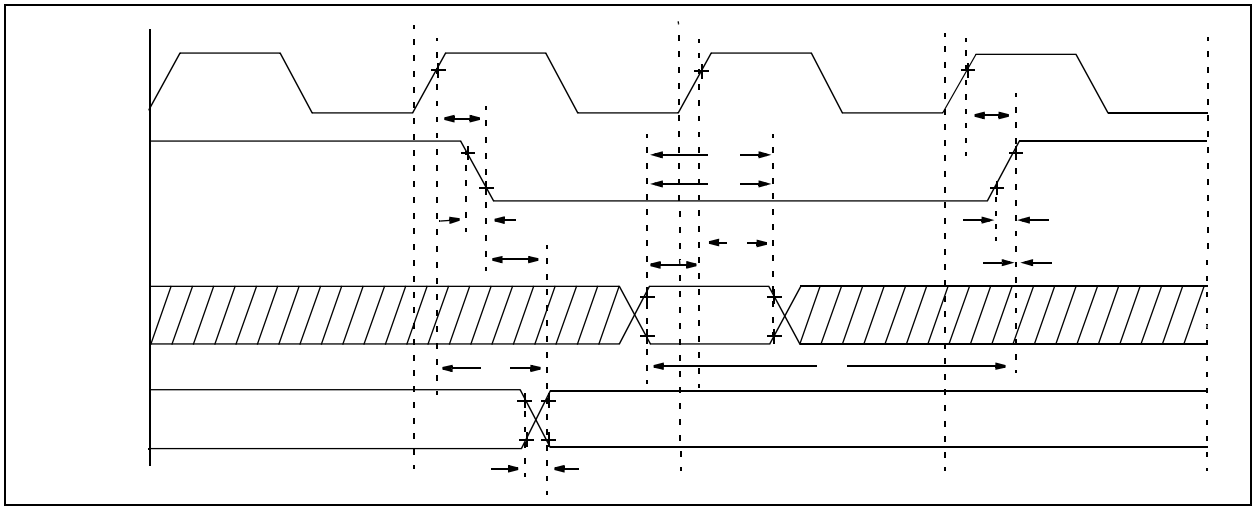


TABLE 17-6: CLKOUT AND I/O TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic		Min	Typ†	Max	Units

FIGURE 17-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

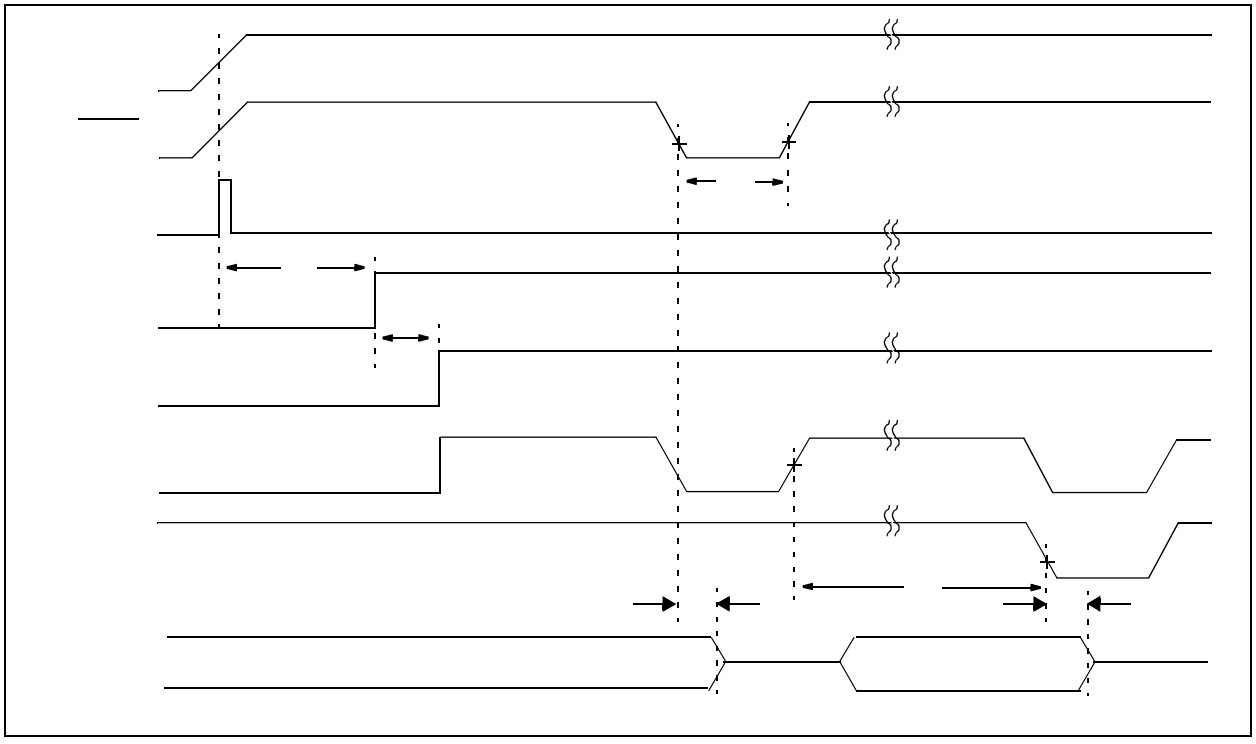


FIGURE 17-7: BROWN-OUT RESET TIMING

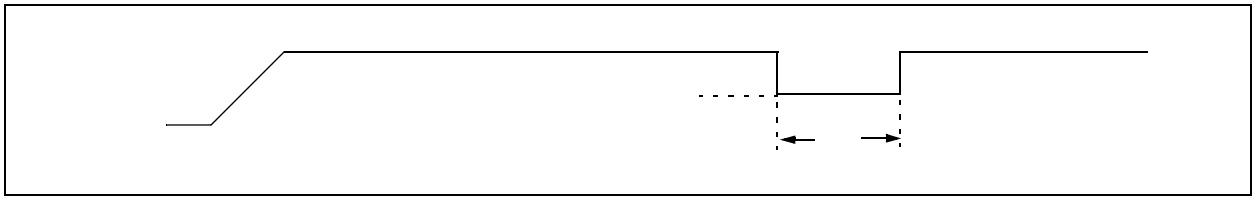


TABLE 17-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions

Legend:

FIGURE 17-8: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

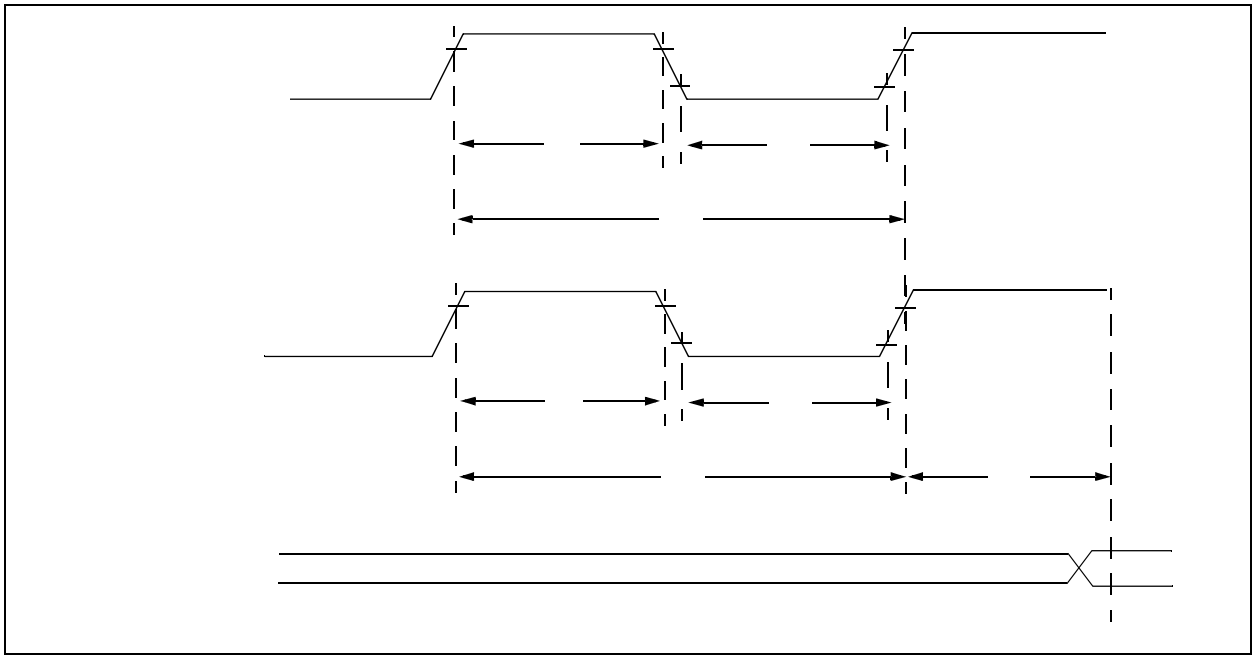


TABLE 17-8: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
				_____				
				_____				
				_____				
					(1)			

Note 1:

FIGURE 17-9: CAPTURE/COMPARE/PWM TIMINGS

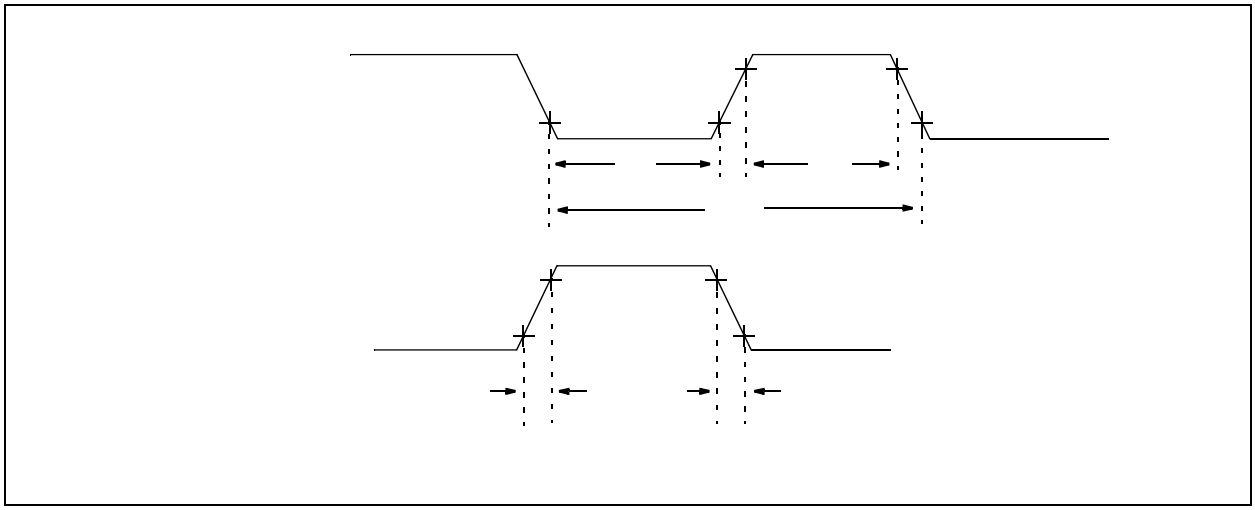


TABLE 17-9: CAPTURE/COMPARE/PWM REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
				—				

NOTES:

18.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

design guidance not tested

outside specified operating range

information only

statistical summary

FIGURE 18-1: TYPICAL BASELINE IPD VS. VDD (-40°C TO 25°C)

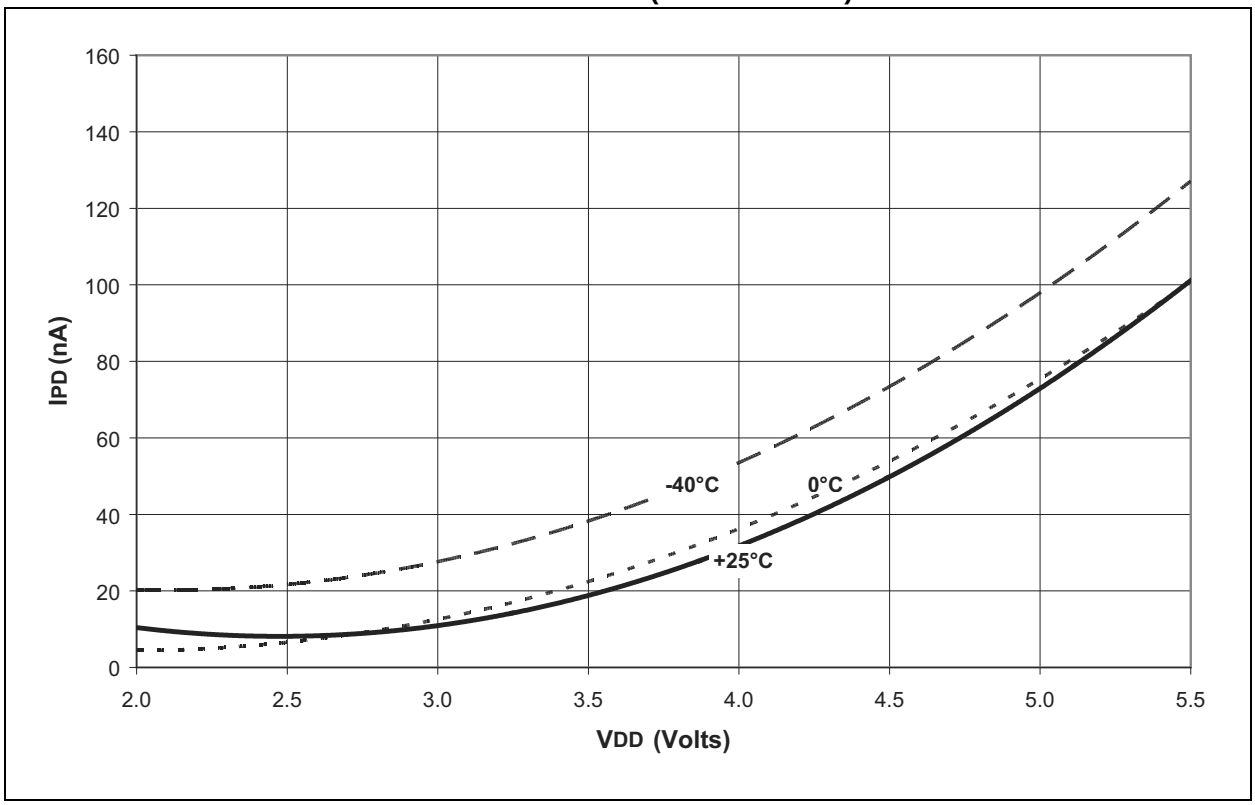


FIGURE 18-2: TYPICAL BASELINE IPD vs. VDD (85°C)

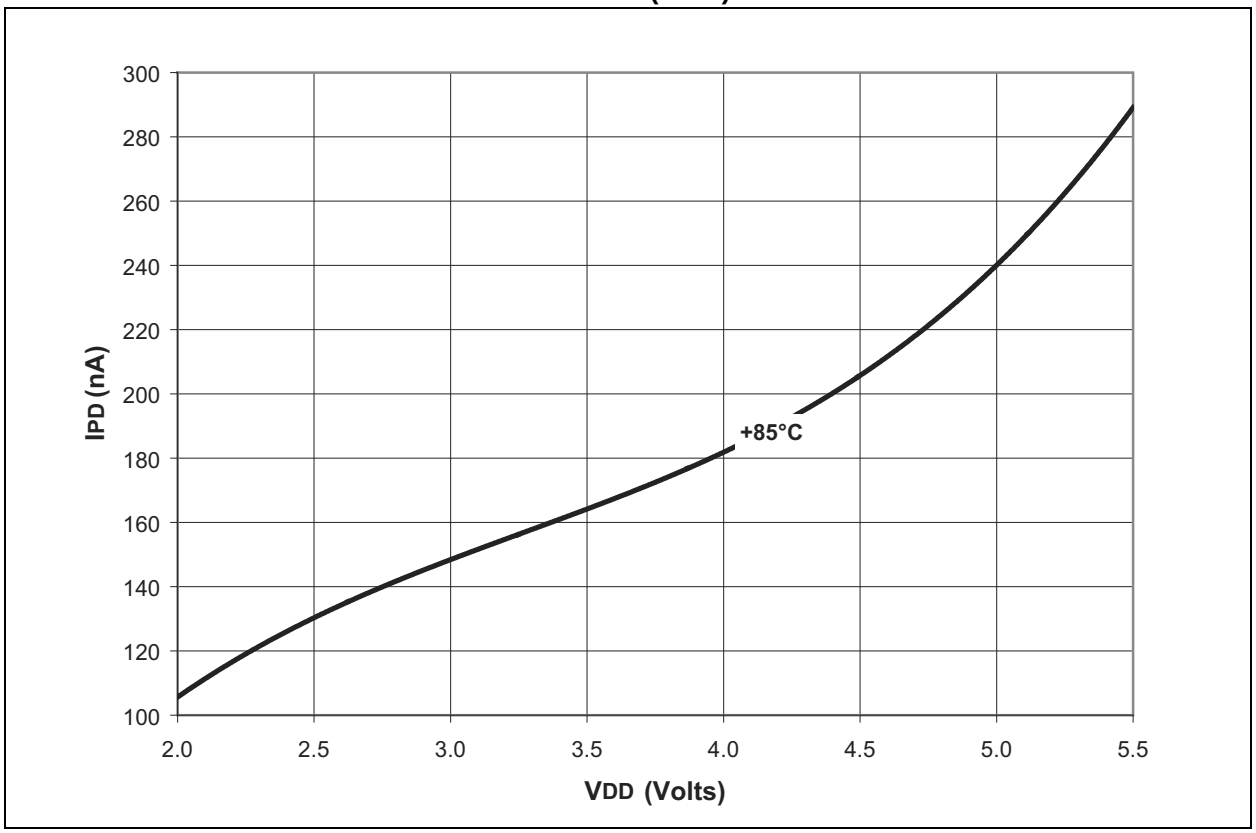


FIGURE 18-3: TYPICAL BASELINE CURRENT IPD vs. VDD (125°C)

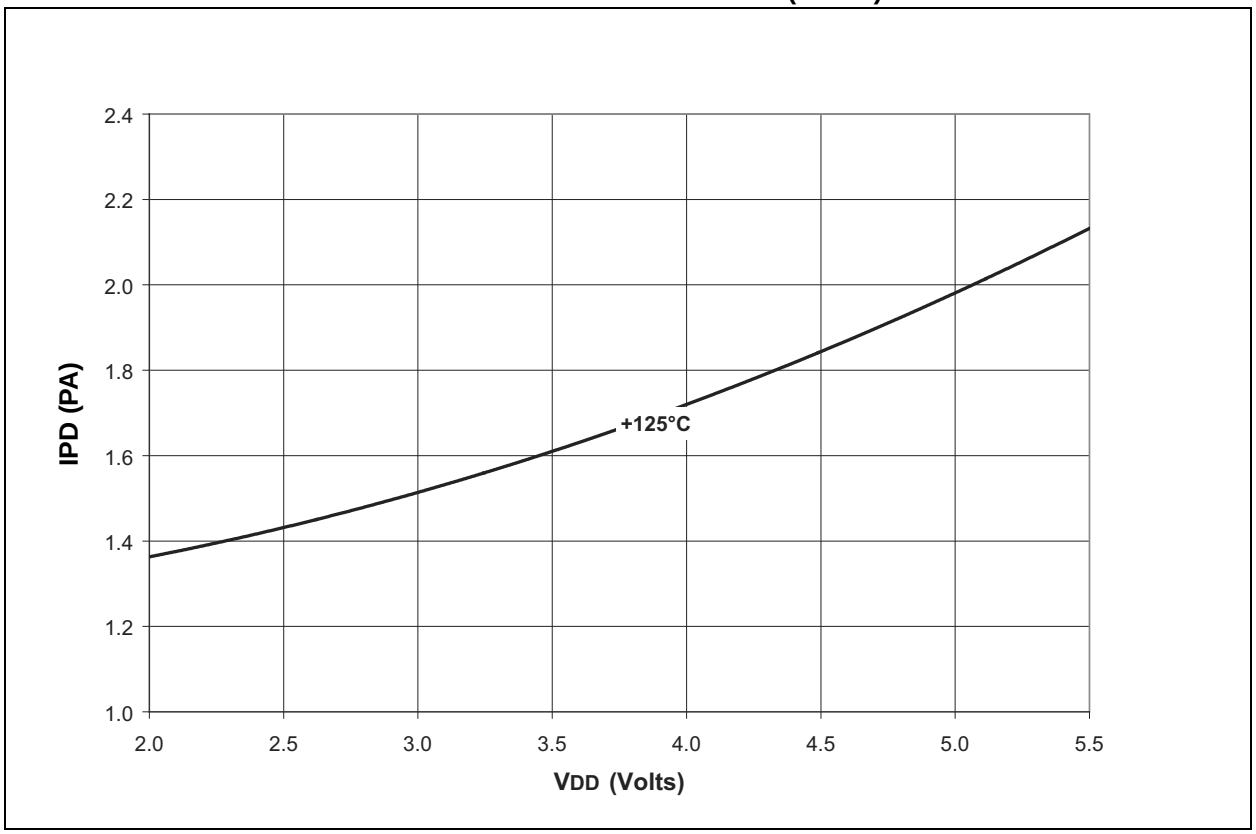


FIGURE 18-4: TYPICAL BOR I_{PD} vs. V_{DD}

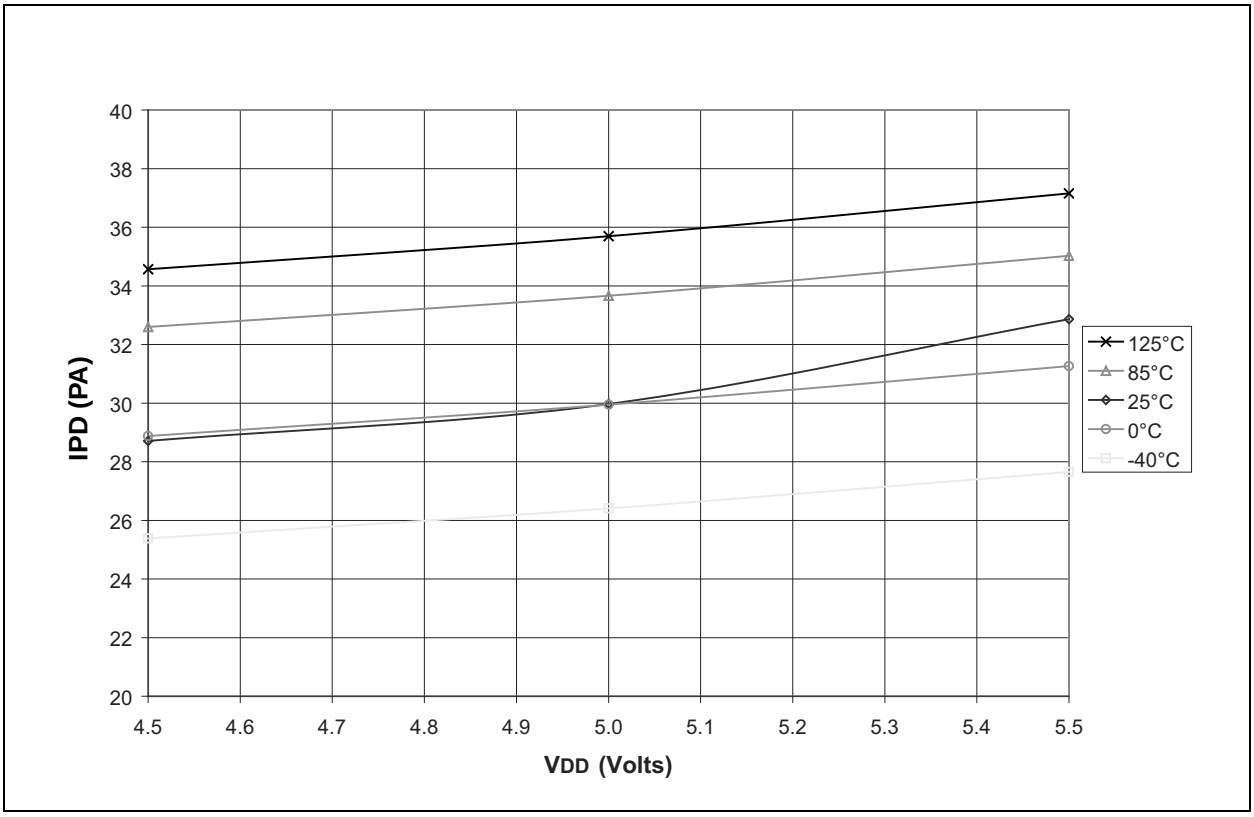


FIGURE 18-5: TYPICAL SINGLE COMPARATOR I_{PD} vs. V_{DD}

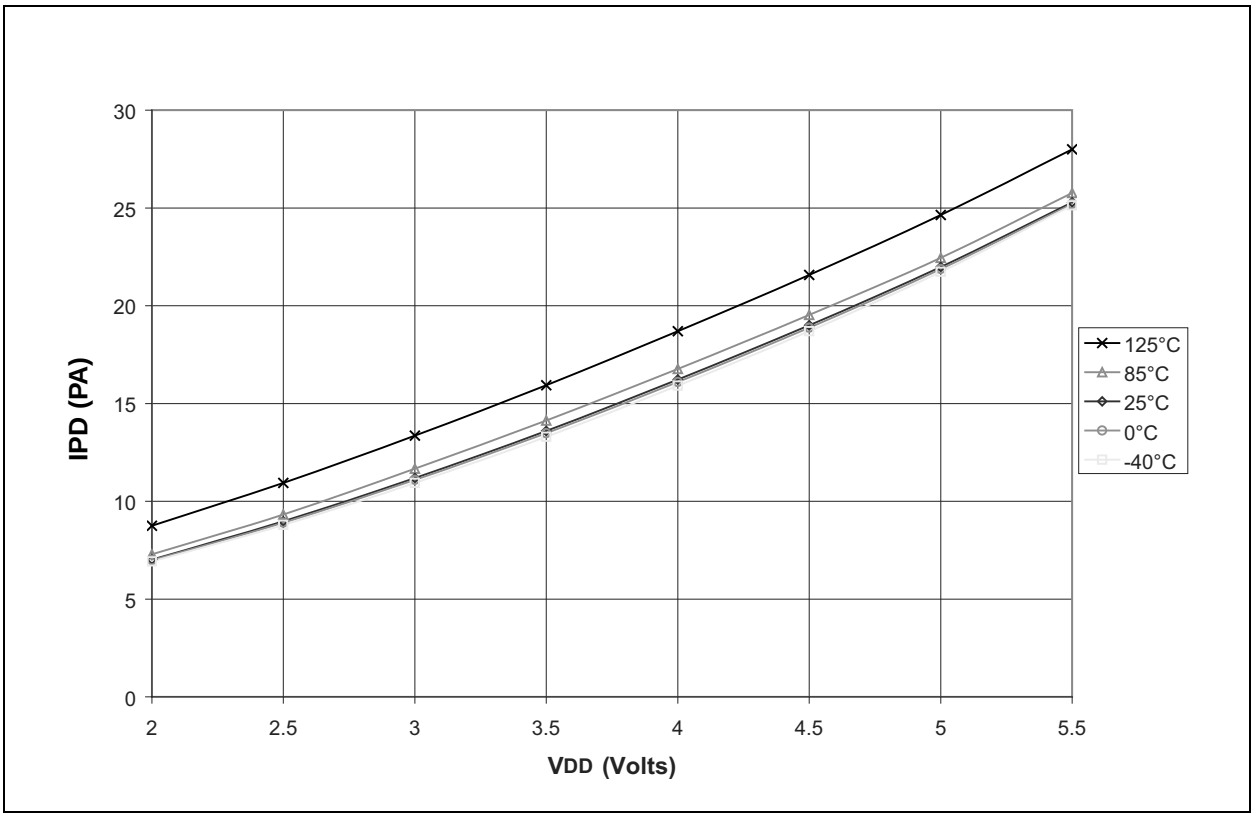


FIGURE 18-6: TYPICAL VREF IPD VS. VDD

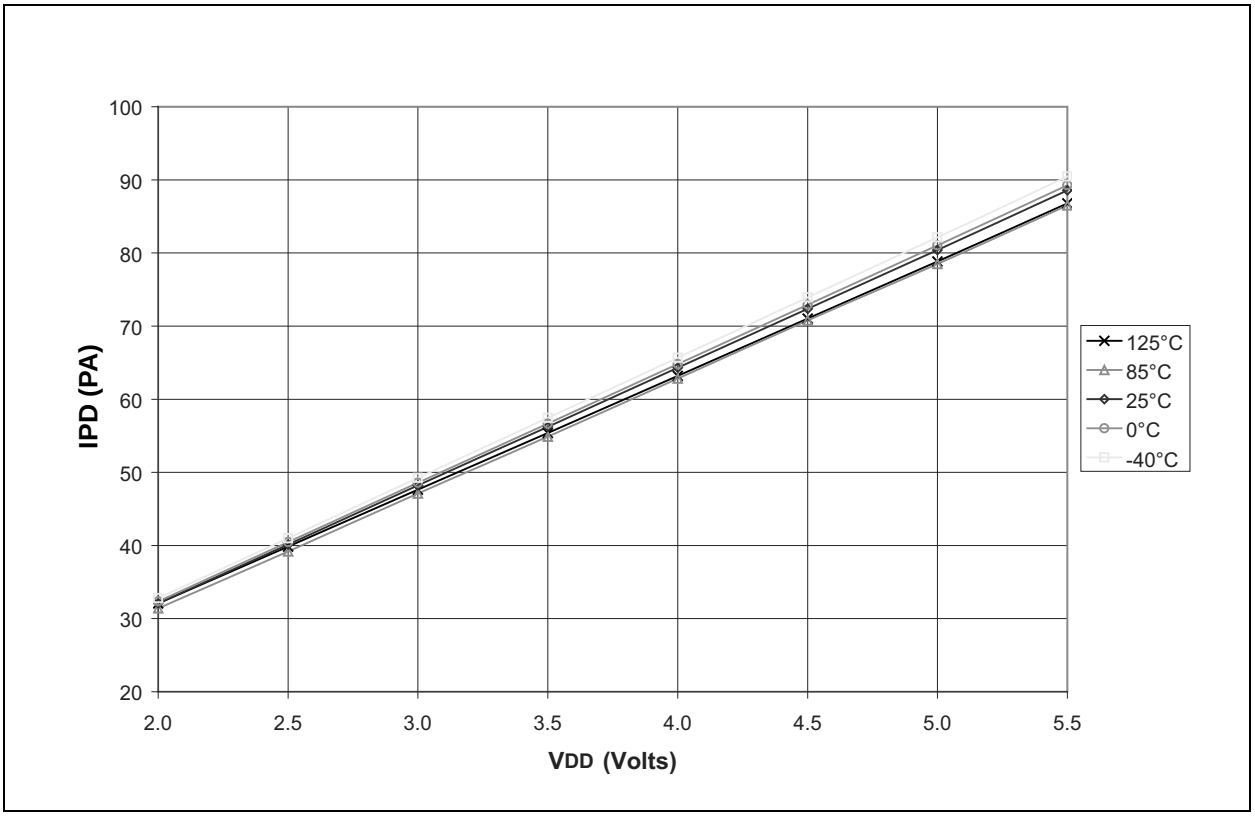


FIGURE 18-7: TYPICAL WDT IPD VS. VDD

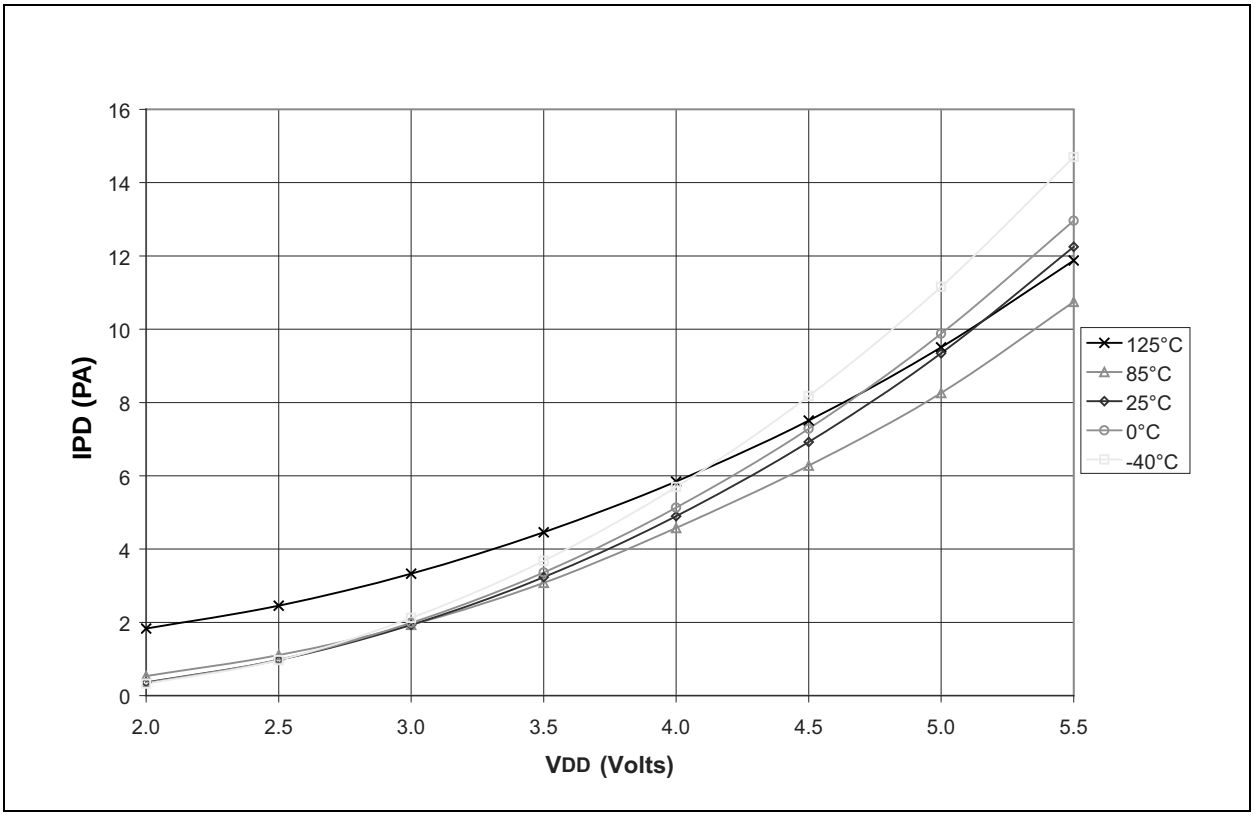


FIGURE 18-8: AVERAGE IPD_TIMER1

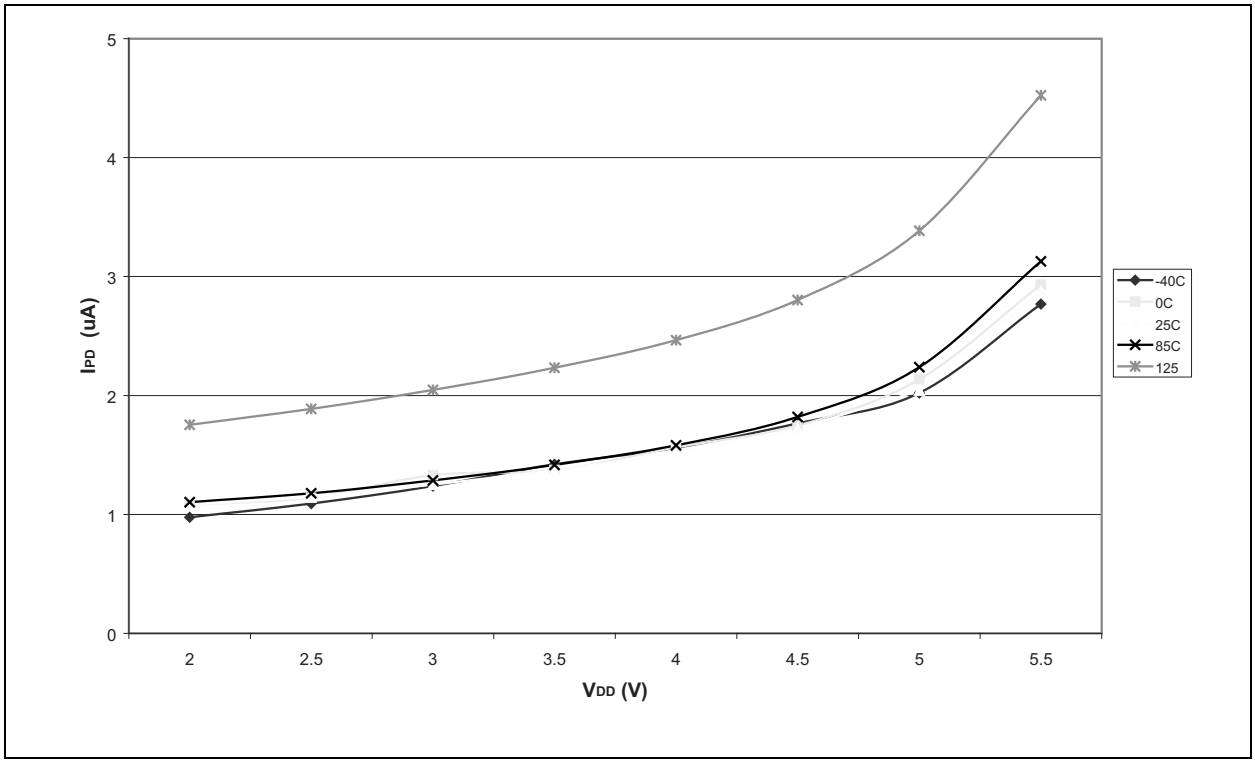


FIGURE 18-9: TYPICAL INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE VDD = 5 VOLTS

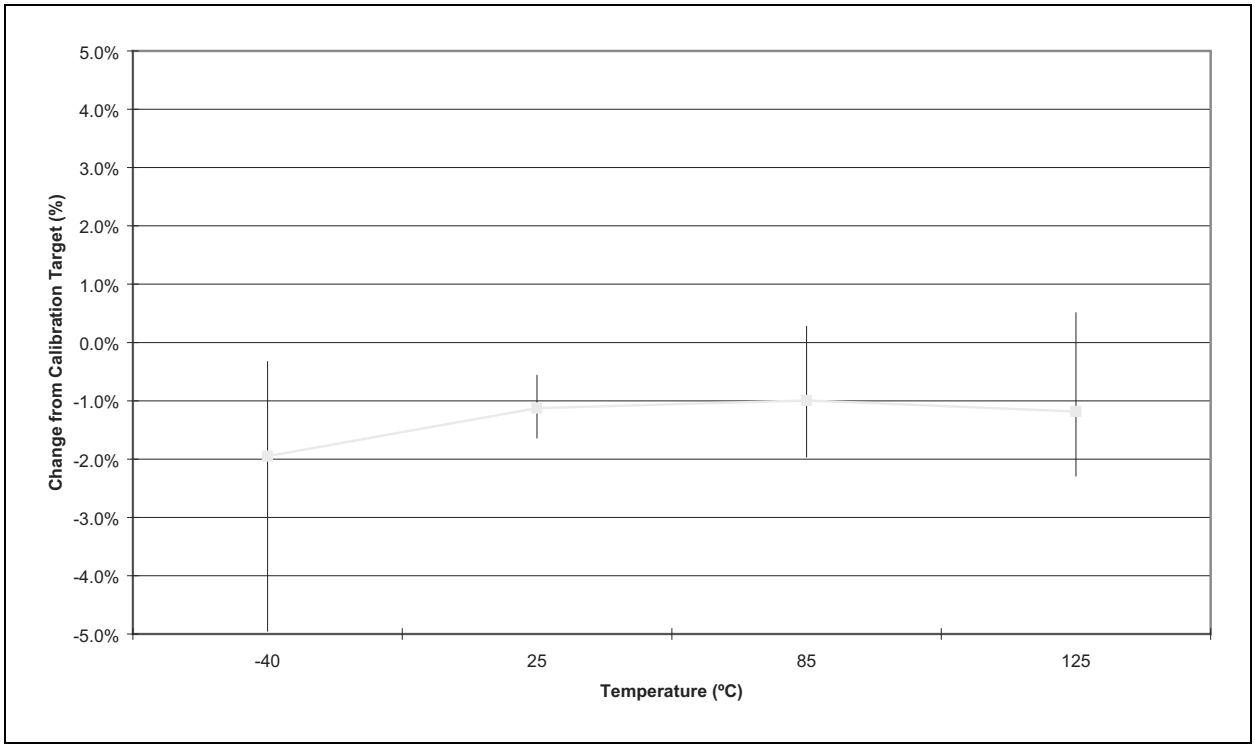


FIGURE 18-10: TYPICAL INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE VDD = 3 VOLTS

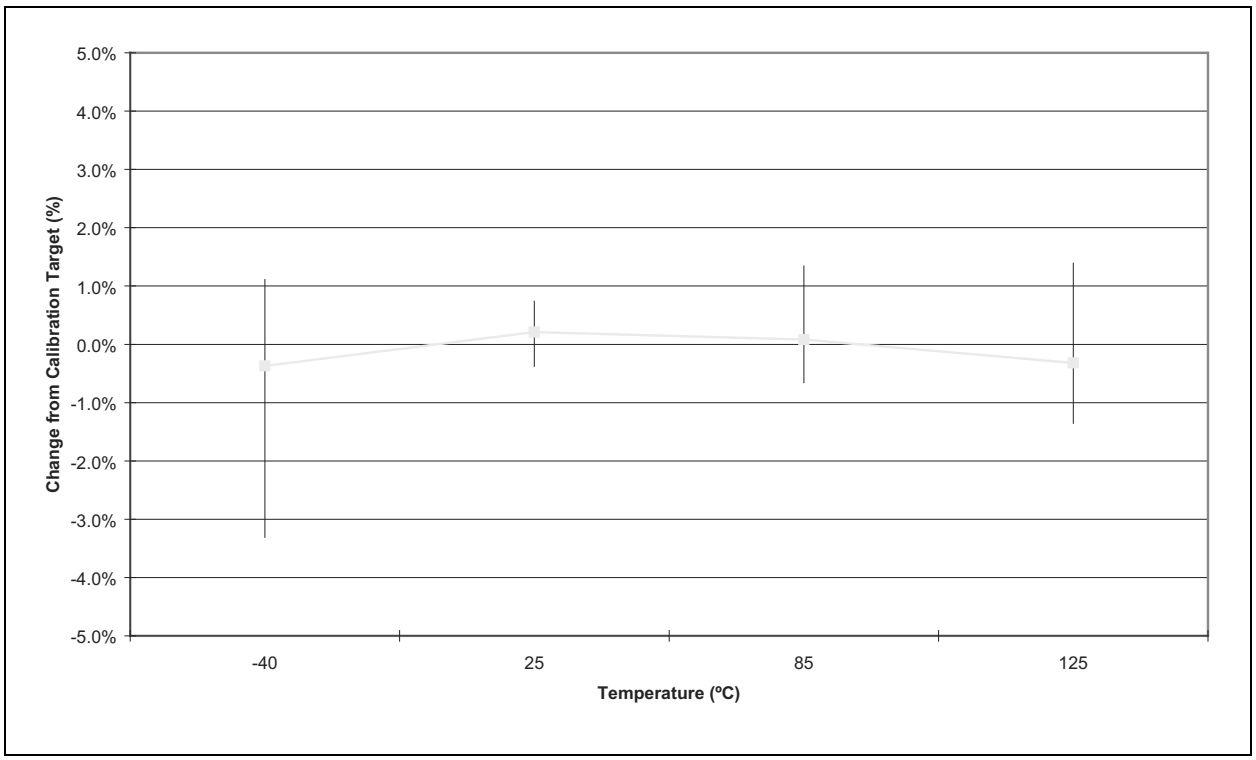


FIGURE 18-11: TYPICAL INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE VDD = 2 VOLTS

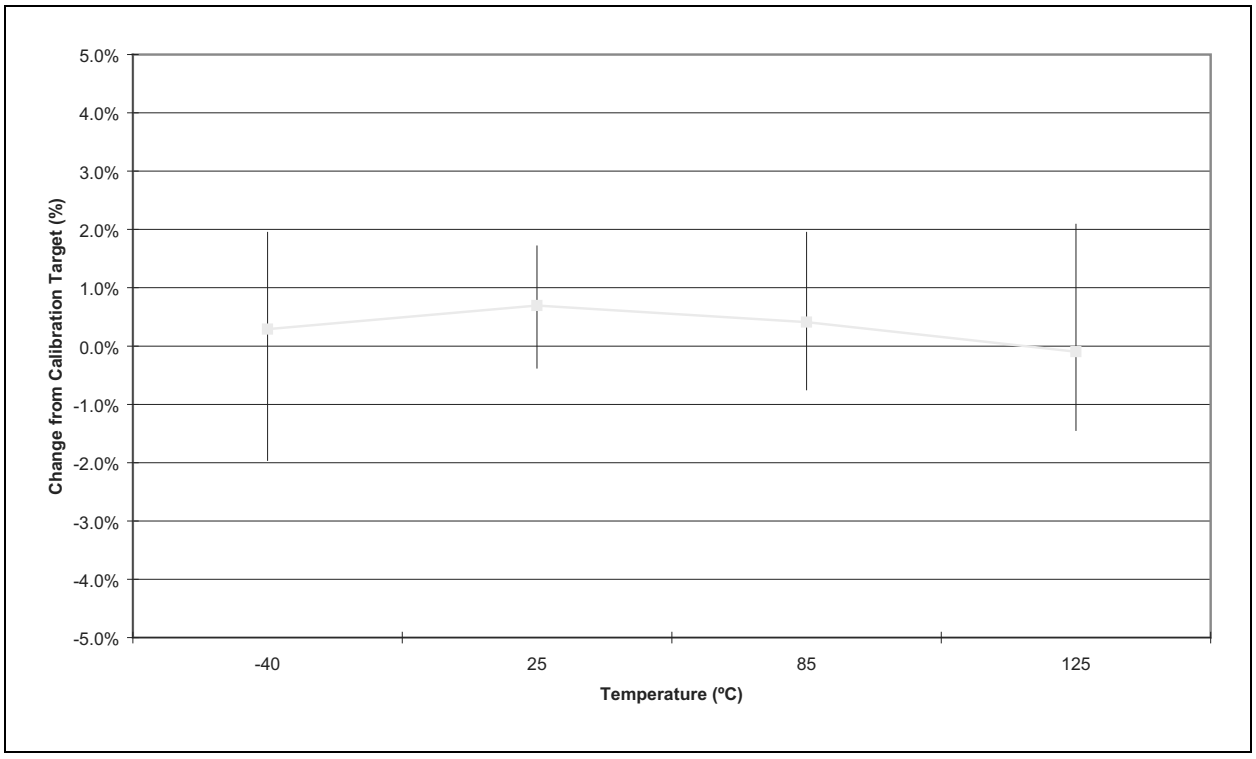


FIGURE 18-12: TYPICAL INTERNAL OSCILLATOR DEVIATION vs. VDD AT 25°C – 4 MHz MODE

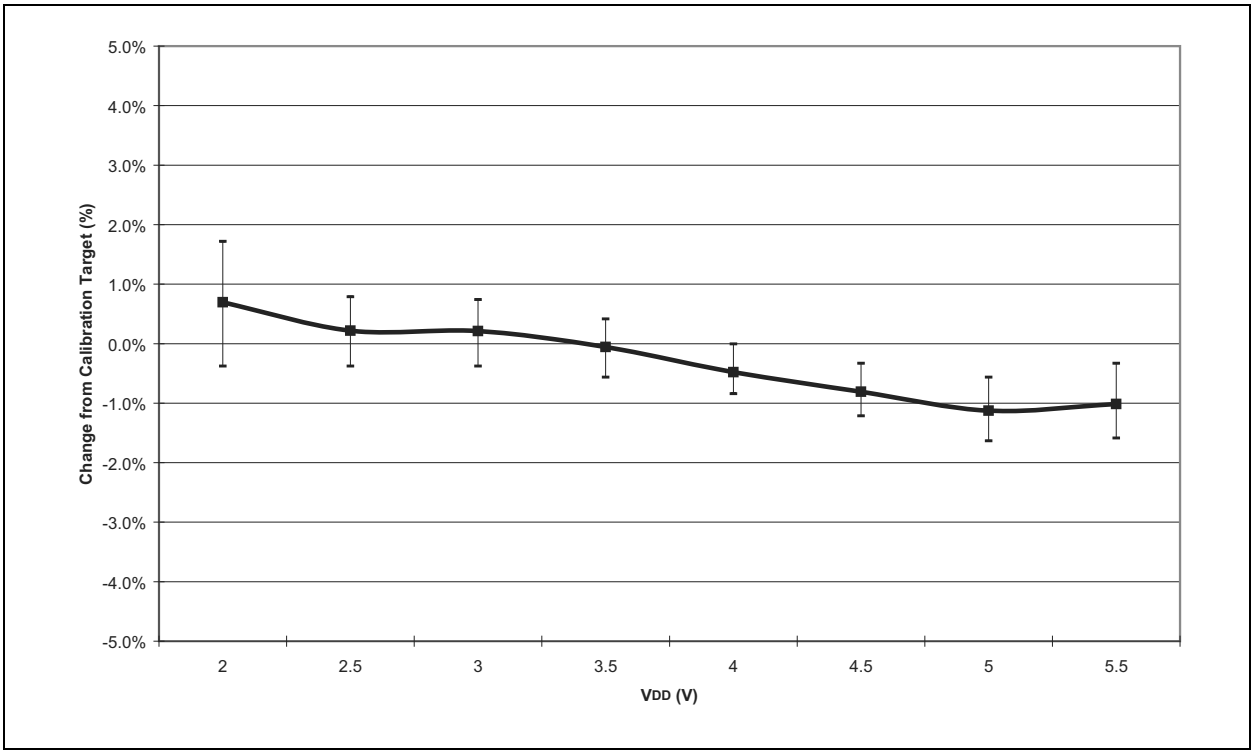


FIGURE 18-13: TYPICAL INTERNAL OSCILLATOR FREQUENCY vs. VDD TEMPERATURE = -40°C TO 85°C

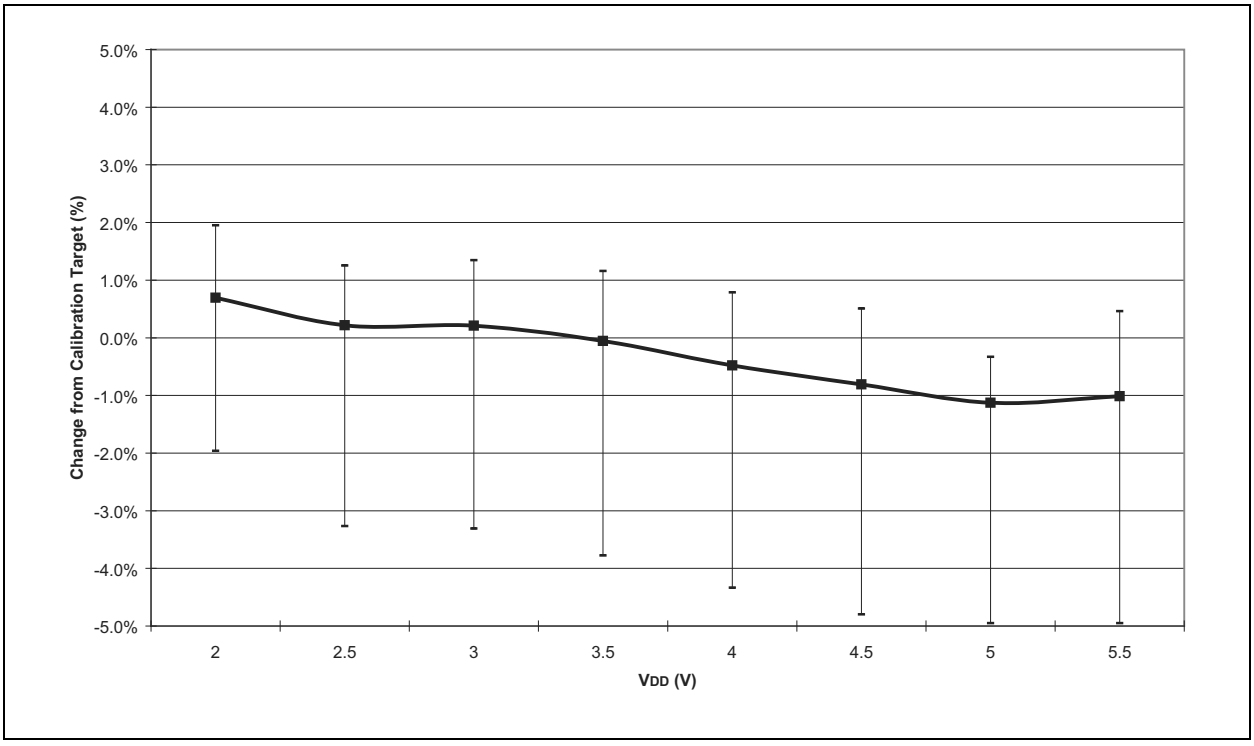


FIGURE 18-14: INTERNAL OSCILLATOR IDD vs. VDD – 4 MHz MODE

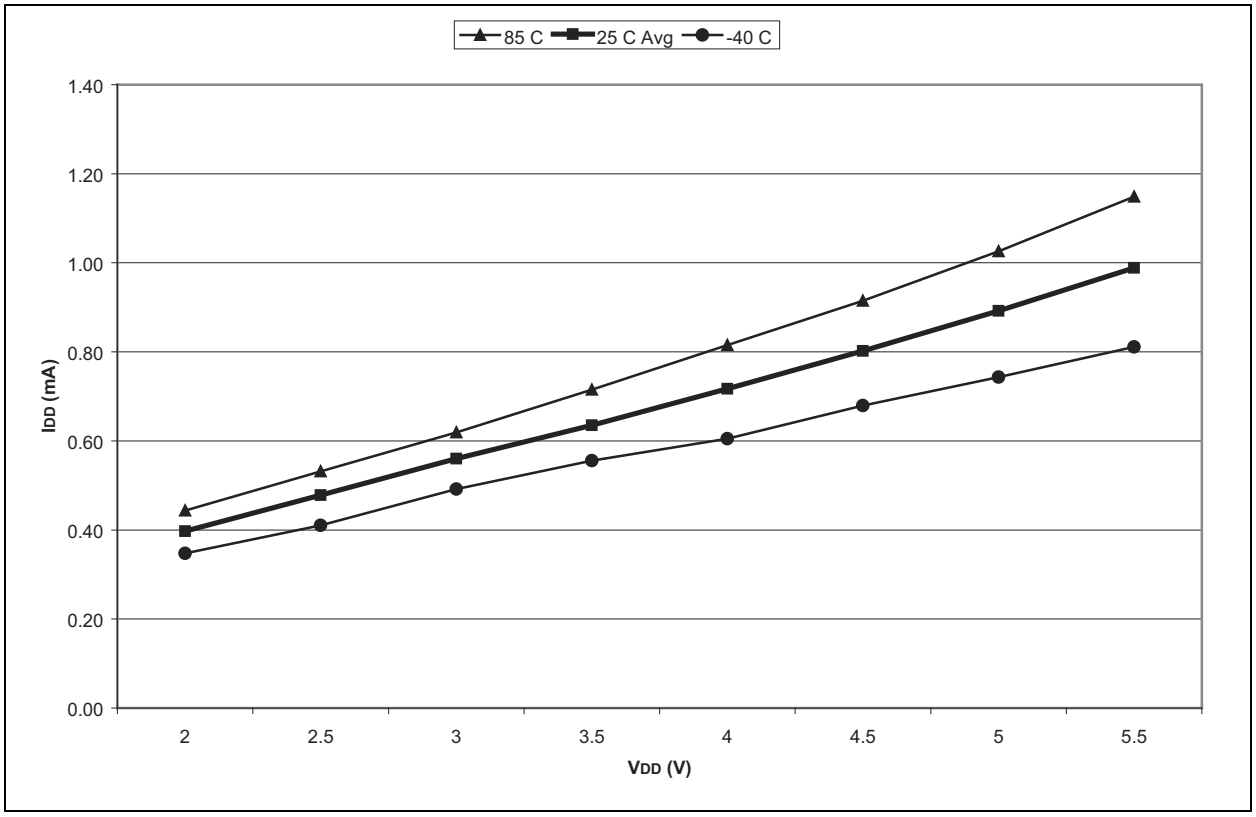


FIGURE 18-15: TYPICAL INTERNAL OSCILLATOR FREQUENCY vs. VDD AT 25°C – SLOW MODE

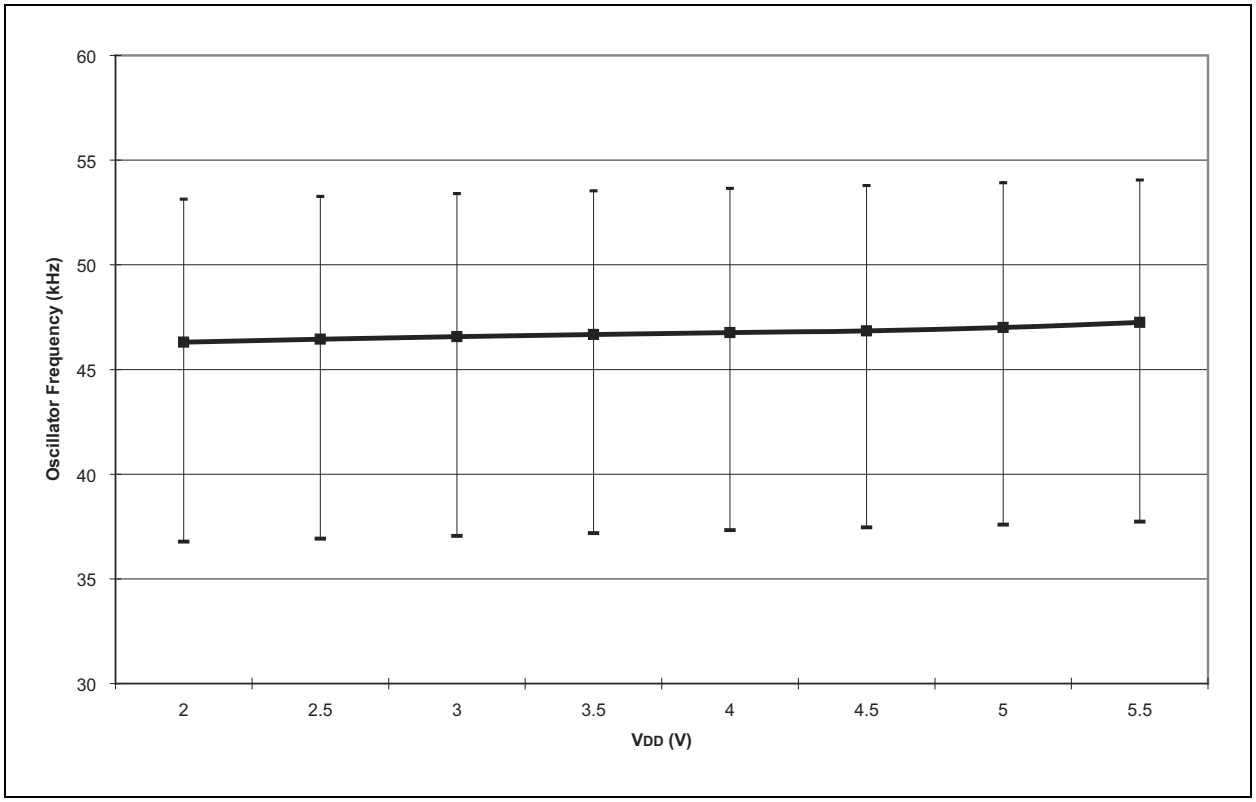


FIGURE 18-16: INTERNAL OSCILLATOR IDD vs. VDD – SLOW MODE

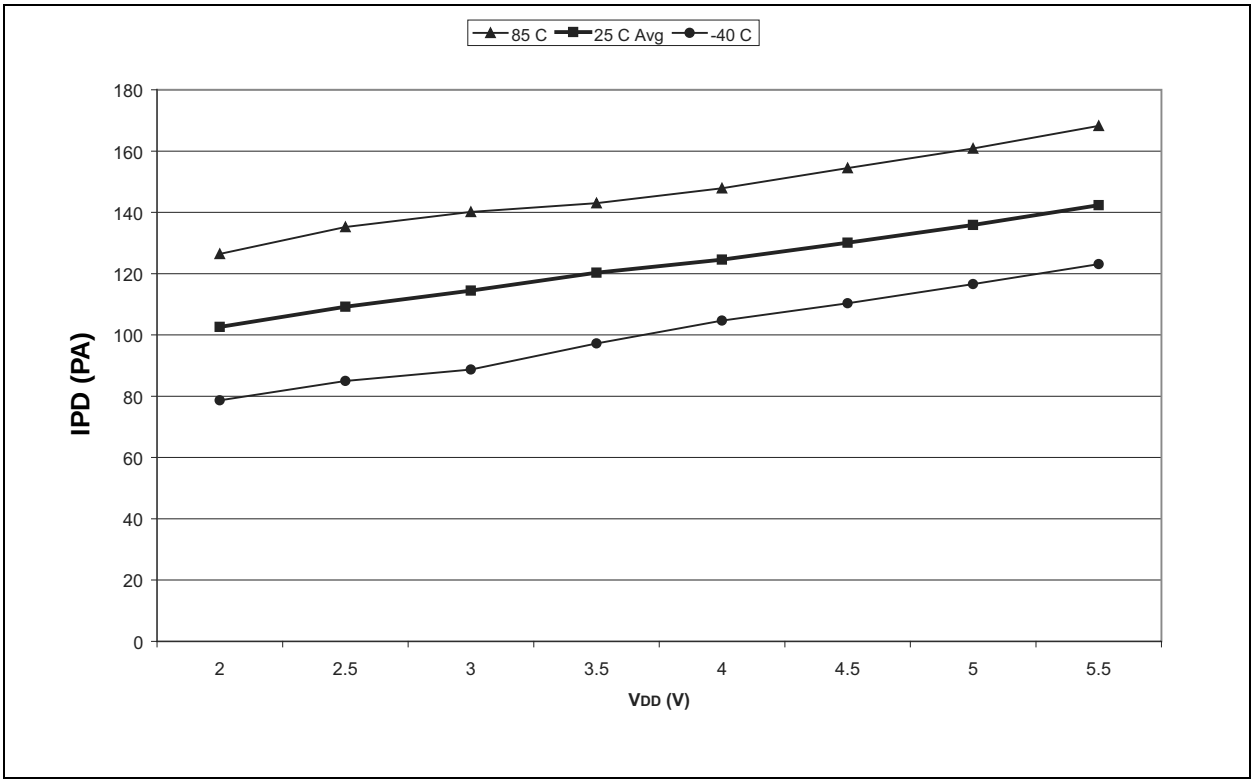


FIGURE 18-17: SUPPLY CURRENT (IDD vs. VDD, FOSC = 1 MHz (XT OSCILLATOR MODE)

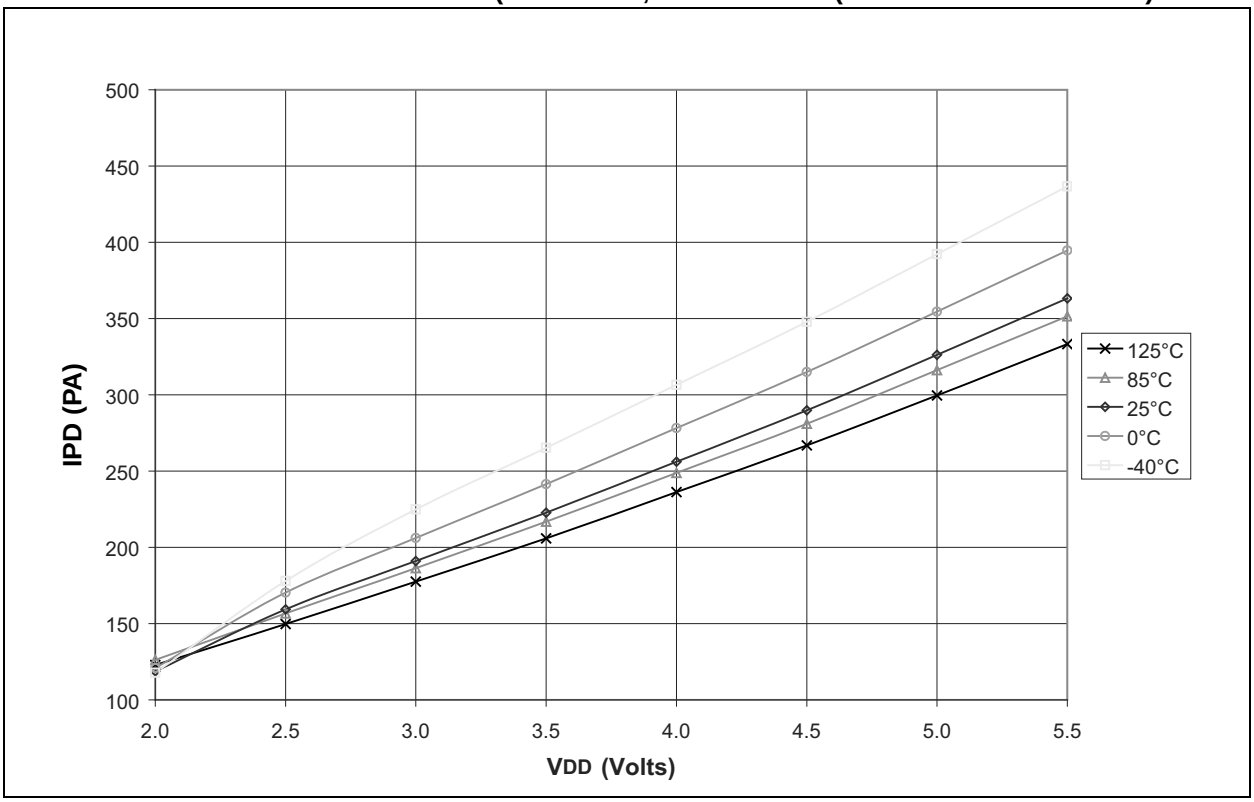


FIGURE 18-18: SUPPLY CURRENT (IDD vs. VDD, FOSC = 4 MHz (XT OSCILLATOR MODE)

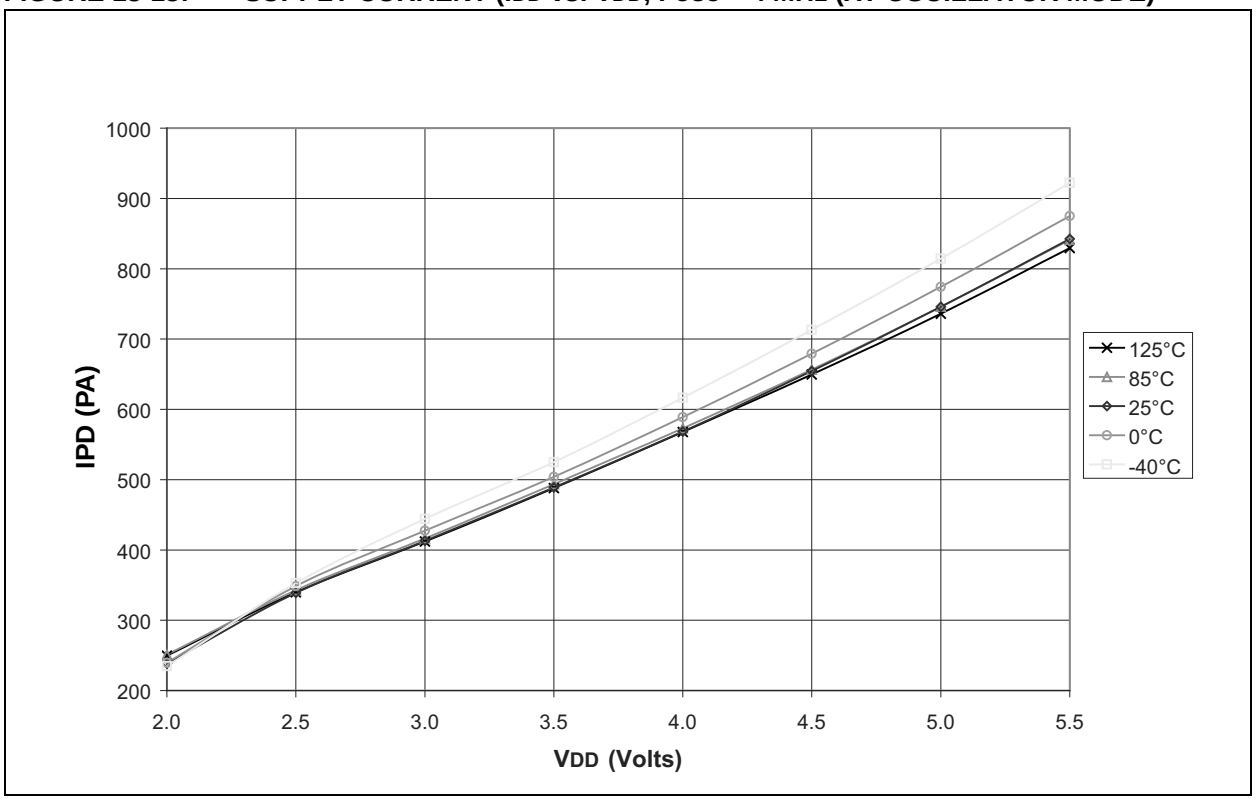


FIGURE 18-19: SUPPLY CURRENT (IDD) vs. VDD, FOSC = 20 MHz (HS OSCILLATOR MODE)

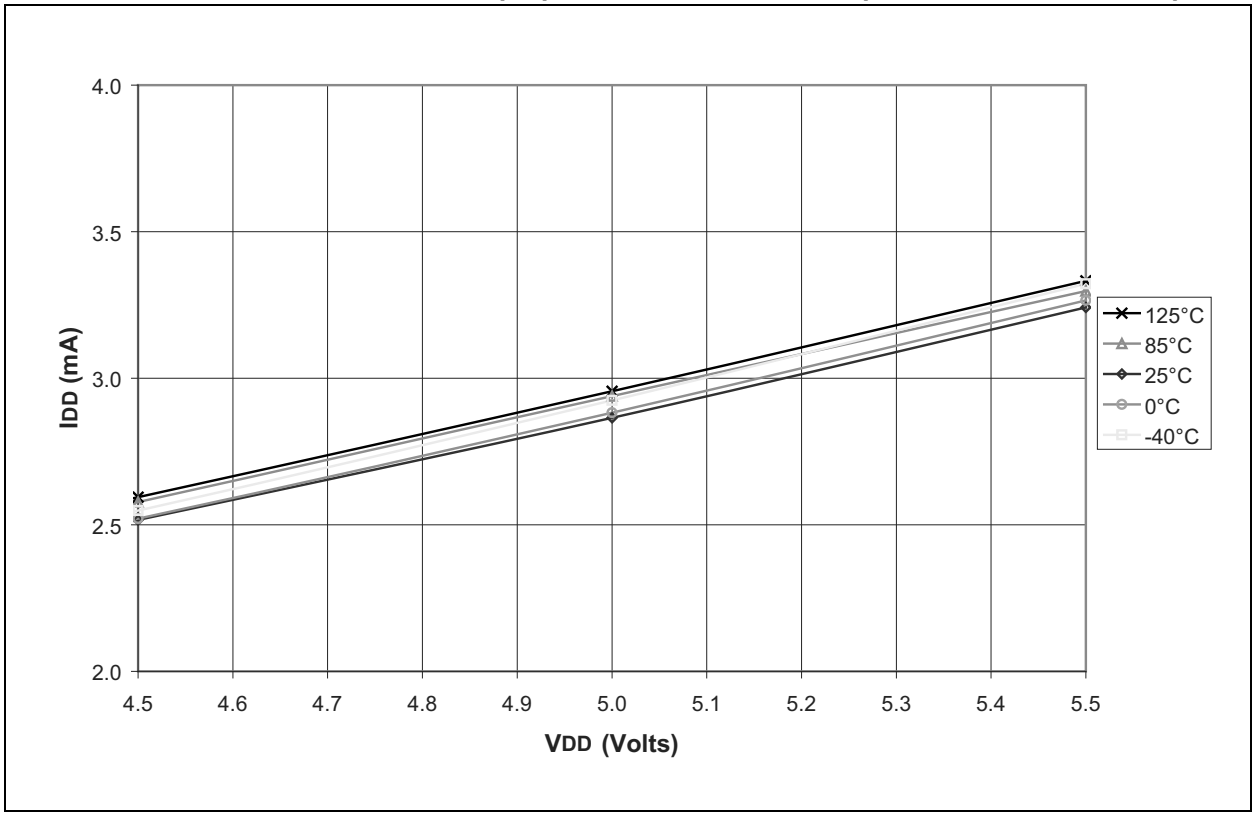
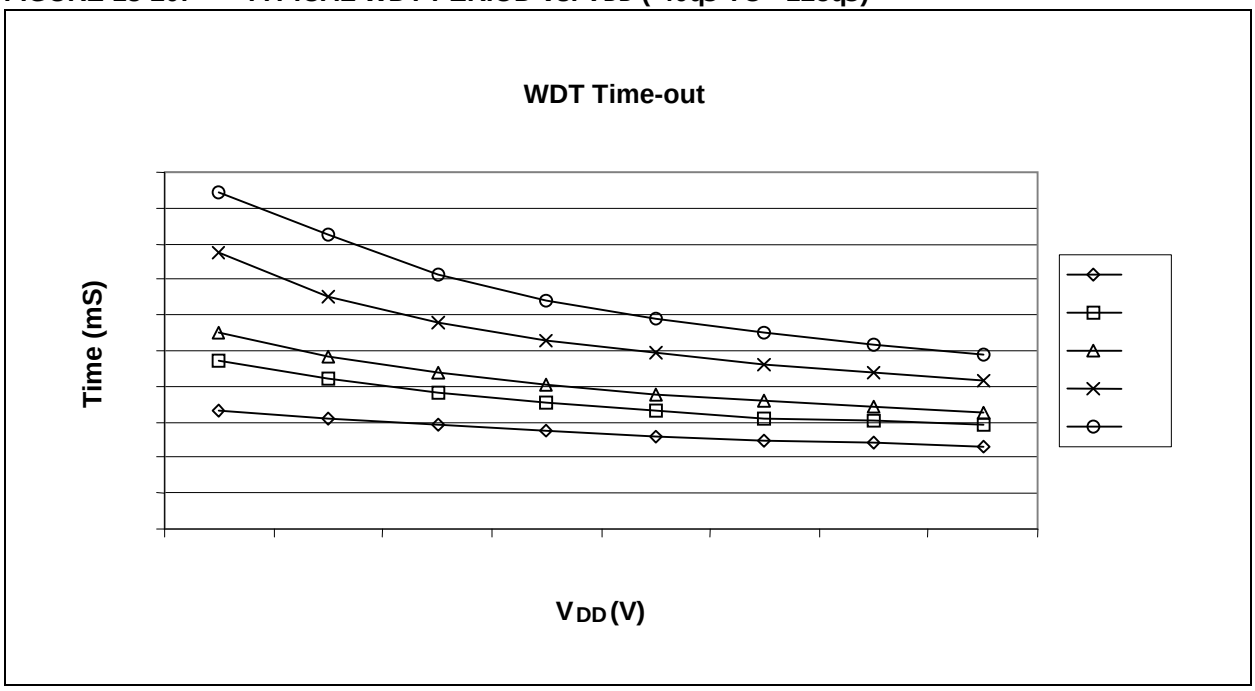


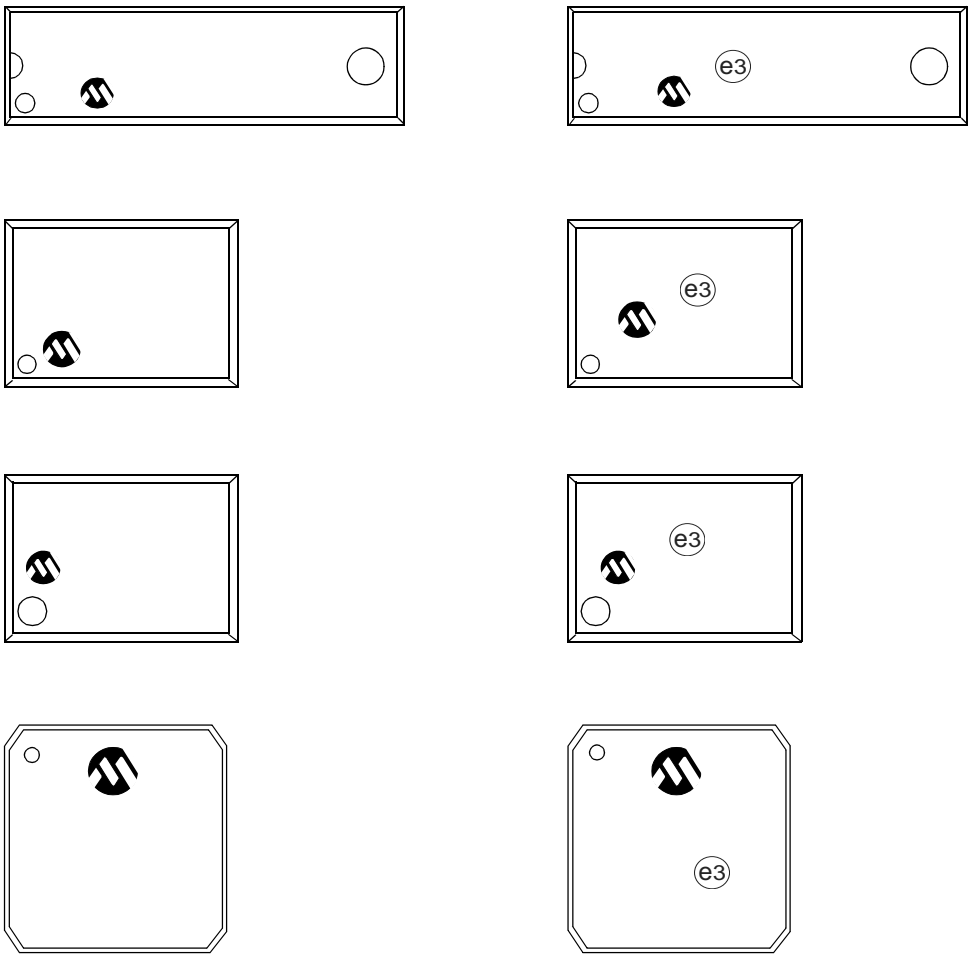
FIGURE 18-20: TYPICAL WDT PERIOD vs. V_{DD} (-40°C TO +125°C)



NOTES:

19.0 PACKAGING INFORMATION

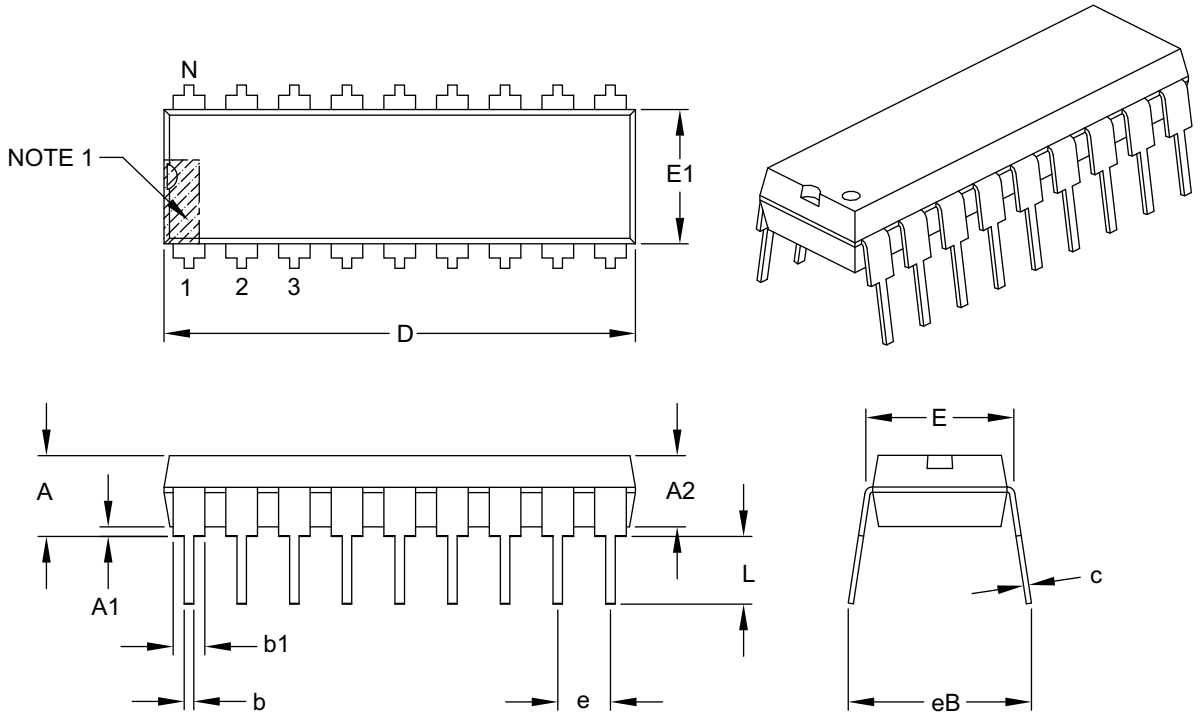
19.1 Package Marking Information



Legend:
e3 * e3
Note

18-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		18	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.880	.900	.920
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.014
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

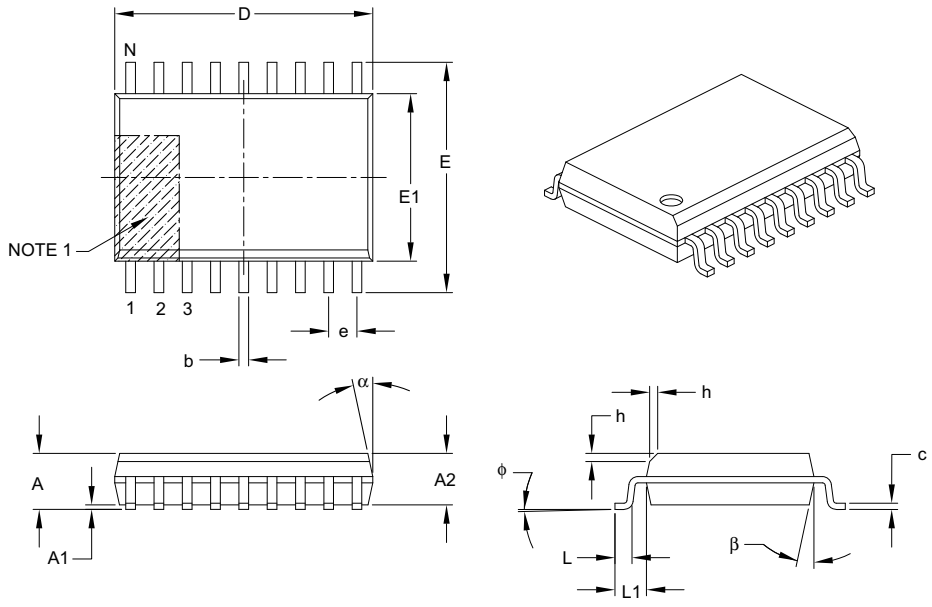
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-007B

18-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		18	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	2.65
Molded Package Thickness	A2	2.05	–	–
Standoff §	A1	0.10	–	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		11.55 BSC	
Chamfer (optional)	h	0.25	–	0.75
Foot Length	L	0.40	–	1.27
Footprint	L1		1.40 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.20	–	0.33
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

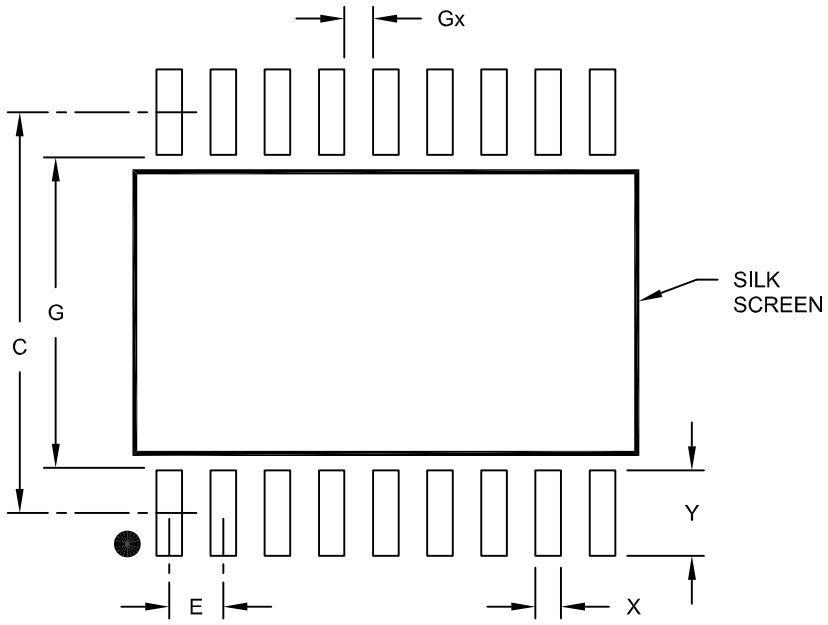
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-051B

18-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

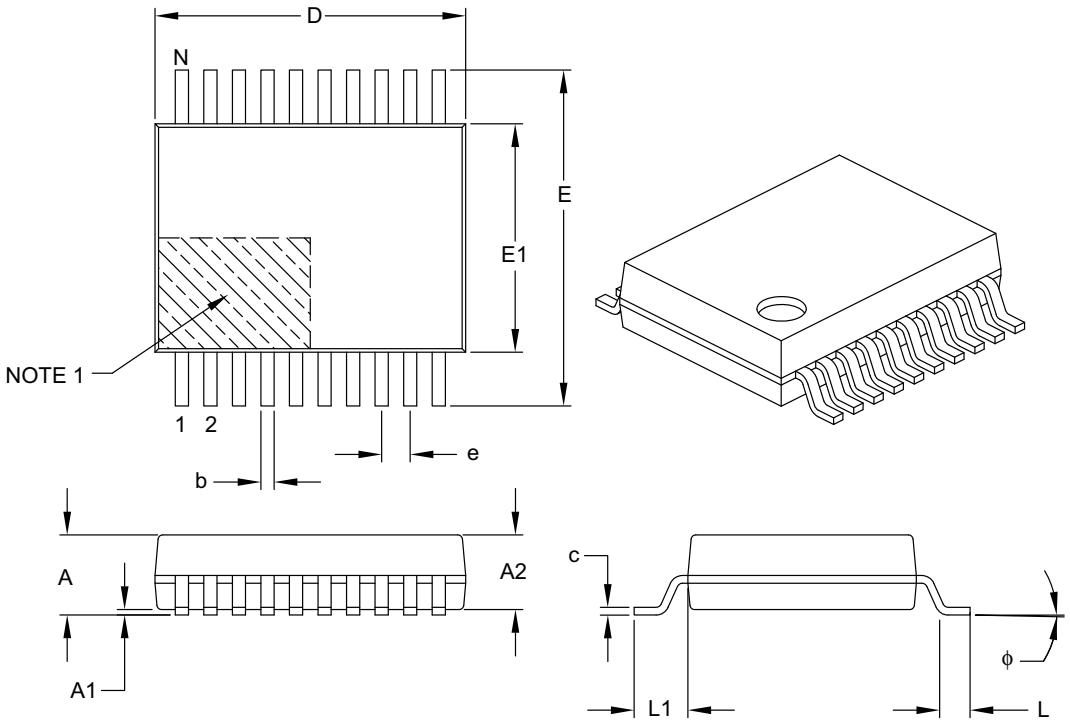
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2051A

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1		1.25 REF	
Lead Thickness	c	0.09	–	0.25
Foot Angle	ϕ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

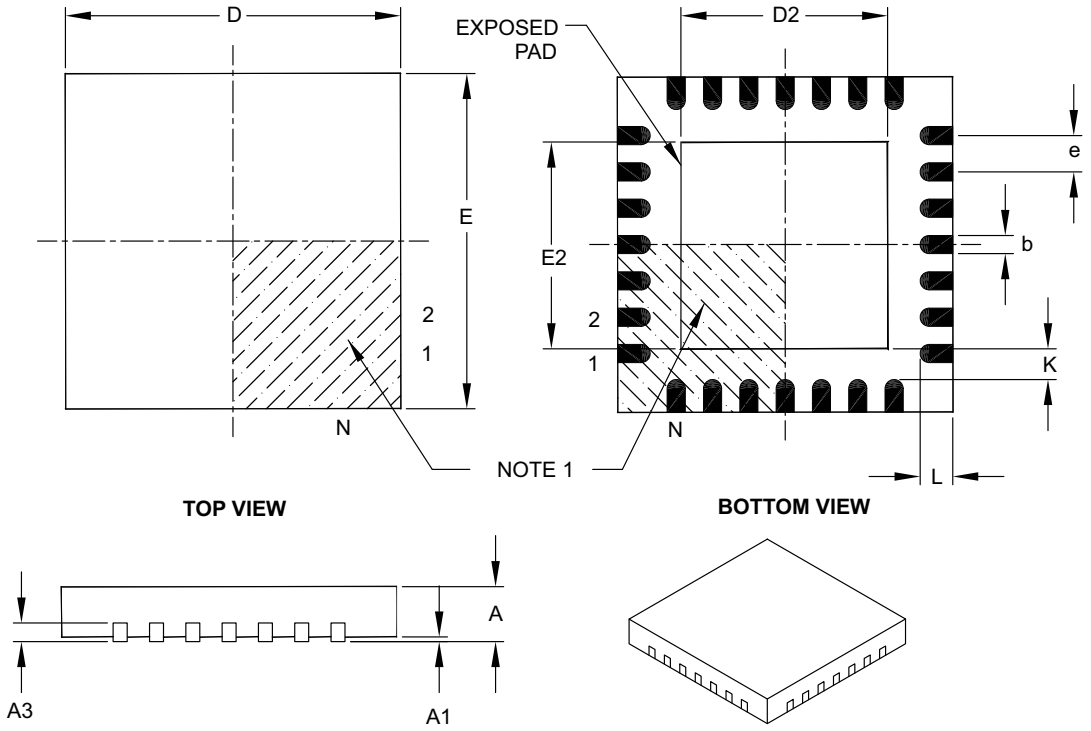
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		6.00 BSC	
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	3.65	3.70	4.20
Contact Width	b	0.23	0.30	0.35
Contact Length	L	0.50	0.55	0.70
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

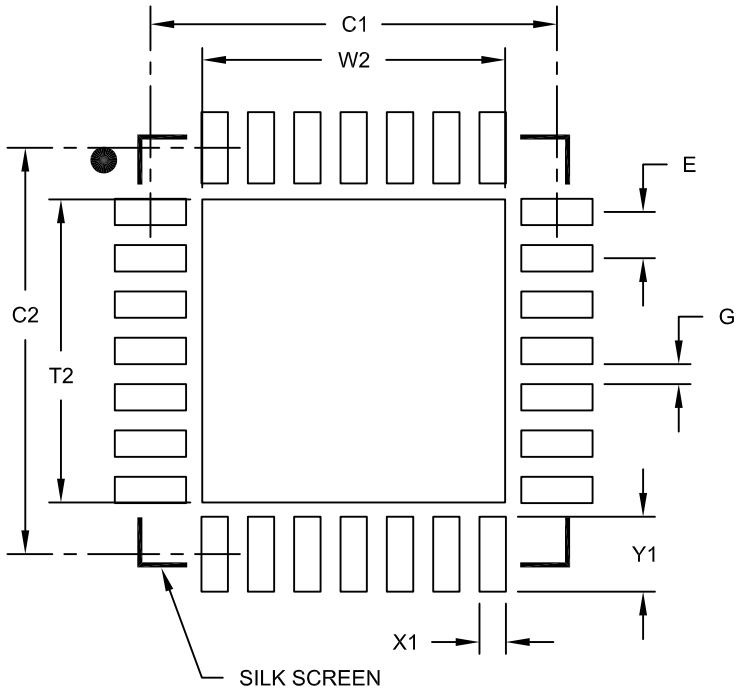
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN]
with 0.55 mm Contact Length

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

NOTES:

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A

Revision B

Revision C

Revision D

Revision E

Revision F (03/2007)

Revision G (10/2009)

APPENDIX B: DEVICE DIFFERENCES

TABLE B-1: DEVICE DIFFERENCES

Device	Memory		
	Flash Program	RAM Data	EEPROM Data

APPENDIX C: DEVICE MIGRATIONS

C.1 PIC16F627/628 PIC16F627A/628A

APPENDIX D: MIGRATING FROM OTHER PIC® DEVICES

D.1 PIC16C62X/CE62X to PIC16F627A/628A/648A Migration

D.2 PIC16C622A to PIC16F627A/628A/648A Migration

Note:

THE MICROCHIP WEB SITE

Product Support

General Technical Support

Business of Microchip

CUSTOMER SUPPORT

Technical support is available through the web site at: http://support.microchip.com

CUSTOMER CHANGE NOTIFICATION SERVICE

READER RESPONSE

INDEX

A

B

C

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See
See

D

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Q

R

S

See

U

T

V

W

X

PRODUCT IDENTIFICATION SYSTEM

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device:

Temperature Range:

Package:

Examples:

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

Atlanta

Boston

Chicago

Cleveland

Dallas

Detroit

Kokomo

Los Angeles

Santa Clara

Toronto

ASIA/PACIFIC

Asia Pacific Office

Australia - Sydney

China - Beijing

China - Chengdu

China - Hong Kong SAR

China - Nanjing

China - Qingdao

China - Shanghai

China - Shenyang

China - Shenzhen

China - Wuhan

China - Xiamen

China - Xian

China - Zhuhai

ASIA/PACIFIC

India - Bangalore

India - New Delhi

India - Pune

Japan - Yokohama

Korea - Daegu

Korea - Seoul

Malaysia - Kuala Lumpur

Malaysia - Penang

Philippines - Manila

Singapore

Taiwan - Hsin Chu

Taiwan - Kaohsiung

Taiwan - Taipei

Thailand - Bangkok

EUROPE

Austria - Wels

Denmark - Copenhagen

France - Paris

Germany - Munich

Italy - Milan

Netherlands - Drunen

Spain - Madrid

UK - Wokingham