

# SN54HC125, SN74HC125 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCLS104B – MARCH 1984 – REVISED MAY 1997

- High-Current 3-State Outputs Interface Directly With System Bus or Can Drive up to 15 LSTTL Loads
- Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

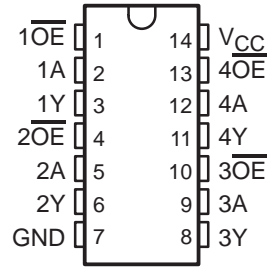
These quadruple bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ( $\overline{OE}$ ) input is high.

The SN54HC125 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC125 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

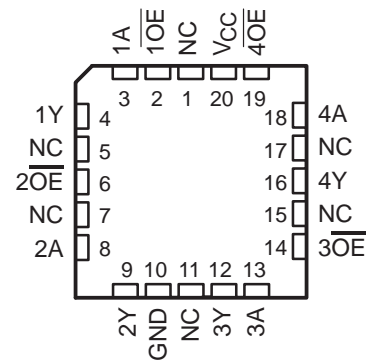
FUNCTION TABLE  
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

SN54HC125 . . . J OR W PACKAGE  
SN74HC125 . . . D, DB, OR N PACKAGE  
(TOP VIEW)

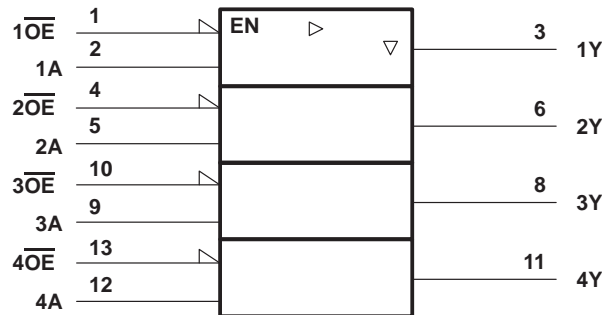


SN54HC125 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the D, DB, J, N, and W packages.



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**TEXAS  
INSTRUMENTS**

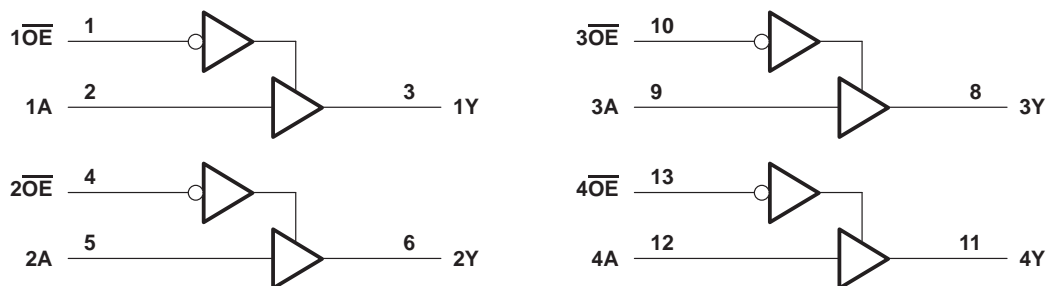
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## logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, and W packages.

## absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 35$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 70$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package .....	127°C/W
DB package .....	158°C/W
N package .....	78°C/W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

## recommended operating conditions

		SN54HC125			SN74HC125			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5			V
		$V_{CC} = 4.5$ V	3.15		3.15			
		$V_{CC} = 6$ V	4.2		4.2			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0	0.5	0	0.5		V
		$V_{CC} = 4.5$ V	0	1.35	0	1.35		
		$V_{CC} = 6$ V	0	1.8	0	1.8		
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$t_t$	Input transition (rise and fall) time	$V_{CC} = 2$ V	0	1000	0	1000		ns
		$V_{CC} = 4.5$ V	0	500	0	500		
		$V_{CC} = 6$ V	0	400	0	400		
$T_A$	Operating free-air temperature	-55		125	-40		85	°C



**SN54HC125, SN74HC125**  
**QUADRUPLE BUS BUFFER GATES**  
**WITH 3-STATE OUTPUTS**

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC125		SN74HC125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998		1.9		1.9	V	
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I <sub>OH</sub> = -6 mA	4.5 V	3.98	4.3		3.7		3.84		
		I <sub>OH</sub> = -7.8 mA	6 V	5.48	5.8		5.2		5.34		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I <sub>OL</sub> = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		I <sub>OL</sub> = 7.8 mA	6 V		0.15	0.26		0.4		0.33	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V		±0.1	±100		±1000		±1000	nA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or 0		6 V		±0.01	±0.5		±10		±5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V			8		160		80	μA
C <sub>i</sub>			2 V to 6 V		3	10		10		10	pF

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC125		SN74HC125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	2 V		48	120		150		150	ns
			4.5 V		14	24		36		30	
			6 V		11	20		25		26	
t <sub>en</sub>	$\overline{\text{OE}}$	Y	2 V		53	120		180		150	ns
			4.5 V		14	24		36		30	
			6 V		11	20		31		26	
t <sub>dis</sub>	$\overline{\text{OE}}$	Y	2 V		30	120		180		150	ns
			4.5 V		15	24		36		30	
			6 V		14	20		31		26	
t <sub>t</sub>		Any	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	



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switching characteristics over recommended operating free-air temperature range,  $C_L = 150 \text{ pF}$   
(unless otherwise noted) (see Figure 1)

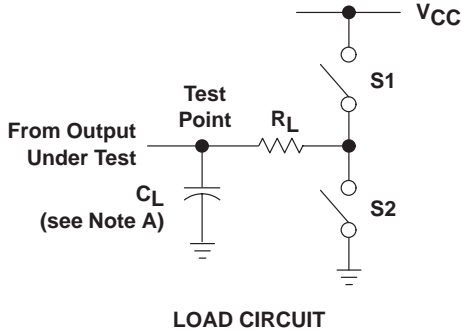
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC125		SN74HC125		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	2 V		67	150		225		190	ns
			4.5 V		19	30		45		38	
			6 V		15	25		39		32	
$t_{en}$	$\overline{OE}$	Y	2 V		100	135		200		170	ns
			4.5 V		20	27		40		34	
			6 V		17	23		34		29	
$t_t$		Any	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

operating characteristics,  $T_A = 25^\circ\text{C}$

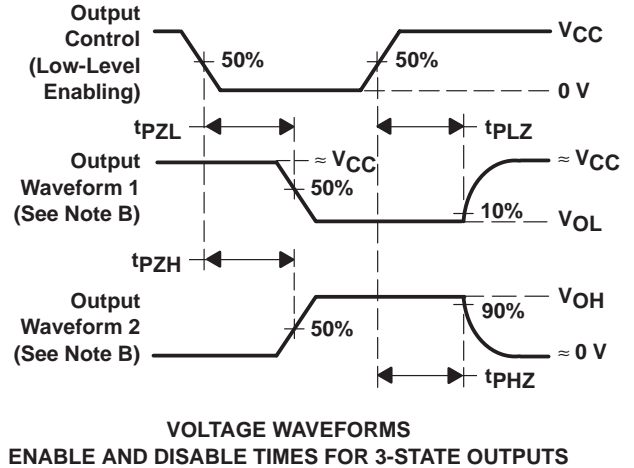
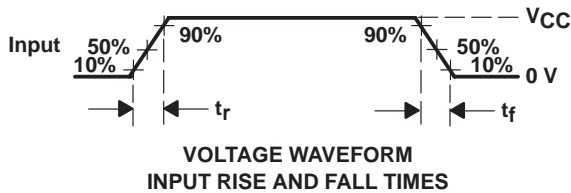
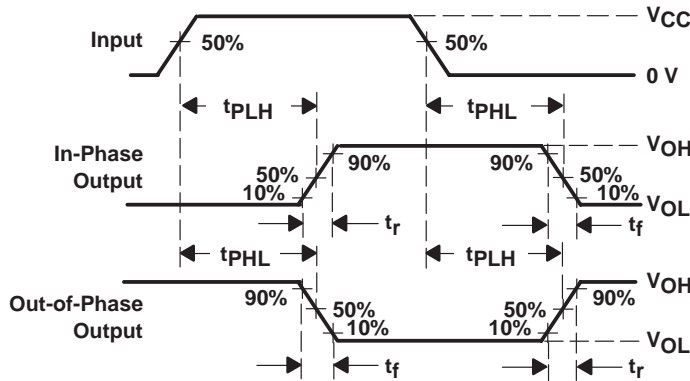
PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per gate	No load	45	pF



PARAMETER MEASUREMENT INFORMATION



PARAMETER	$R_L$	$C_L$	S1	S2
$t_{en}$	1 k $\Omega$	50 pF or 150 pF	Open	Closed
			Closed	Open
$t_{dis}$	1 k $\Omega$	50 pF	Open	Closed
			Closed	Open
$t_{pd}$ or $t_t$	—	50 pF or 150 pF	Open	Open



- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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