

## 19N10

Power MOSFET

15.6A, 100V N-CHANNEL  
POWER MOSFET

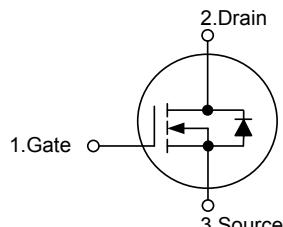
## ■ DESCRIPTION

The UTC 100V N-Channel enhancement mode power field effect transistors (MOSFET) are produced by UTC's planar stripe, DMOS technology which has been tailored especially in the avalanche and commutation mode to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse. They are suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

## ■ FEATURES

- \*  $R_{DS(ON)} < 0.1\Omega$  @  $V_{GS} = 10$  V
- \* Ultra low gate charge ( typical 19nC )
- \* Low reverse transfer Capacitance (  $C_{RSS}$  = typical 32pF )
- \* Fast switching capability
- \* Avalanche energy Specified
- \* Improved dv/dt capability, high ruggedness

## ■ SYMBOL



## ■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
19N10L-T3P-T	19N10G-T3P-T	TO-3P	G	D	S	Tube
19N10L-TA3-T	19N10G-TA3-T	TO-220	G	D	S	Tube
19N10L-TM3-T	19N10G-TM3-T	TO-251	G	D	S	Tube
19N10L-TMS-T	19N10G-TMS-T	TO-251S	G	D	S	Tube
19N10L-TN3-R	19N10G-TN3-R	TO-252	G	D	S	Tape Reel
19N10L-TQ2-R	19N10G-TQ2-R	TO-263	G	D	S	Tape Reel
19N10L-TQ2-T	19N10G-TQ2-T	TO-263	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

 (1)T: Tube, R: Tape Reel (2) T3P: TO-3P, TA3: TO-220, TM3: TO-251, TMS: TO-251S, TN3: TO-252, TQ2: TO-263 (3) L: Lead Free, G: Halogen Free

**■ MARKING INFORMATION**

PACKAGE	MARKING
TO-220	
TO-251	
TO-251S	
TO-252	
TO-263	<p>The marking diagram for the TO-263 package shows the following layout: 'UTC' at the top, followed by '19N10' in a larger font, and a small square at the end. Below this, there is a row of six squares labeled 'Lot Code' with an arrow pointing left. At the bottom right, there is a single square labeled '1'. To the right of the marking area, three labels are defined: 'L: Lead Free' with an arrow pointing right, 'G: Halogen Free' with an arrow pointing right, and 'Data Code' with an arrow pointing right.</p>

■ ABSOLUTE MAXIMUM RATINGS ( $T_c=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT	
Drain-Source Voltage	$V_{DSS}$	100	V	
Gate-Source Voltage	$V_{GSS}$	$\pm 25$	V	
Continuous Drain Current	$I_D$	15.6	A	
Pulsed Drain Current (Note 2)	$I_{DM}$	62.4	A	
Avalanche Current (Note 2)	$I_{AR}$	15.6	A	
Single Pulsed Avalanche Energy (Note 3)	$E_{AS}$	220	mJ	
Repetitive Avalanche Energy (Note 2)	$E_{AR}$	5.0	mJ	
Peak Diode Recovery dv/dt (Note 4)	dv/dt	6.0	V/ns	
Power Dissipation	TO-251/TO-251S	$P_D$	50	W
	TO-252		62.5	W
	TO-220/TO-263		178	W
	TO-3P			
Junction Temperature	$T_J$	+150	$^\circ\text{C}$	
Storage Temperature	$T_{STG}$	-55 ~ +150	$^\circ\text{C}$	

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Pulse width limited by  $T_{J(\text{MAX})}$

3.  $L=1.8\text{mH}$ ,  $I_{AS}=15.6\text{A}$ ,  $V_{DD}=25\text{V}$ ,  $R_G=25\ \Omega$ , Starting  $T_J=25^\circ\text{C}$

4.  $I_{SD}\leq 19\text{A}$ ,  $di/dt \leq 300\text{A}/\mu\text{s}$ ,  $V_{DD}\leq BV_{DSS}$ , Starting  $T_J=25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT	
Junction to Ambient	TO-251/TO-251S	$\theta_{JA}$	50	$^\circ\text{C/W}$
	TO-252		62.5	$^\circ\text{C/W}$
	TO-220/TO-263		40	$^\circ\text{C/W}$
	TO-3P			
Junction to Case	TO-251/TO-251S	$\theta_{JC}$	2.5	$^\circ\text{C/W}$
	TO-252		2.0	$^\circ\text{C/W}$
	TO-220/TO-263		0.7	$^\circ\text{C/W}$
	TO-3P			

■ ELECTRICAL CHARACTERISTICS ( $T_J=25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_D=250\mu\text{A}$	100			V
Breakdown Voltage Temperature Coefficient	$\Delta \text{BV}_{\text{DSS}}/\Delta T_J$	$I_D=250\mu\text{A}$ , Referenced to $25^\circ\text{C}$		0.1		$\text{V}/^\circ\text{C}$
Drain-Source Leakage Current	$I_{\text{DSS}}$	$V_{\text{DS}}=100\text{V}, V_{\text{GS}}=0\text{V}$ $V_{\text{DS}}=100\text{V}, T_J=125^\circ\text{C}$		1	$\mu\text{A}$	
Gate-Source Leakage Current	Forward Reverse	$I_{\text{GSS}}$	$V_{\text{GS}}=25\text{V}, V_{\text{DS}}=0\text{V}$ $V_{\text{GS}}=-25\text{V}, V_{\text{DS}}=0\text{V}$	100 -100	nA	
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{\text{GS(TH)}}$	$V_{\text{DS}}=V_{\text{GS}}, I_D=250\mu\text{A}$	2.0		4.0	V
Static Drain-Source On-Resistance	$R_{\text{DS(ON)}}$	$V_{\text{GS}}=10\text{V}, I_D=7.8\text{A}$		0.078	0.1	$\Omega$
Forward Transconductance	$g_{\text{FS}}$	$V_{\text{DS}}=40\text{V}, I_D=7.8\text{A}$ (Note 1)			11	S
<b>DYNAMIC PARAMETERS</b>						
Input Capacitance	$C_{\text{ISS}}$	$V_{\text{DS}}=25\text{V}, V_{\text{GS}}=0\text{V}, f=1.0\text{MHz}$		600	780	pF
Output Capacitance	$C_{\text{OSS}}$			165	215	pF
Reverse Transfer Capacitance	$C_{\text{RSS}}$			32	40	pF
<b>SWITCHING PARAMETERS</b>						
Total Gate Charge	$Q_G$	$V_{\text{DS}}=50\text{V}, I_D=1.3\text{A}, V_{\text{GS}}=10\text{V}$ (Note 1, 2)		19	25	nC
Gate Source Charge	$Q_{\text{GS}}$			6		nC
Gate Drain Charge	$Q_{\text{GD}}$			6		nC
Turn-ON Delay Time	$t_{\text{D(ON)}}$	$V_{\text{DD}}=30\text{V}, I_D=0.5\text{A}, R_G=25\Omega$ (Note 1, 2)		45	60	ns
Turn-ON Rise Time	$t_R$			70	90	ns
Turn-OFF Delay Time	$t_{\text{D(OFF)}}$			165	250	ns
Turn-OFF Fall-Time	$t_F$			78	90	ns
<b>SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS</b>						
Diode Forward Voltage	$V_{\text{SD}}$	$V_{\text{GS}}=0\text{V}, I_S=15.6\text{A}$			1.5	V
Maximum Body-Diode Continuous Current	$I_S$				15.6	A
Maximum Pulsed Drain-Source Diode Forward Current	$I_{\text{SM}}$				62.4	A
Body Diode Reverse Recovery Time	$t_{\text{RR}}$	$V_{\text{GS}}=0\text{V}, I_S=19\text{A}$		78		ns
Body Diode Reverse Recovery Charge	$Q_{\text{RR}}$	$dI_F/dt=100\text{A}/\mu\text{s}$ (Note 1)		200		nC

Note: 1. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$

2. Essentially independent of operating temperature

■ TEST CIRCUITS AND WAVEFORMS

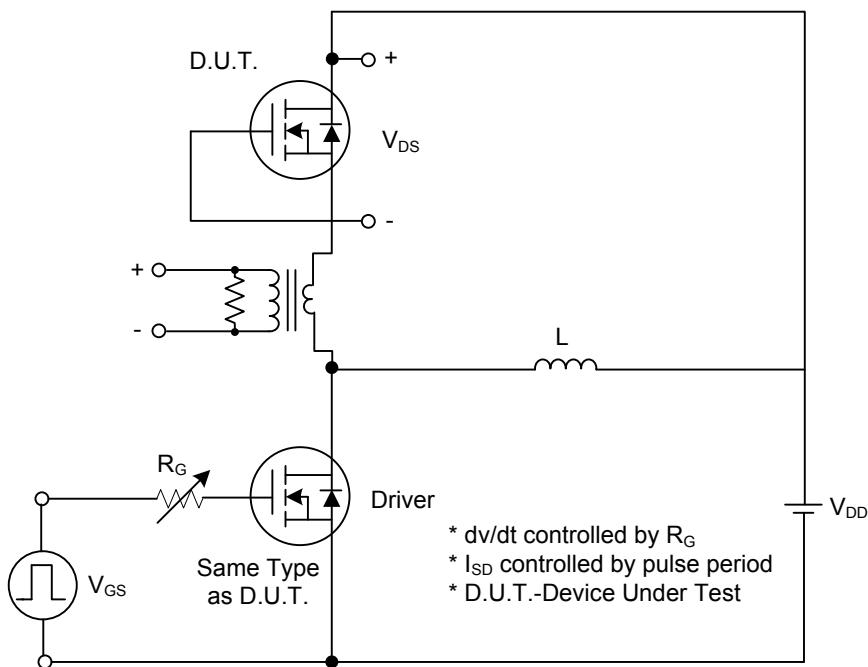


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

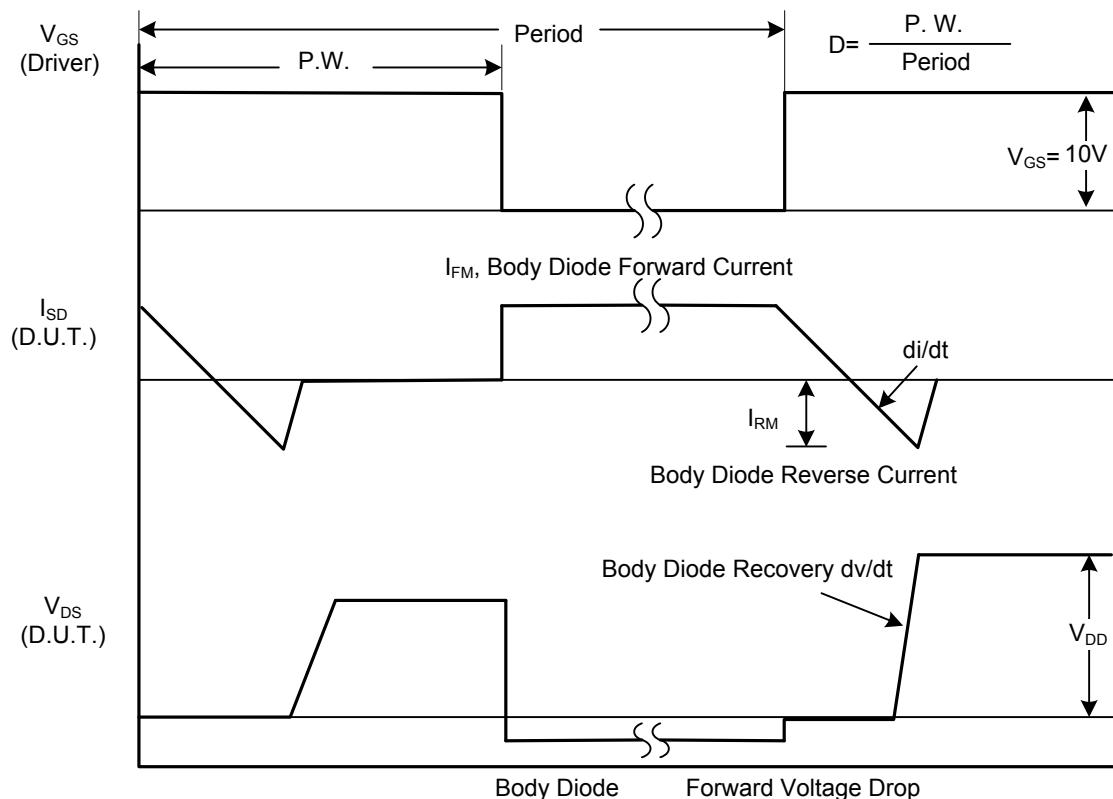


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

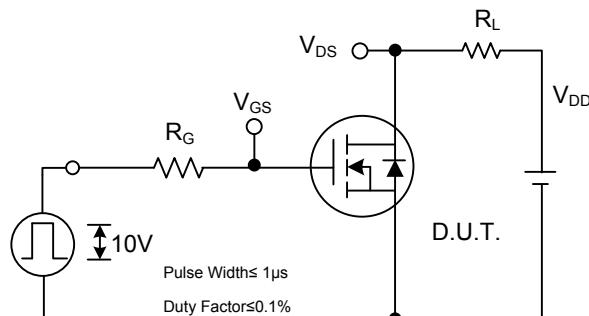


Fig. 2A Switching Test Circuit

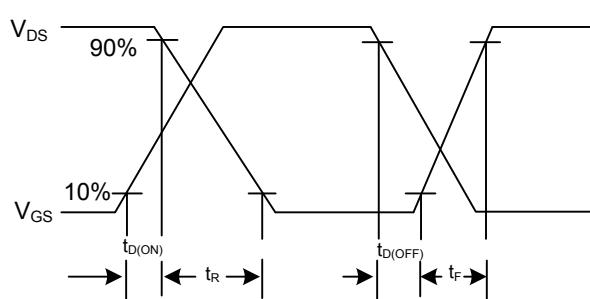


Fig. 2B Switching Waveforms

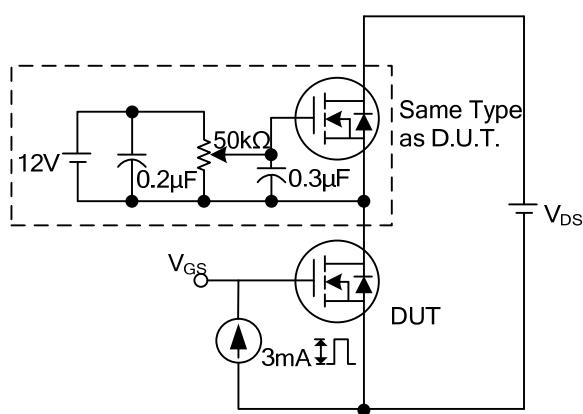


Fig. 3A Gate Charge Test Circuit

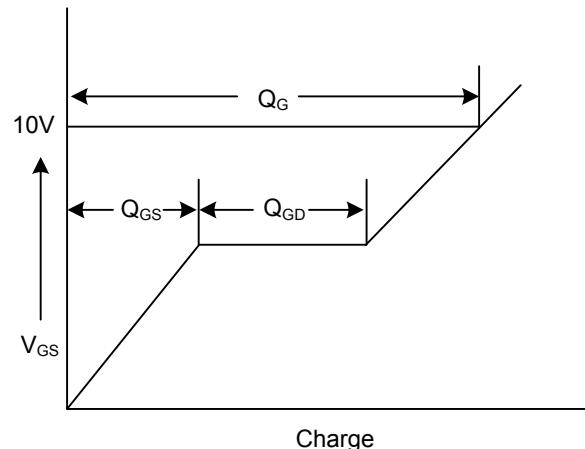


Fig. 3B Gate Charge Waveform

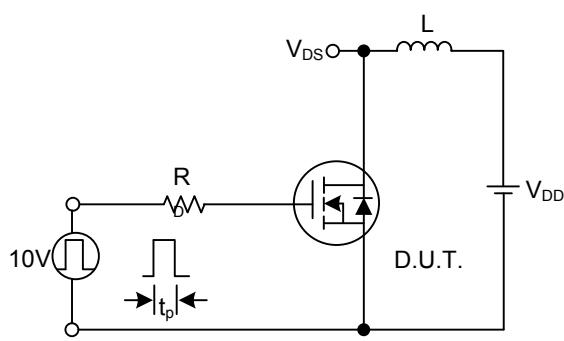


Fig. 4A Unclamped Inductive Switching Test Circuit

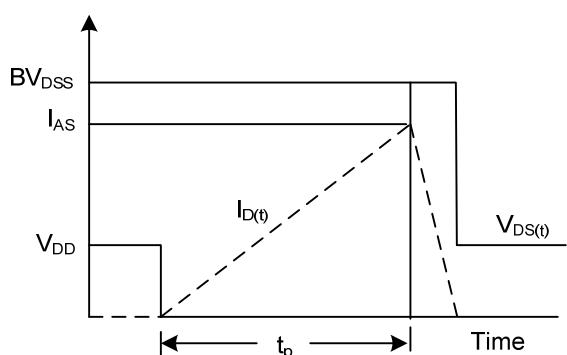
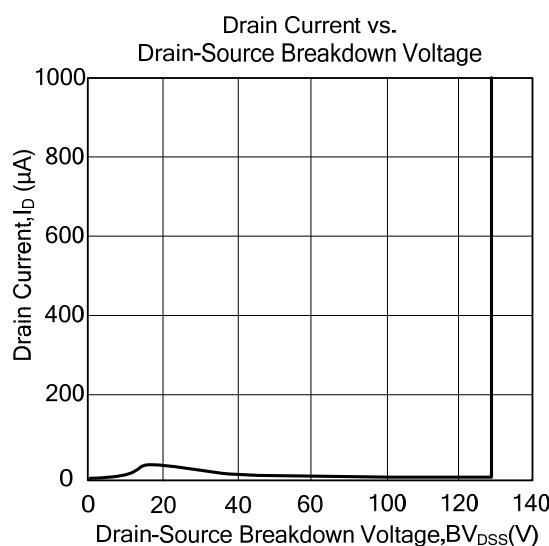
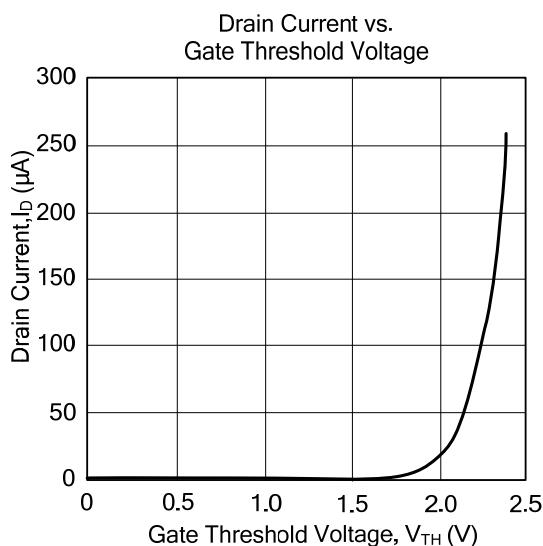
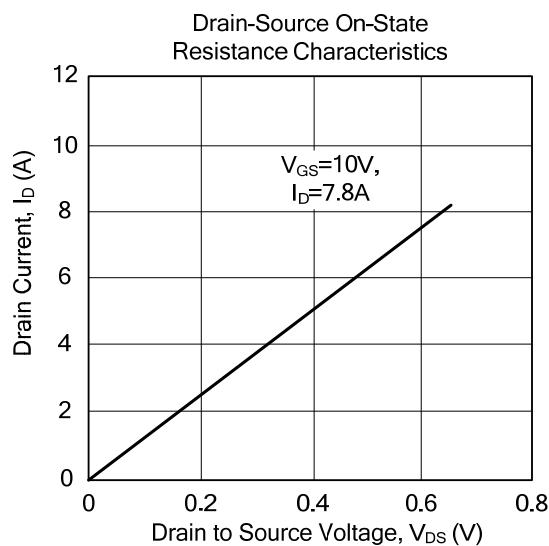
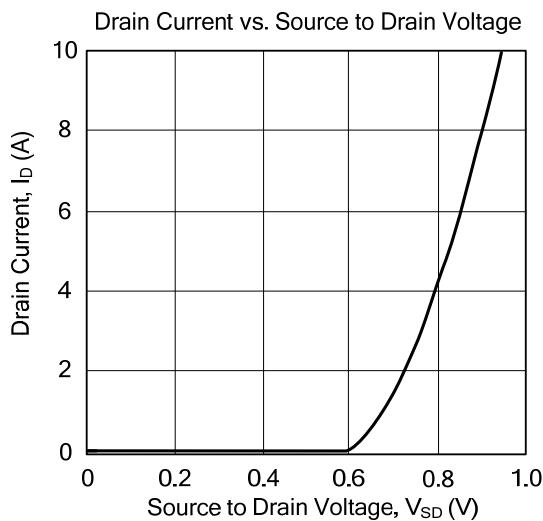


Fig. 4B Unclamped Inductive Switching Waveforms

■ TYPICAL CHARACTERISTICS



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